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S5933QE PCI Controller Device Summary

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PCI S5933QE Matchmaker Device Summary
Revision 2, November 1, 1997

The following are all known device and document variations for the AMCC S5933QE PCI Matchmaker and 1997 device data book. The workarounds described below are factory suggestions and are not to imply the only or all possible solutions. Contact your local Field Application Engineer for new workaround developments. Also contact your FAE for the latest design notes and data book corrections or see the AMCC home page at www.amcc.com.

D8:   Bus Master Burst Write Operation with an Asynchronous FIFO Interface

Description : When performing a bus master write to the PCI bus, if only one location of the FIFO remains full, the S5933 deasasserts FRAME# on the next clock to indicate the last data phase is in progress. If another value is written from the add-on at the right moment, an internal condition may cause IRDY# to remain asserted to sustain the burst, but FRAME# has already been dasserted.

Workaround: Externally synchronizing WRFIFO# or WR# to BPCLK moves the rising edge of the write strobe to prevent this event from occuring. Request separate D8 applications note from your local FAE for more detail.

Status: No Factory D8 alteration planned.

D14.1:   False Add-On to PCI FIFO Empty Indication

Description : If the last data in the Add-On to PCI FIFO is written by the S5933 to the PCI bus and receives a target retry, the FWE output and Add-On to PCI FIFO status bits will go active, indicating that the FIFO is empty, even though the final data has not yet been transferred. This is only a problem when using Add-On initiated bus mastering when FWE is used as a condition to deassert AMWEN at the end of a bus master write. Using FWE in this way could cause AMWEN to be deasserted before the last bus master write has successfully completed.

Workaround: Instead of using FWE, the Add-On interrupt signal, IRQ#, can beconfigured to go active when the transfer count reaches zero. The transfer count is only updated when data is successfully written.

Note :   When FWE and the status bits indicate that the Add-On to PCI FIFO is empty, there are 8 empty locations in the FIFO. The data for the transfer which received the retry is stored in a holding register and is not involved.

Status: No factory D14.1 alteration planned.

D17:   PCI to Add-On FIFO Loses Data when Written w/o all PCI Byte Enables Asserted

Description: When writing to the FIFO from the PCI side (as a target), if the byte enable for the specified byte lane is not active, then that data could be lost. The problem is encountered when the S5933 Operation Registers are mapped to I/O and the FIFO is written to 16 bits at a time, alternating between bytes 0,1 and bytes 2,3. Under certain conditions internal to the S5933, when the byte enable for the FIFO advance byte lane is not active, the data written is not captured by the FIFO.

Workaround 1: Always write the FIFO with the byte enable that corresponds to the FIFO advance byte lane active.

Workaround 2: Always perform 32-bit FIFO writes from the PCI bus.

Status : No factory D17 alteration planned.

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B1: PCI Bus Hang when S5933 PCI initiated Bus Mastering is Disabled and the S5933 has GNT#

Description: S5933 PCI initiated bus mastering hangs the bus when the S5933 gets GNT# when another master is disabling bus mastering through THE MCSR register before the transfer count reaches 0. This only occurs when the PCI bus arbiter offers GNT# to the S5933 while another master is executing a transaction on the PCI bus. If the active transaction disables S5933 bus mastering, then the S5933 will start a bus master transaction, then realize its bus mastering is disabled and hang on the bus with FRAME# active.

Workaround 1: Use the S5933 transfer count register(s) going to 0 in order to get the S5933 to stop bus mastering before it is disabled through the MCSR. The transfer counts should be programmed for the number of bytes that need to be transferred. When that number of bytes has been transferred, the S5933 will get off the bus normally.

Workaround 2: Write the transfer count to 4. This safely aborts the bus master transfer after one more PCI transaction. Then bus mastering can be disabled through the MCSR.

Status : No factory B1 alteration planned.

B2: S5933 Bus Master Writes to Bus Master Read Address when Bus Master Write has priority over Bus Master Read

Description: When bus master writes are set up to have priority over bus master reads (MCSR register, bit 12=0, bit 8=1) and both bus master writes and reads are enabled at the same time, then the S5933 could write to the read address.

Workaround: Set the bus master write and read to the same priority.

Status : No factory B2 alteration planned.

1997 Data Book Timing Call Out Error

Description: Chapter 13, page 13-11 shows time t_{165} for RDEMPTY valid as 15 ns maximum. This should be 12 ns maximum for QE silicon. Chapter 13, page 13-12 shows time t_{167} for WRFULL valid as 17 ns maximum. This should be 11 ns maximum for QE silicon.

Status : The data book to be updated.

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Table of Contents

1.   What´s in the data-books ?

The Spring 1996 data-book was referring to the S5933Q timings.
We found out by the end of 1996 that some Add-on timings required re-simulations for the S5933 QX revisions. That´s what we finalized in early 1997.
You have received an early version of those updated timings for FIFO access in Spring 1997, valid for the S5933 QA and QB and QC.
Final timings, also valid for the S5933 QE, now in the 1997 Data-book (with two exceptions mentioned further) show some major changes compared to the Q timings from Spring 96. These are real worst case timings valid for the full temperature range, voltage range and taking into consideration the process variations. We do understand those timings may create some trouble.
Please carefully review the S5933 QE transition design note. This will tell you if your application requires any modification.

2.   What is the S5933QE ?

Thanks to costumers feedback, we worked on the improvements we could bring to the part and decided to design the S5933QE. This version brings a 6ns improvement on FIFO status flag (RDEMPTY and WRFULL) availability in synchronous mode compared to the S5933QC. It gives more time for the generation of RDFIFO# or WRFIFO#.

3.   Timings for Synchronous RDFIFO# and WRFIFO# in the 1997 Data-book

Please add the following corrections to your 1997 Data-book:

t165 page 13-11   for QC=15ns   RDEMPTY valid from BPCLK rising edge
                         for QE=12ns

t167 page 13-12   for QC=17ns   WRFULL valid from BPCLK rising edge
                         for QE=11ns

The S5933QE gives more margins for FIFO synchronous operations. A status signals are valid earlier, the RDFIFO# or WRFIFO# command can be asserted/de-asserted with sufficient setup time to rising edge of BPCLK.

4. New designs with the S5933QE using the FIFO is DMA mode

Based on our experience with the S5933 in DMA applications using the internal FIFOs, we´d like to give you a few tips on how to successfully implement your Add-on interface logic:

1.   Always use synchronous logic (state machine) to generate strobes and read status (all signals change on a BPCLK rising edge).
2.   Use synchronous FIFO mode (defined in NVRAM location 45h, bits 5-6=00).
3.   Only use RDFIFO# / WRFIFO# signals instead of RD# / WR# to access the FIFO.
4.   Do not use FRF or FWE to monitor a DMA transfer but only to initiate the transfer.
5.   First data of a FIFO read is asynchronous: data is valid 12ns max after the falling edge of RDFIFO#.
            All following data is synchronous to BPCLK with a setup time of 14ns min and a hold time of 6ns min.

Please carefully review the FIFO timings in Figure 1 and Figure 2.
Let suppose the PCI bus runs at 33MHz, the BPCLK cycle time is then 30ns.
FIFO write: When the Add-on to PCI FIFO is full, WRFULL is asserted 11ns max after the rising edge of BPCLK.
As WRFIFO# requires a 12ns setup, this gives 7ns to de-assert this command before the next BPCLK edge.
FIFO read: When PCI to Add-on FIFO is empty, RDEMPTY is asserted 12ns max after the rising edge of BPCLK.
As RDFIFO# requires an 8ns setup, this gives 10ns to de-assert this command before the next BPCLK edge.

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S5933QE Synchronous RDFIFO# Timing

S5933QE Synchronous RDFIFO# Timing

Functional Operation Range (V_{CC}=5.0V 5%, 0C to 70C T_S50pf load on outputs)

Symbol	Parameter	Min	Max	Units	Notes
t_{144}	RDFIFO# Setup to BPCLK Rising Edge	8	26	ns	1
t_{145}	RDFIFO# Low Time	8		ns	
t_{146}	RDFIFO# Low to DQ(31:0) Driven		12	ns	
t_{148}	RDFIFO# High to DQ(31:0) Float		3	ns	
t_{149}	DQ(31:0) Valid from BPCLK Rising Edge		16	ns	3
t_{165}	PCI to ADD-ON FIFO RDEMPTY Valid from BPCLK Rising Edge	8	12	ns	2

Notes:
1. Min and Max Times are indicated to allow increased valid data time as shown by dashed lines.
2. State change of RDEMPTY shown below is reference only. Actual change would indicate no Data 3 available.
3. Valid applies after first access. First access is async with following as sync accesses.
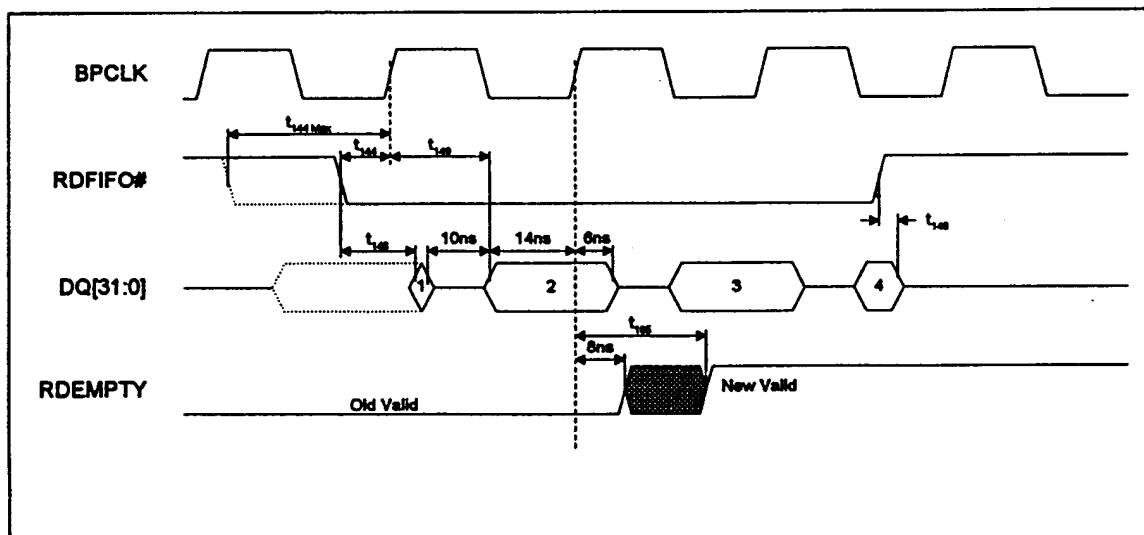
Figure 1

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S5933QE Synchronous WRFIFO# Timing

S5933QE Synchronous WRFIFO# Timing

Functional Operation Range (V_{CC}=5.0V 5%, 0C to 70C T_S50pf load on outputs)

Symbol	Parameter	Min	Max	Units	Notes
t_{150}	WRFIFO# Setup to BPCLK Rising Edge	12		ns	
t_{150e}	WRFIFO# Hold Time to BPCLK Rising Edge	0		ns	
t_{151}	DQ(31:0) Setup to BPCLK Rising Edge	7			
t_{151e}	DQ(31:0) Hold from BPCLK Rising Edge	0			
t_{167}	ADD-ON to PCI FIFO WRFULL Valid from BPCLK Rising Edge	6	11	ns	1

Notes:
1. State change of WRFULL shown below is reference only. Actual change would indicate no Data 3 written.
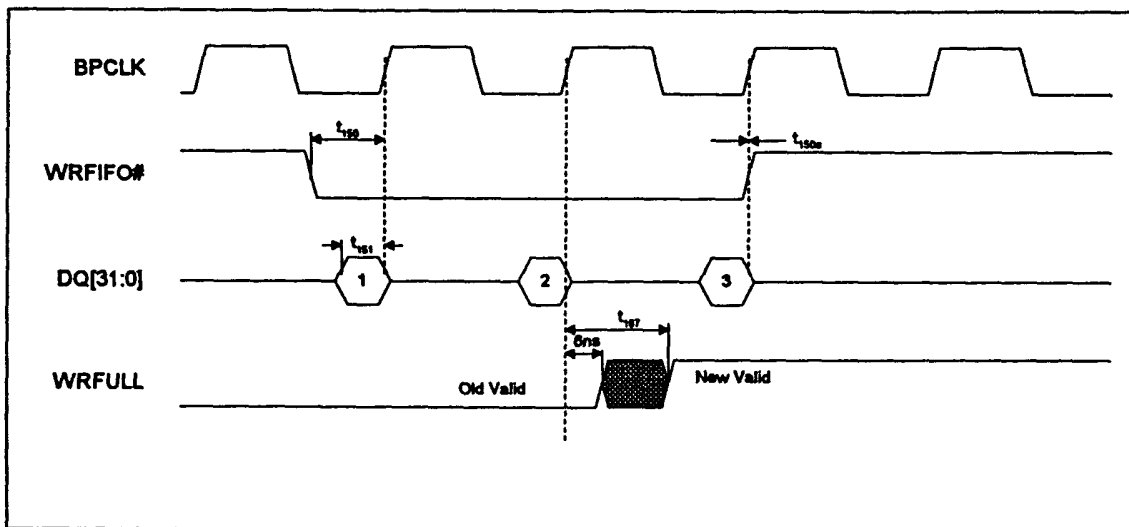
Figure 2

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DESIGN NOTE   S5933

September 6, 1996

Errata D8 Workaround Detail

Errata D8: Bus Master Burst Write Operation with an Asynchronous FIFO Interface

Description : When performing a bus master write to the PCI bus, if only one location of the FIFO remains full, the S5933 deasasserts FRAME# on the next clock to indicate the last data phase is in progress. If another value is written from the add-on at the right moment, an internal condition may cause IRDY# to remain asserted to sustain the burst, but FRAME# has already been dasserted.

Workaround: Externally synchronizing WRFIFO# or WR# to BPCLK moves the rising edge of the write strobe prevents this errata from occurring. The WRFIFO# or WR# is to be synced with the rising edge of BPCLK.

The object of this Workaround is to avoid an internal S5933 timing window which, when WRFIFO# is deasserted in, will cause the errata phenomena to occur. This window is approximately 4ns before the rising edge of PCI CLK to approximately 4ns after the rising edge of PCI CLK. The ADD-ON side can detect this window by examining the BPCLK. The BPCLK signal will always lag the PCI CLK by the average propagation delay time of an internal S5933 buffer driving BPCLK. The average propagation delay time for this buffer is 4ns. Therefore, taking this into account and variations in timing windows due to lot variations and temperature, WRFIFO# or WR# may be deasserted anytime from 1 ns after the rise of BPCLK till it´s fall. The timing diagram below details this window.