MJ21294

NPN Silicon Power Transistor

With superior safe operating area performance, this power transistor is ideal for high temperature linear control circuits.

Features

- Exceptional Safe Operating Area
- Dual Die Device with Standard 40 mil pins
- Pb−Free Package is Available*

Benefits

- More Reliable Performance at Higher Powers
- Designed for Higher Temperature SOA
- Interchangeable with Standard Single Die TO−3 Devices

Applications

- Linear Power Supplies
- Battery Conditioning
- DC Motor Control
- Positioners
- DC Heating Controls
- High Power Audio Amplifiers

ON Semiconductor®

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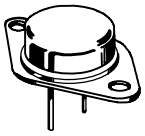
20 AMPS
250 VOLTS
350 WATTS

MARKING DIAGRAM



TO−204AA
(TO−3)
CASE 1−07

MJ21294 = Specific Device Code
G = Pb−Free Package
A = Assembly Site
YY = Year
WW = Work Week
MEX = Assembly Location

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	250	Vdc
Collector−Base Voltage	V_{CBO}	400	Vdc
Emitter−Base Voltage	V_{EBO}	5.0	Vdc
Collector−Emitter Voltage − 1.5 V	V_{CEX}	400	Vdc
Collector Current − Continuous Peak (Note 1)	I_C	20 40	Adc
Base Current − Continuous	I_B	5.0	Adc
Total Power Dissipation @ T_C = 25°C Derate Above 25°C	P_D	350 2.0	W W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	− 65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	0.50	°C/W

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Pulse Test: Pulse Width = 5 μs, Duty Cycle ≤10%. (continued)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ORDERING INFORMATION

Device	Package	Shipping
MJ21294	TO−3	100 Units / Tray
MJ21294G	TO−3 (Pb−Free)	100 Units / Tray

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (I_C = 100 mAdc, I_B = 0)	$V_{CEO(sus)}$	250	−	−	Vdc
Collector Cutoff Current (V_{CE} = 200 Vdc, I_B = 0)	I_{CEO}	−	−	100	μAdc
Emitter Cutoff Current (V_{CE} = 5 Vdc, I_C = 0)	I_{EBO}	−	−	10	μAdc
Collector Cutoff Current (V_{CE} = 250 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	I_{CEX}	−		100	μAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased (V_{CE} = 40 Vdc, t = 1 s (non−repetitive)	$I_{S/b}$	6.0	−	−	Adc
ON CHARACTERISTICS					
DC Current Gain (I_C = 8 Adc, V_{CE} = 5 Vdc) (I_C = 16 Adc, V_{CE} = 5 Vdc)	h_{FE}	 40 15	 − −	 100 −	
Base−Emitter On Voltage (I_C = 8 Adc, V_{CE} = 5 Vdc)	$V_{BE(on)}$	−	−	1.4	Vdc
Collector−Emitter Saturation Voltage (I_C = 8 Adc, I_B = 0.8 Adc) (I_C = 16 Adc, I_B = 3.2 Adc)	$V_{CE(sat)}$	 − −	 − −	 0.5 1.0	Vdc
DYNAMIC CHARACTERISTICS					
Current Gain Bandwidth Product (I_C = 1 Adc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)	f_T	4	−	−	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1 MHz)	C_{ob}	−	−	500	pF

NOTE: Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤2%

TYPICAL CHARACTERISTICS

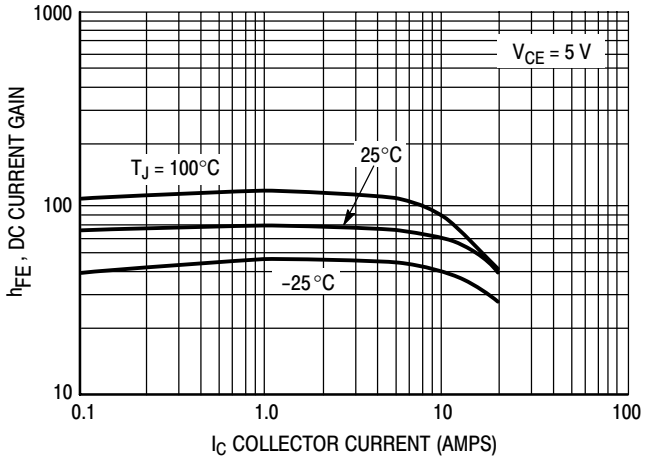


Figure 1. DC Current Gain

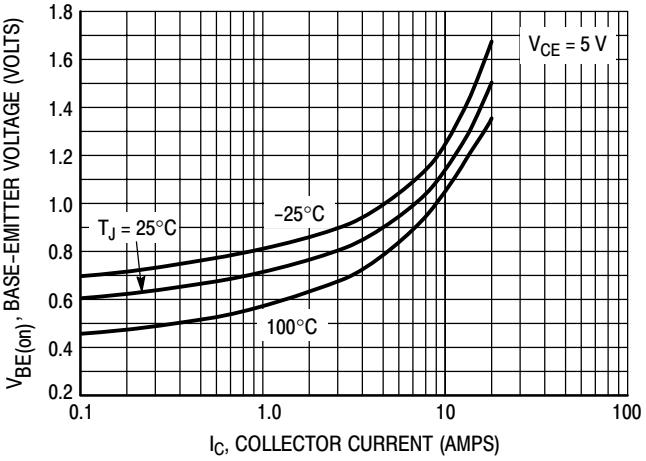


Figure 2. Base−Emitter Voltage

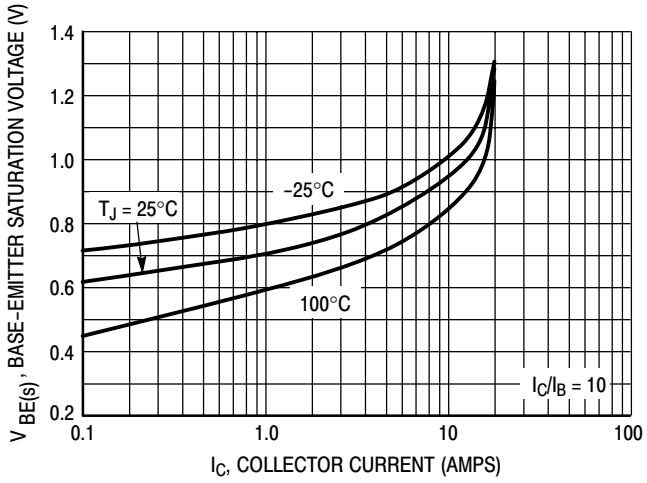


Figure 3. Base−Emitter Saturation Voltage

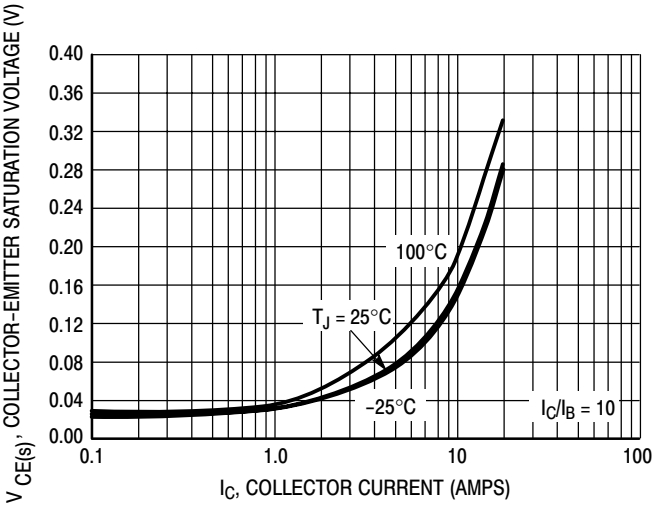


Figure 4. Collector−Emitter Saturation Voltage

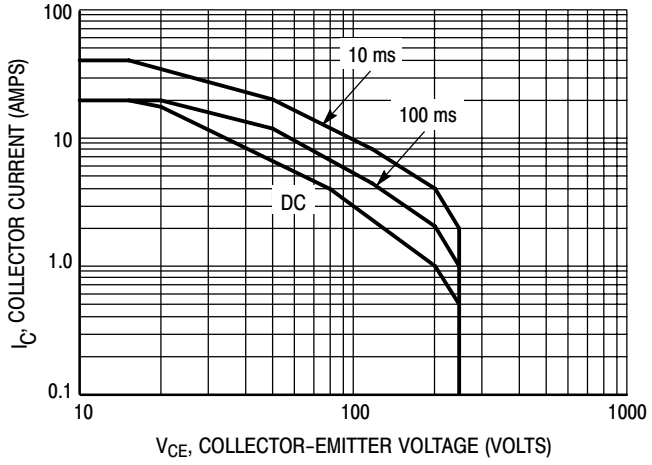


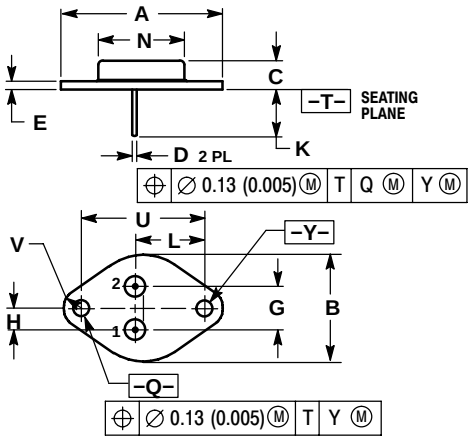
Figure 5. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor; average junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power than can be handled to values less than the limitations imposed by second breakdown.

PACKAGE DIMENSIONS

TO−204AA (TO−3)
CASE 1−07
ISSUE Z



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO−204AA OUTLINE SHALL APPLY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.550 REF		39.37 REF	
B	---	1.050	---	26.67
C	0.250	0.335	6.35	8.51
D	0.038	0.043	0.97	1.09
E	0.055	0.070	1.40	1.77
G	0.430 BSC		10.92 BSC	
H	0.215 BSC		5.46 BSC	
K	0.440	0.480	11.18	12.19
L	0.665 BSC		16.89 BSC	
N	---	0.830	---	21.08
Q	0.151	0.165	3.84	4.19
U	1.187 BSC		30.15 BSC	
V	0.131	0.188	3.33	4.77

STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
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