16,384-BIT ROM WITH I/O PORTS
*16,384-BIT EPROM WITH I/O PORTS

DESCRIPTION

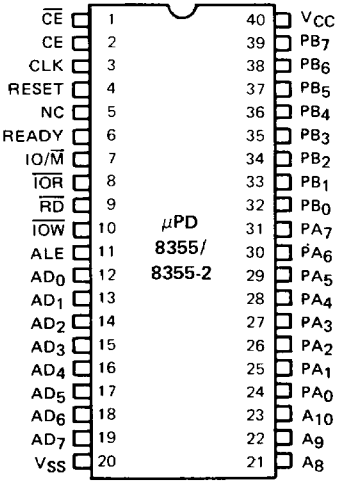
The μPD8355 and the μPD8755A are μPD8085A Family components. The μPD8355 contains 2048 x 8 bits of mask ROM and the μPD8755A contains 2048 x 8 bits of mask EPROM for program development. Both components also contain two general purpose 8-bit I/O ports. They are housed in 40 pin packages, are designed to directly interface to the μPD8085A, and are pin-for-pin compatible with each other.

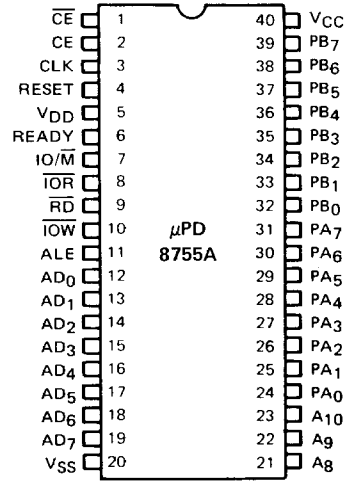
FEATURES

- 2048 X 8 Bits Mask ROM (μPD8355 and μPD8355-2)
- 2048 X 8 Bits Mask EPROM (μPD8755A)
- 2 Programmable I/O Ports
- Single Power Supplies: +5V
- Directly Interfaces to the μPD8085A
- Pin for Pin Compatible
- μPD8755A: UV Erasable and Electrically Programmable
- μPD8335 and μPD8355-2 Available in Plastic Package
- μPD8755A Available in Ceramic Package

6

PIN CONFIGURATIONS





NC: Not Connected

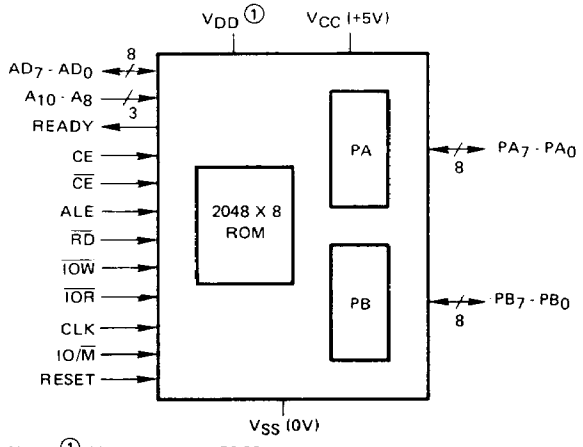
Rev/2

FUNCTIONAL DESCRIPTION

The μPD8355 and μPD8755A contain 16,384 bits of mask ROM and EPROM respectively, organized as 2048 X 8. The 2048 word memory location may be selected anywhere within the 64K memory space by using the upper 5 bits of address from the μPD8085A as a chip select.

The two general purpose I/O ports may be programmed input or output at any time. Upon power up, they will be reset to the input mode.

BLOCK DIAGRAM



Note: ① V_{DD} applies to μPD8755A only.

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature (μPD8355)	0°C to +70°C
(μPD8755A)	0°C to +70°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin (μPD8355)	-0.5 to +7V ①
(μPD8755A)	-0.5 to +7V ①
Power Dissipation	1.5W

Note: ① With Respect to Ground

T_a = 25°C

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = 5V ± 5%

PARAMETER	SYMBOL	LIMITS MIN	LIMITS MAX	UNIT	TEST CONDITIONS
Input Low Voltage	V_{IL}	-0.5	0.8	V	V_{CC} = 5.0V ①
Input High Voltage	V_{IH}	2.0	V_{CC}+0.5	V	V_{CC} = 5.0V ①
Output Low Voltage	V_{OL}		0.45	V	I_{OL} = 2 mA
Output High Voltage	V_{OH}	2.4		V	I_{OH} = -400 μA
Input Leakage	I_{IL}		10	μA	V_{IN} = V_{CC} to 0V
Output Leakage Current	I_{LO}		±10	μA	0.45V ≤ V_{OUT} ≤ V_{CC}
V_{CC} Supply Current	I_{CC}		180/125	mA	μPD8355/8355-2

Note: ① These conditions apply to μPD8355/μPD8355-2 only.

PIN IDENTIFICATION

PIN NO.	PIN SYMBOL	PIN NAME	FUNCTION
1,2	$\overline{CE}$, CE	Chip Enables	Enable Chip activity for memory or I/O
3	CLK	Clock Input	Used to Synchronize Ready
4	Reset	Reset Input	Resets PA and PB to all inputs
5 ①	NC	Not Connected	
5 ②	V_{DD}	Programming Voltage	Used as a programming voltage, tied to +5V normally
6	Ready	Ready Output	A tri-state output which is active during data direction register loading
7	IO/$\overline{M}$	I/O or Memory Indicator	An input signal which is used to indicate I/O or memory activity
8	IOR	I/O Read	I/O Read Strobe In
9	$\overline{RD}$	Memory Read	Memory Read Strobe In
10	$\overline{IOW}$	I/O Write	I/O Write Strobe In
11	ALE	Address Low Enable	Indicates information on Address/Data lines is valid
12-19	AD_0-AD_7	Low Address/Data Bus	Multiplexed Low Address and Data Bus
20	V_{SS}	Ground	Ground Reference
21-23	A_8-A_{10}	High Address	High Address inputs for ROM reading
24-31	PA_0-PA_7	Port A	General Purpose I/O Port
32-39	PB_0-PB_7	Port B	General Purpose I/O Port
40	V_{CC}	5V Input	Power Supply

Notes: ① μPD8355
② μPD8755A

I/O PORTS

I/O port activity is controlled by performing I/O reads and writes to selected I/O port numbers. Any activity to and from the μPD8355 requires the chip enables to be active. This can be accomplished with no external decoding for multiple devices by utilizing the upper address lines for chip selects. ① Port activity is controlled by the following I/O addresses:

AD_1	AD_0	PORT SELECTED	FUNCTION
0	0	A	Read or Write PA
0	1	B	Read or Write PB
1	0	A	Write PA Data Direction
1	1	B	Write PB Data Direction

Since the data direction registers for PA and PB are each 8-bits, any pin on PA or PB may be programmed as input or output (0 = in, 1 = out).

Note: ① During ALE time the data/address lines are duplicated on A_{15}-A_8.

AC CHARACTERISTICS

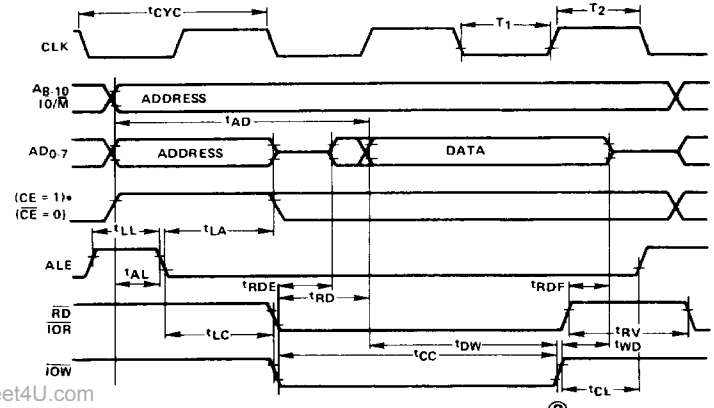
T_a = 0°C to 70°C; V_{CC} = 5V ± 5%

Symbol	Parameter	8355 Min.	8355 Max.	8355-2 Min.	8355-2 Max.	Unit	Test Conditions
t_{CYC}	Clock Cycle Time	320		200		ns	C_{LOAD} = 150 pF
T_1	CLK Pulse Width	80		40		ns	
T_2	CLK Pulse Width	120		70		ns	
t_f, t_r	CLK Rise and Fall Time		30		30	ns	
t_{AL}	Address to Latch Set Up Time	50		30		ns	150 pF Load
t_{LA}	Address Hold Time after Latch	80		30		ns	
t_{LC}	Latch to READ/WRITE Control	100		40		ns	
t_{RD}	Valid Data Out Dealy from READ Control		170		140	ns	
t_{AD}	Address Stable to Data Out Valid		400		330	ns	
t_{LL}	Latch Enable Width	100		70		ns	
t_{RDF}	Data Bus Float after READ	0	100	0	85	ns	
t_{CL}	READ/WRITE Control to Latch Enable	20		10		ns	
t_{CC}	READ/WRITE Control Width	250		200		ns	
t_{DW}	Data in to Write Set Up Time	150		150		ns	
t_{WD}	Data in Hold Time After WRITE	10		10		ns	
t_{WP}	WRITE to Port Output		400		400	ns	
t_{PR}	Port Input Set Up Time	50		50		ns	
t_{RP}	Port Input Hold Time	50		50		ns	
t_{RYH}	READY HOLD Time	0	160	0	160	ns	
t_{ARY}	ADDRESS (CE) to READY		160		160	ns	
t_{RV}	Recovery Time Between Controls	300		200		ns	
t_{RDE}	READ Control to Data Bus Enable	10		10		ns	

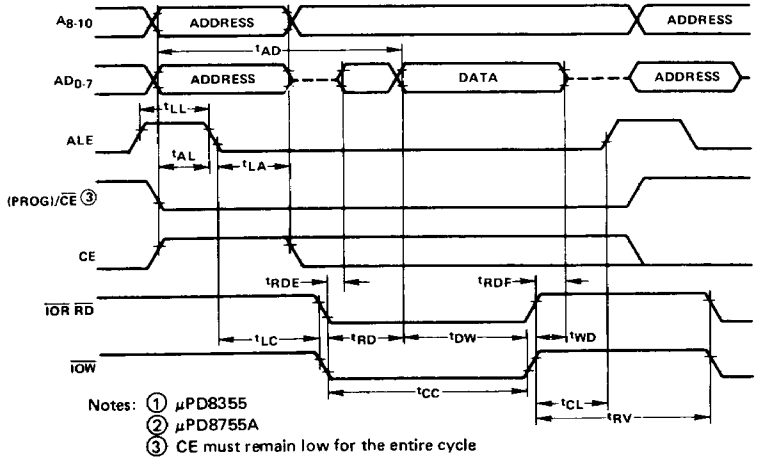
Notes: 30 ns for μPD8755A
C_{LOAD} = 150 pF

TIMING WAVEFORMS

ROM READ, I/O READ AND WRITE ①



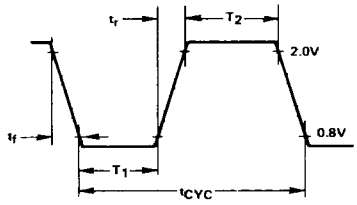
PROM READ, I/O READ AND WRITE ②



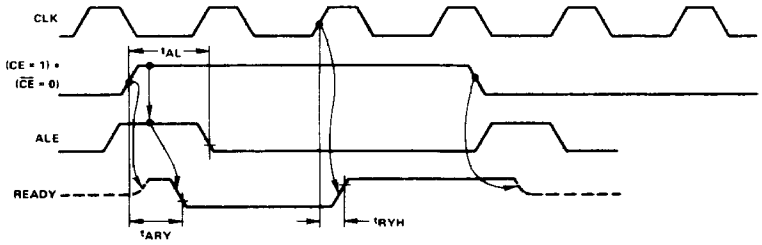
Notes: ① μPD8355
② μPD8755A
③ CE must remain low for the entire cycle

TIMING WAVEFORMS (CONT.)

CLOCK

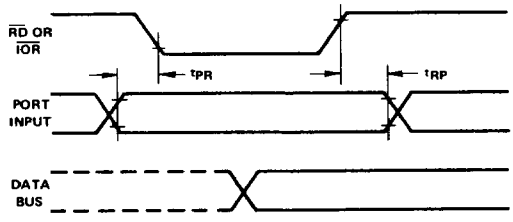


WAIT STATE TIMING (READY = 0)

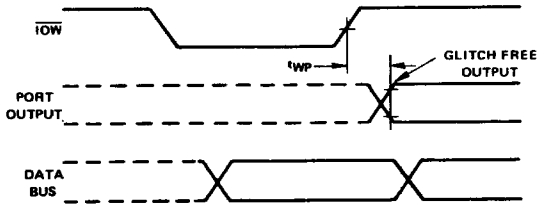


I/O PORT

INPUT MODE:



OUTPUT MODE:



EPROM PROGRAMMING μPD8755A

Erasure of the μPD8755A occurs when exposed to ultraviolet light sources of wavelengths less than 4000 Å. It is recommended, if the device is exposed to room fluorescent lighting or direct sunlight, that opaque labels be placed over the window to prevent exposure. To erase, expose the device to ultraviolet light at 2537 Å at a minimum of 15 W-sec/cm^2 (intensity X expose time). After erasure, all bits are in the logic 1 state. Logic 0's must be selectively programmed into the desired locations. It is recommended that NEC's PROM programmer be used for this application.

Package Outlines

For information, see Package Outline Section 7.

Plastic, μPD8355HC/8755AC
Ceramic, μPD8355D
Ceramic, μPD8355HD
Ceramic, μPD8755AD
Cerdip, μPD8755AD, has quartz window