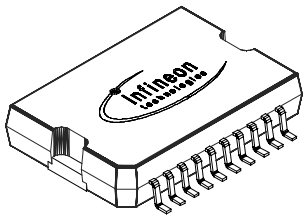
H-Bridge for DC-Motor Applications **TLE 5209 GP**

Data Sheet

Version 1.0

1 Overview



P-DSO-20-12

1.1 Features

- Delivers up to 5 A continuous
- Current limit at max 7.5 A
- Optimized for DC motor management applications
- Operates at supply voltages from 5.2 V up to 40 V
- Very low $R_{DS\ ON}$; typ. 280 mΩ @ 25 °C per switch
- Output full short circuit protected
- Overtemperature protection with hysteresis
- Short circuit and open load diagnosis
- Undervoltage lockout
- CMOS/TTL compatible inputs with hysteresis
- Internal freewheeling diodes
- Wide temperature range; – 40 °C < T_j < 150 °C

Description

The TLE 5209 GP is an integrated power H-bridge with DMOS output stages for driving DC-Motors and Torque-motors. The part is built using the Infineon multi-technology process SPT® which allows bipolar and CMOS control circuitry plus DMOS power MOS-FETs on the same monolithic structure. Operation modes forward (cw), reverse (ccw) and brake are invoked from the two control pins DIR and PWM with TTL/CMOS compatible levels.

A diagnostic logic recognizes three failures at the output stage: overcurrent, open load and overtemperature. These failures are shown at the two diagnostic outputs STATUS1 (non latched) and STATUS2 (latched).

The combination of an extremely low $R_{DS\ ON}$ and the use of a power IC package with low thermal resistance leads to high permissible output currents. The DIR/PWM input interface minimises the effort of control signal generation and the integrated functionality reduces the external circuitry to a minimum.

Type	Ordering Code	Package
TLE 5209 GP	Q67007-A9347	P-DSO-20-12

1.2 Pin Configuration

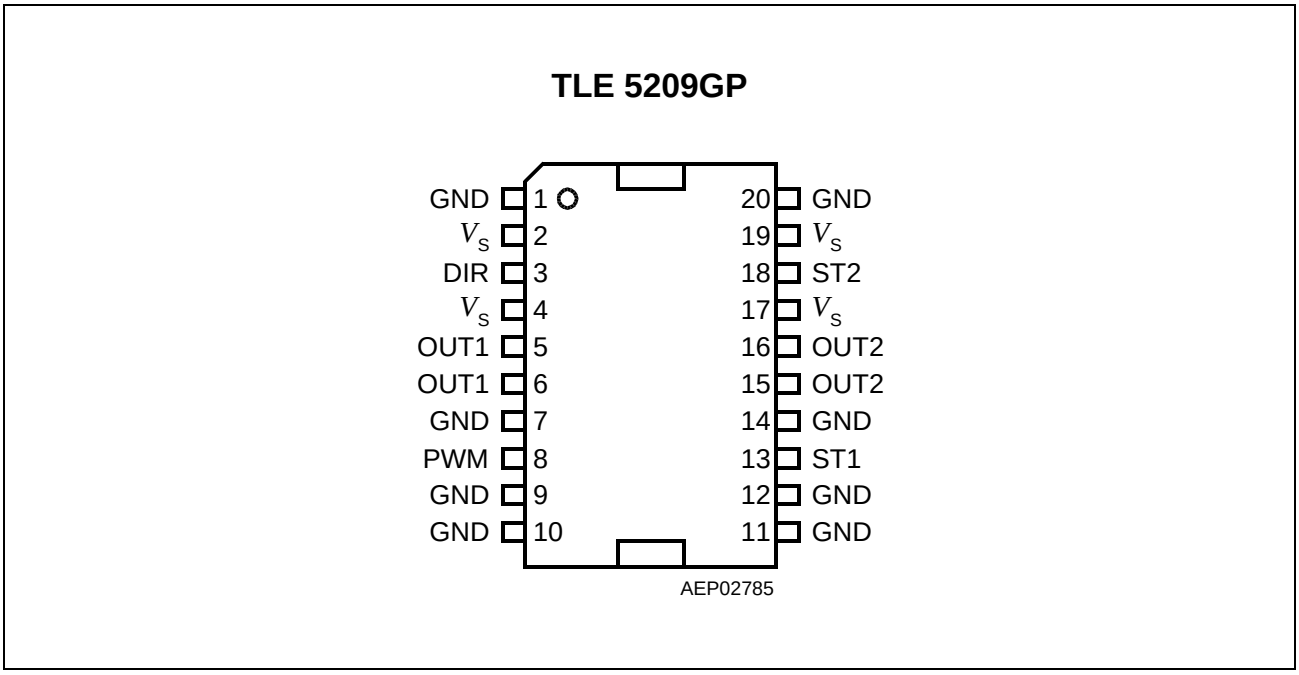


Figure 1 Pin Configuration (top view)

1.3 Pin Definitions and Functions

Pin No.	Symbol	Function
1, 9, 10, 11, 12, 20	GND	**Ground;** internally connected to cooling tab; pins have to be connected to each other externally;
2, 4, 17, 19	V_S	**Supply voltage;** needs a blocking capacitor to GND; pins have to be connected to each other externally
3	DIR	**Direction input;** TTL/CMOS compatible input.
5, 6	OUT1	**Output of Halfbridge 1;** pins have to be connected to each other externally.
8	PWM	**Pulse Width Modulation input;** TTL/CMOS compatible input
13	ST1	**Status flag output 1;** open drain output, requires external pull-up; not latched.
15; 16	OUT2	**Output of Halfbridge 2;** pins have to be connected to each other externally.
18	ST2	**Status flag output 1;** open drain output with internal pull-up; latched, reset if DIR or PWM is toggled.

1.4 Functional Block Diagram

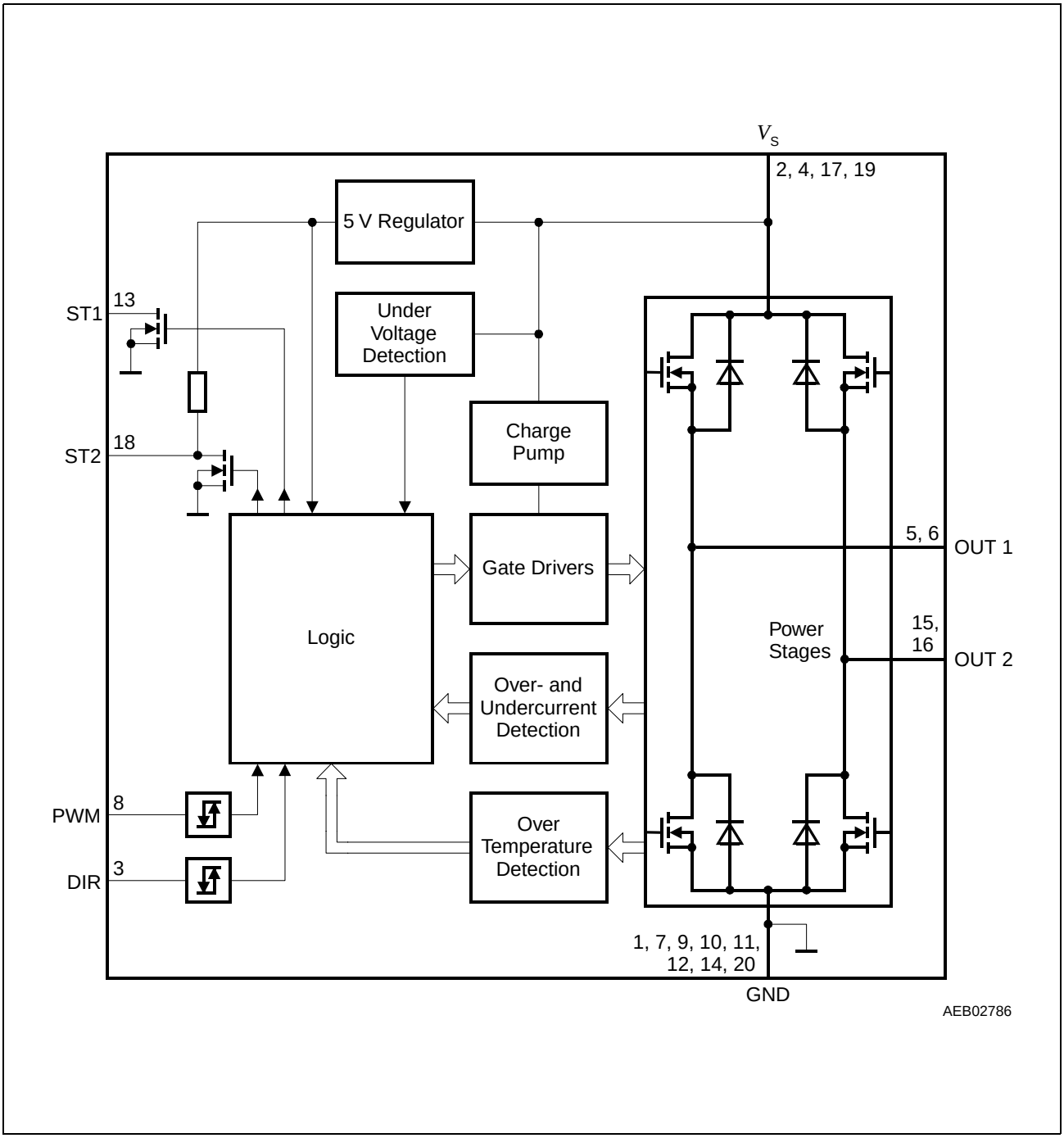


Figure 2 Block Diagram

2 Circuit Description

2.1 Input Circuit

The control inputs DIR and PWM consist of TTL/CMOS-compatible schmitt-triggers with hysteresis. Buffer amplifiers are driven by this stages. Operation modes forward (CW), reverse (CCW) and brake are invoked by these two inputs. If the inputs are not connected, then the load between OUT1 and OUT2 is braked. (both highside switches ON). There's no need for synchronization of the input signals DIR and PWM.

2.2 Output Stages

The output stages consist of a DMOS H-bridge built by two highside switches and two lowside switches. Integrated circuits protect the outputs against overcurrent and overtemperature if there is a short-circuit to ground (SCG) or to the supply voltage (SCB) or short of the load (SCL).

Positive and negative voltage spikes, which occur when switching inductive loads, are limited by integrated freewheeling diodes. A monitoring circuit for each output transistor detects whether the particular transistor is active and in this case prevents the corresponding source transistor (sink transistor) from conducting in sink operation (source operation). Therefore no crossover currents can occur.

2.3 Input Logic Truth Table

Table 1 Functional Truth Table

DIR	PWM	OUT1	OUT2	Comments
L	L	H	H	Brake; both highside transistors switched ON.
L	H	H	L	Motor turns clockwise.
H	L	H	H	Brake; both highside transistors are turned ON.
H	H	L	H	Motor turns counterclockwise.

Table 2 Notes for Output Stage

Symbol	Value
L	Low side transistor is turned-ON. High side transistor is turned-OFF.
H	High side transistor is turned-ON. Low side transistor is turned-OFF.

2.4 Monitoring Functions

Undervoltage lockout (UVLO):
When V_S reaches the switch on voltage $V_{UV\ ON}$ the IC becomes active with a hysteresis. All output transistors are switched off if the supply voltage V_S drops below the switch off voltage $V_{UV\ OFF.}$

2.5 Protective and Diagnostic Functions

The device is fully protected against all kinds of shorts at the outputs and overtemperature and also detects open load.

a) **Output Shorted to Ground Detection**
If a high side transistor is switched on and the output current rises above the shutdown threshold I_{CS} for longer than the delay time t_{dCS}, all output transistors are switched OFF and the Status outputs are set.

b) **Output Shorted to + V_S**
If a low side transistor is switched on and the output current rises above the shutdown threshold I_{CS} for longer than the delay time t_{dCS}, all output transistors are switched OFF and the Status outputs are set.

c) **Overload Detection**
If a low side transistor and a hide side transistor is switched on and the current through the load rises above the shutdown threshold I_{CS} for longer than the delay time t_{dCS}, all output transistors are switched OFF and the Status outputs are set.

The diagnostic behaviour at short circuit is shown schematically in **Figure 4**.

d) **Overtemperature protection**
At a junction temperature higher than T_{OFF} the thermal shutdown turns OFF all four output stages commonly and the Status outputs are set.

e) **Open Load Detection**
If the current through the low side transistor is lower than the reference current I_{dOL} in the ON-state, a timer is started. After a filter time t_{dOL} an open load failure will be recognized and the Status outputs are set. If the current exceeds the reference current I_{dOL} the open load timer is reset. If the H-bridge is switched to OFF-state (PWM = L) during the open load filter time, the timer is stopped. The timer continues if the H-bridge is switched in ON-state again. There is no reset of the open load timer if the direction is changed using the DIR input in open load condition. This is shown schematically in **Figure 3**.

2.6 Diagnosis Truth Table

Various errors as listed in the table “Diagnosis” are detected. Short circuits and overload result in turning off the output stages after a delay. ST1 is active as long as the error exists, but at least 10 µs. ST2 provides a latched output, this means if a fault occurs it is active until at least one of the inputs DIR or PWM are toggled.

Table 3

Flag	DIR	PWM	OUT1	OUT2	ST1	ST2	Remark	No.
Normal operation	0	0	H	H	1	1	–	1
	0	1	H	L	1	1		2
	1	0	H	H	1	1		3
	1	1	L	H	1	1		4
Open circuit between OUT1 and OUT2	0	0	H	H	1	1	Not detectable	5
	0	1	H	L	0	0	Detected	6
	1	0	H	H	1	1	Not detectable	7
	1	1	L	H	0	0	Detected	8
Short circuit of OUT1 to OUT2	0	0	H	H	1	1	Not detectable	9
	0	1	Z	Z	0	0	Detected	10
	1	0	H	H	1	1	Not detectable	11
	1	1	Z	Z	0	0	Detected	12
Short circuit of OUT1 to GND	0	0	Z	Z	0	0	Detected	13
	0	1	Z	Z	0	0	Detected	14
	1	0	Z	Z	0	0	Detected	15
	1	1	L	H	1	1	Not detectable	16
Short circuit of OUT2 to GND	0	0	Z	Z	0	0	Detected	17
	0	1	H	L	1	1	Not detectable	18
	1	0	Z	Z	0	0	Detected	19
	1	1	Z	Z	0	0	Detected	20
Short circuit of OUT1 to V_S	0	0	H	H	1	1	Not detectable	21
	0	1	H	L	1	1	Not detectable	22
	1	0	H	H	1	1	Not detectable	23
	1	1	Z	Z	0	0	Detected	24
Short circuit of OUT2 to V_S	0	0	H	H	1	1	Not detectable	25
	0	1	Z	Z	0	0	Detected	26
	1	0	H	H	1	1	Not detectable	27
	1	1	L	H	1	1	Not detectable	28
Overtempera-ture or undervoltage	0	0	Z	Z	0	0	Detected	29
	0	1	Z	Z	0	0	Detected	30
	1	0	Z	Z	0	0	Detected	31
	1	1	Z	Z	0	0	Detected	32

IN:
0 = Logic LOW
1 = Logic HIGH

OUT:
Z = Both output transistors OFF
L = Low-side transistor ON
H = High-side transistor ON

Status:
1 = high, no error
0 = low, error

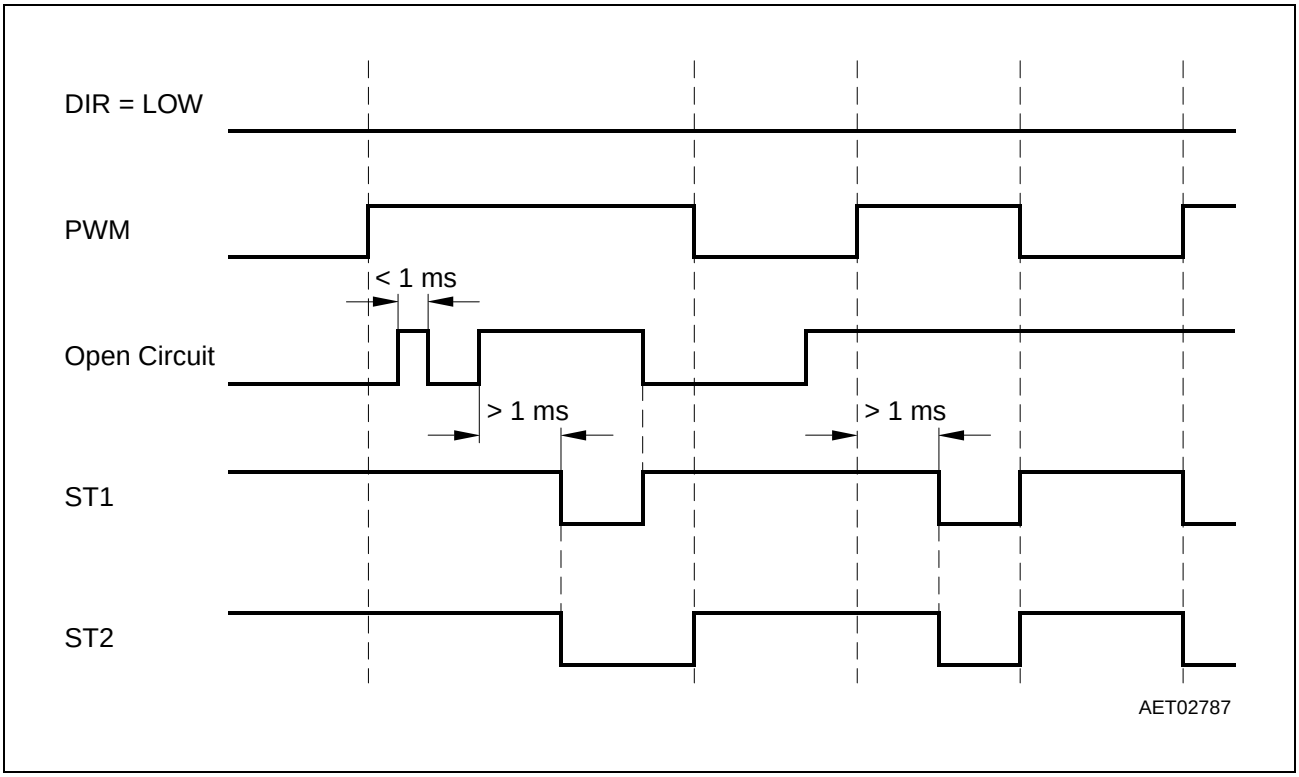


Figure 3 Open Load Diagnosis

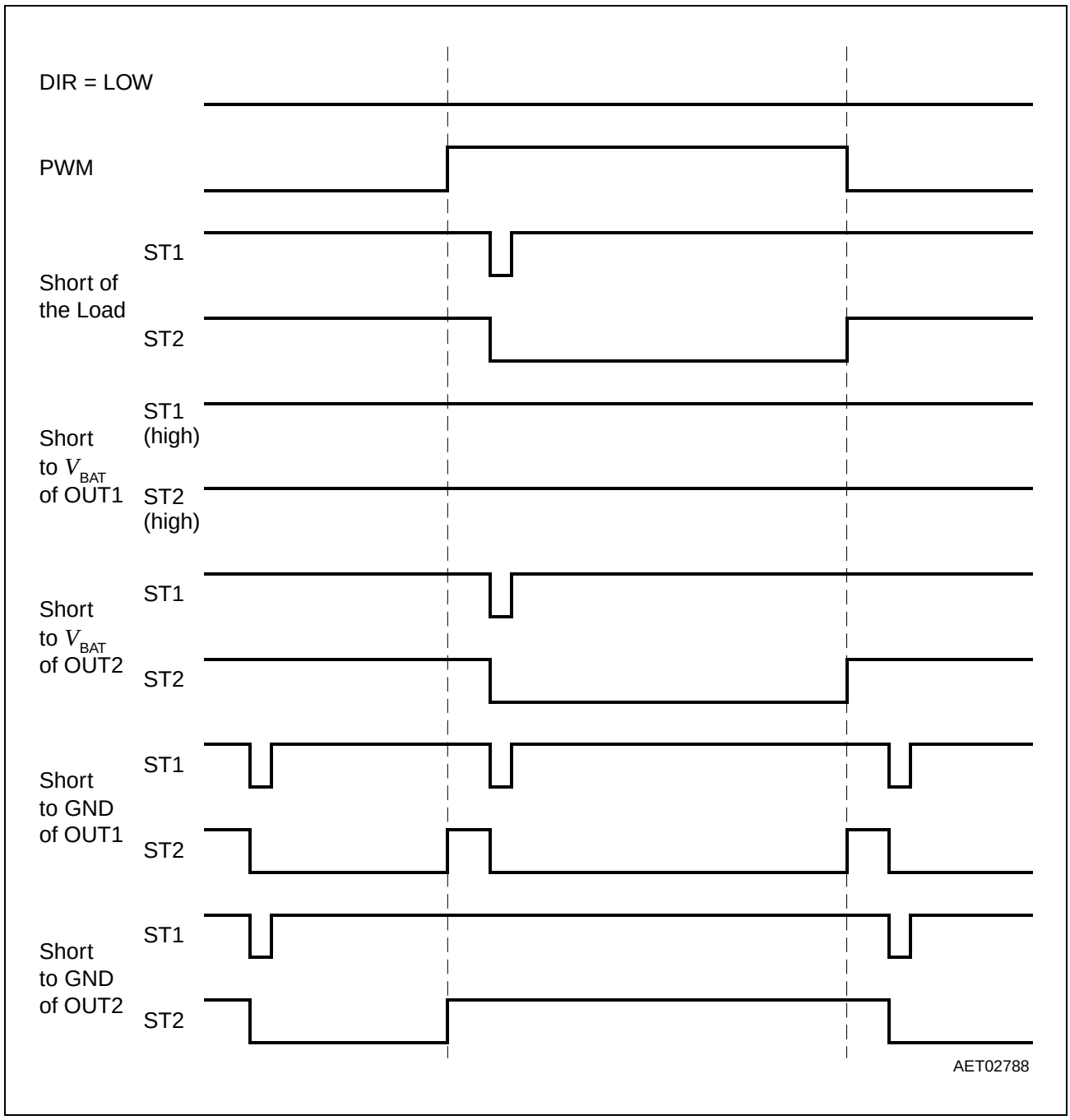


Figure 4 Short Circuit Diagnosis

3 Characteristics

3.1 Absolute Maximum Ratings

– 40 °C < T_j < 150 °C

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Voltages					
Supply voltage	V_S	– 0.3	40	V	–
		– 1	40	V	t < 0.5 s; I_S > – 5 A
Logic input voltage	V_{DIR}, V_{PWM}	– 0.3	7	V	0 V < V_S < 40 V
Diagnostics output voltage	$V_{ST1, 2}$	– 0.3	7	V	–
Currents of DMOS-Transistors and Freewheeling Diodes					
Output current (cont.)	$I_{OUT1, 2}$	– 5	5	A	–
Output current (peak)	$I_{OUT1, 2}$	–10	10	A	t < 2 ms
Temperatures					
Junction temperature	T_j	– 40	150	°C	–
Storage temperature	T_{stg}	– 50	150	°C	–
Thermal Resistances					
Junction case	R_{thjC}	–	4	K/W	–
Junction ambient	R_{thjA}	–	65	K/W	–

Note: Maximum ratings are absolute ratings; exceeding any one of these values may cause irreversible damage to the integrated circuit.

3.2 Operating Range

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply voltage	V_S	$V_{UV\ OFF}$	40	V	After V_S rising above $V_{UV\ ON}$
Supply voltage increasing		– 0.3	$V_{UV\ ON}$	V	Outputs in tristate condition
Supply voltage decreasing		– 0.3	$V_{UV\ OFF}$	V	
Logic input voltage	V_{DIR}, V_{PWM}	– 0.3	7	V	–
Status1 input current	I_{ST1}	–	500	µA	Status active
Junction temperature	T_j	– 40	150	°C	–
Input frequency (PWM, DIR)	f_{IN}	–	1000	Hz	–

Note: The following restrictions for the operation frequency and the duty cycle have to be considered:

a) switching power dissipation
b) diagnostic filter time
c) switching characteristics

3.3 Electrical Characteristics

6 V < V_S < 18 V; $I_{OUT1,2}$ = 0 A (No load); – 40 °C < T_j < 150 °C; unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Outputs OUT1, 2 **Static Drain-Source-On Resistance**						
High-side transistor I_{OUT} = – 1 A; 5.2V < V_S < 6 V	$R_{DS\ ON\ H}$	–	280	600	mΩ	T_j = 25 °C
		–	–	870	mΩ	–
High-side transistor I_{OUT} = – 3 A; 6 V < V_S < 9 V	$R_{DS\ ON\ H}$	–	260	430	mΩ	T_j = 25 °C
		–	–	640	mΩ	–
High-side transistor I_{OUT} = – 3 A; 9 V < V_S < 24 V	$R_{DS\ ON\ H}$	–	250	340	mΩ	T_j = 25 °C
		–	–	560	mΩ	–
Low-side transistor I_{OUT} = 1 A; 5.2V < V_S < 6 V	$R_{DS\ ON\ L}$	–	280	550	mΩ	T_j = 25 °C
		–	–	850	mΩ	–
Low-side transistor I_{OUT} = 3 A; 6 V < V_S < 9 V	$R_{DS\ ON\ L}$	–	260	380	mΩ	T_j = 25 °C
		–	–	620	mΩ	–
Low-side transistor I_{OUT} = 3 A; 9 V < V_S < 24 V	$R_{DS\ ON\ L}$	–	250	340	mΩ	T_j = 25 °C
		–	–	560	mΩ	–
Short Circuit Protection						
Shutdown current threshold 5.2 V< V_S < 6V	I_{CS5}	4.5	–	7.5	A	$t < t_{dCS}$
Shutdown current threshold 6 < V_S < 9 V	I_{CS6}	4.8	–	7.5	A	$t < t_{dCS}$
Shutdown current threshold 9 < V_S < 24 V	I_{CS9}	5.0	–	7.5	A	$t < t_{dCS}$
Delaytime for overcurrent shutdown	t_{dCS}	5	18	28	µs	–

3.3 Electrical Characteristics (cont'd)

6 V < V_S < 18 V; $I_{OUT1,2}$ = 0 A (No load); – 40 °C < T_j < 150 °C; unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Logic						
Control Inputs DIR, PWM; $V_{IN} = V_{DIR}, V_{PWM}$; $I_{IN} = I_{DIR}, I_{PWM}$						
H-input voltage threshold	V_{INH}	–	–	3.5	V	V_{IN} rising
L-input voltage threshold	V_{INL}	1.0	–	–	V	V_{IN} falling
Hysteresis of input voltage	V_{INHY}	0.3	1	–	V	–
H-input current	I_{INH}	20	–	100	µA	V_{IN} = 3.5 V
L-input current	I_{INL}	20	–	100	µA	V_{IN} = 1 V
Status Outputs; $V_{ST} = V_{ST1}, V_{ST2}$; $I_{ST} = I_{ST1}, I_{ST2}$						
ST1, ST2 Low output voltage	V_{STL}	–	–	0.4	V	I_{ST} = 100 µA
ST2 High output voltage	V_{ST2H}	3.9	–	5.4	V	I_{ST2} = – 20 µA
ST1 Output Leakage current	$I_{ST1(OFF)}$	–	–	5	µA	V_{ST1} = 5 V
Open Load Detection						
Detection current	I_{dOL}	10	40	100	mA	5.2 V < V_S <18 V
Filter time	t_{dOL}	1	5	10	ms	
Under Voltage Lockout						
UV-Switch-ON voltage	$V_{UV\ ON}$	4.5	–	5.2	V	V_S increasing
UV-Switch-OFF voltage	$V_{UV\ OFF}$	4.0	–	5.1	V	V_S decreasing
UV-ON/OFF-Hysteresis	$V_{UV\ HY}$	–	0.15	–	V	$V_{UV\ ON} - V_{UV\ OFF}$
Current Consumption						
Supply current	I_S	–	4	20	mA	PWM = high

3.3 Electrical Characteristics (cont'd)

6 V < V_S < 18 V; $I_{OUT1,2}$ = 0 A (No load); – 40 °C < T_j < 150 °C; unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Output Timing (device active for *t* > 100 µs)						
Output low-to-high switching time	$t_{ON\,H}$	–	–	100	µs	resistive load of 12 Ω; V_S = 13 V; PWM H -> L
Output high-to-low switching time	$t_{ON\,L}$	–	–	100	µs	resistive load of 12 Ω; V_S = 13 V; PWM L -> H
Slew rate rising; 30% - 80%	$(dV/dt)_R$	0.8	–	6	V/µs	resistive load of 12 Ω; V_S = 13 V
Slew rate falling; 30% - 80%	$(dV/dt)_F$	0.8	–	6	V/µs	resistive load of 12 Ω; V_S = 13 V
Setup time after power up on V_S	t_{ds}	–	–	100	µs	–

Note: Setup time is guaranteed by design.

3.3 Electrical Characteristics (cont'd)

6 V < V_S < 18 V; $I_{OUT1,2}$ = 0 A (No load); – 40 °C < T_j < 150 °C; unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Clamp Diodes **Forward Voltage**						
High-side transistor	V_{FH}	–	–	2	V	I_{FH} = 5 A
Low-side transistor	V_{FL}	–	–	2	V	I_{FL} = 5 A
Leakage Current (all Output Transistors OFF)						
High-side transistor	I_{LKH}	– 200	–	–	µA	V_{OUT} = 0; V_S = 14 V
Low-side transistor	I_{LKL}	–	–	200	µA	V_{OUT} = V_S = 14 V
Thermal Shutdown						
Thermal shutdown junction temperature	T_{jSD}	150	–	200	°C	–
Thermal switch-on junction temperature	T_{jSO}	120	–	170	°C	–
Temperature hysteresis	ΔT	–	30	–	K	–

Note: Temperatures are guaranteed by design.

4 Diagrams

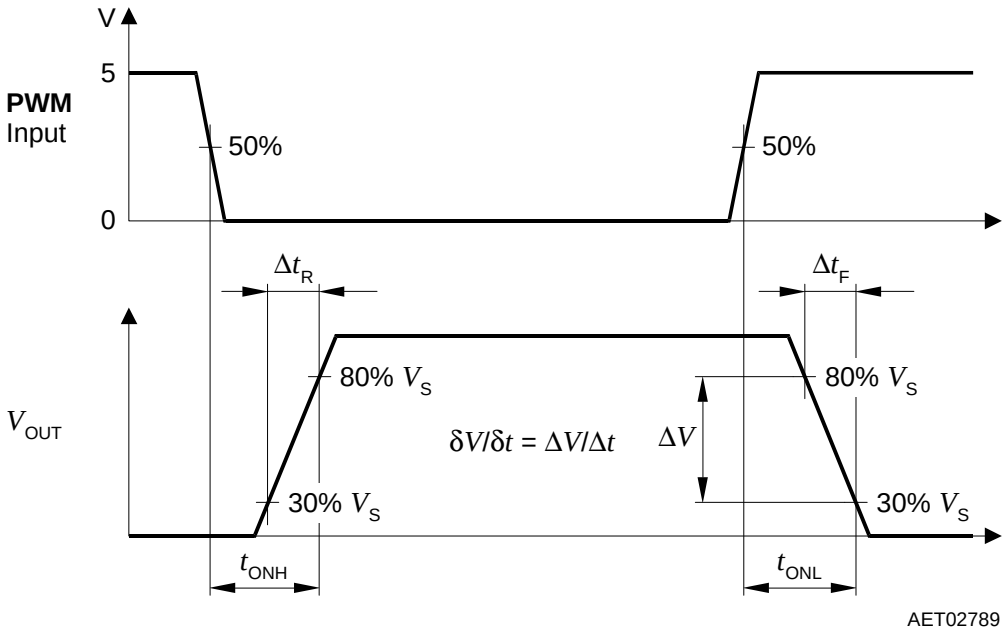


Figure 5 Switching Time Definitions

DIR	high	low
V_{OUT} =	V_{OUT1}	V_{OUT2}

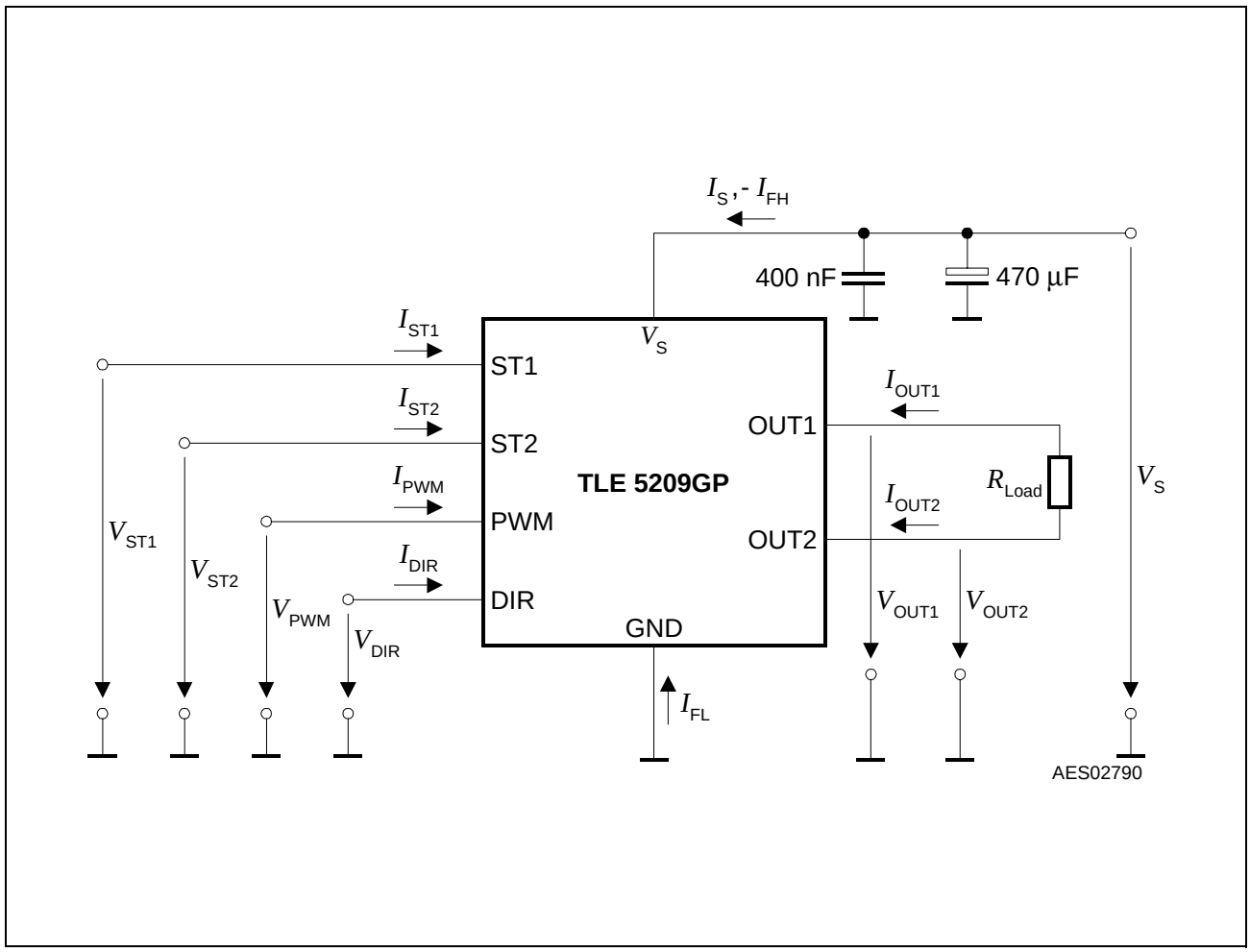


Figure 6 Test Circuit

	Overcurrent high-side, short to GND	Overcurrent low-side, short to Vs	Open Load
I_{OUT}	$-I_{CS}$	I_{CS}	I_{dOL}

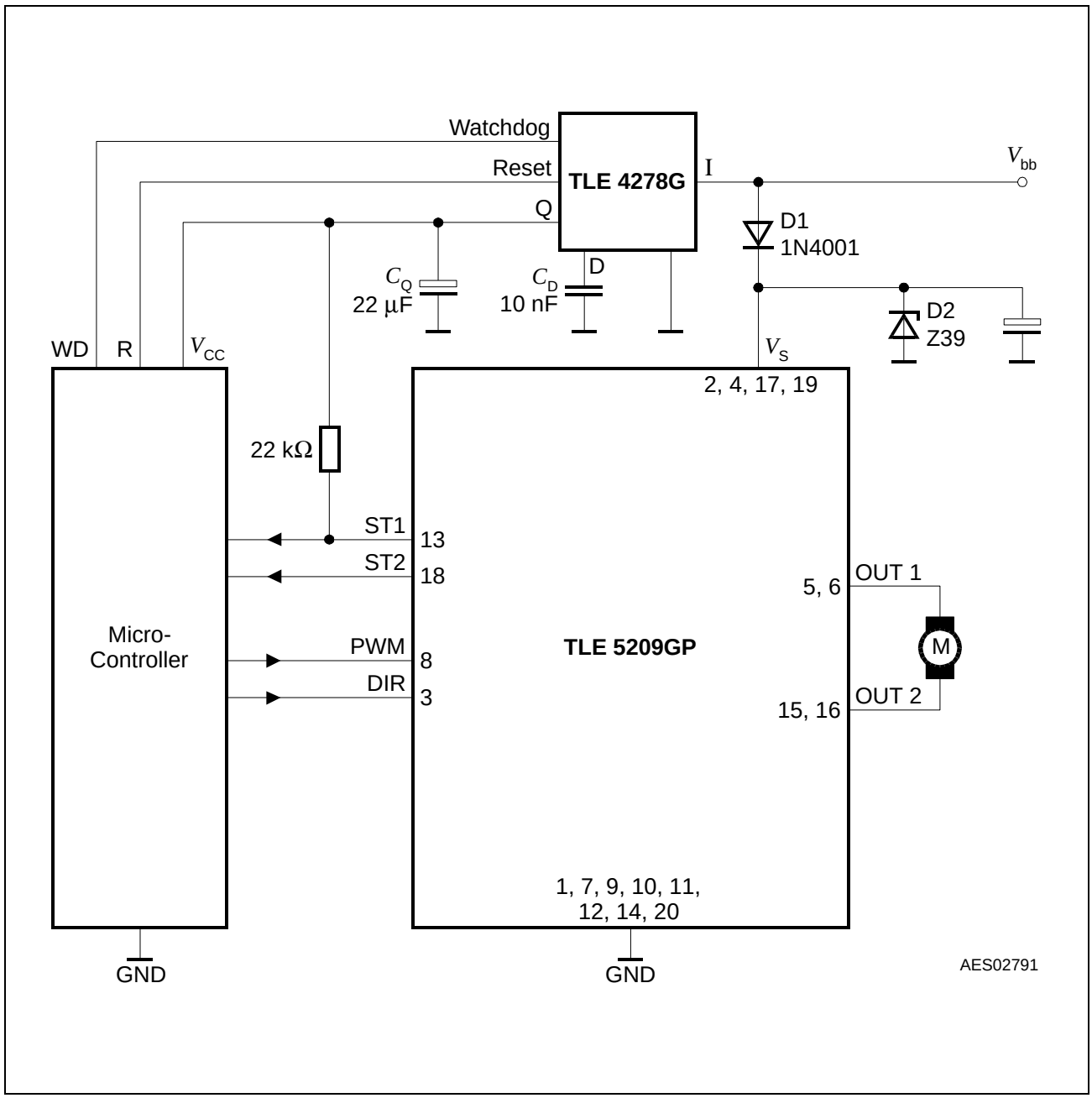
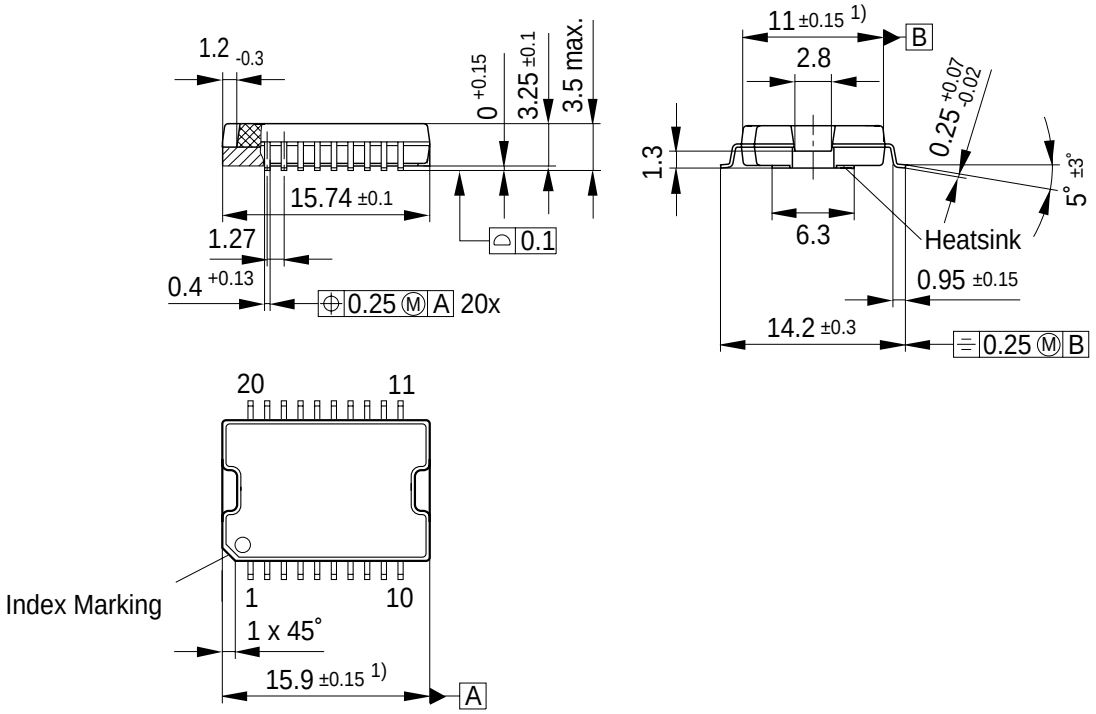


Figure 7 Application Circuit

5 Package Outlines

P-DSO-20-12
(Plastic Dual Small Outline Package)



1) Does not include plastic or metal protrusion of 0.15 max. per side

GPS05791

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm