

Document Title

256Kx36 & 512Kx18-Bit Synchronous Pipelined Burst SRAM

Revision History

<u>Rev. No.</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>
0.0	Initial draft	April. 10 . 1998	Preliminary
0.1	Modify DC characteristics(Input Leakage Current test Conditions) form V _{DD} =V _{SS} to V _{DD} to Max.	June .08. 1998	Preliminary
0.2	Change DC Characteristics. I _{SB} value from 80mA to 130mA at -60 I _{SB} value from 70mA to 120mA at -67 I _{SB} value from 65mA to 110mA at -72 I _{SB} value from 50mA to 100mA at -10 I _{SB1} value from 10mA to 30mA I _{SB2} value from 10mA to 30mA	Aug . 27. 1998	Preliminary

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256Kx36 & 512Kx18-Bit Synchronous Pipelined Burst SRAM

FEATURES

- Synchronous Operation.
- 2 Stage Pipelined operation with 4 Burst.
- On-Chip Address Counter.
- Self-Timed Write Cycle.
- On-Chip Address and Control Registers.
- $V_{DD} = 3.3V \pm 5\%$ Power Supply.
- 5V Tolerant Inputs Except I/O Pins.
- Byte Writable Function.
- Global Write Enable Controls a full bus-width write.
- Power Down State via ZZ Signal.
- LBO Pin allows a choice of either a interleaved burst or a linear burst.
- Three Chip Enables for simple depth expansion with No Data Contention only for TQFP ; 2cycle Enable, 1cycle Disable.
- Asynchronous Output Enable Control.
- ADSP, ADSC, ADV Burst Control Pins.
- TTL-Level Three-State Output.
- 100-TQFP-1420A / 119BGA(7x17 Ball Grid Array Package)

GENERAL DESCRIPTION

The KM736V889 and KM718V989 are 9,437,184-bit Synchronous Static Random Access Memory designed for high performance second level cache of Pentium and Power PC based System.

It is organized as 256K(512K) words of 36(18) bits and integrates address and control registers, a 2-bit burst address counter and added some new functions for high performance cache RAM applications; \overline{GW} , \overline{BW} , \overline{LBO} , \overline{ZZ} . Write cycles are internally self-timed and synchronous.

Full bus-width write is done by \overline{GW} , and each byte write is performed by the combination of \overline{WEx} and \overline{BW} when \overline{GW} is high. And with $\overline{CS1}$ high, \overline{ADSP} is blocked to control signals.

Burst cycle can be initiated with either the address status processor(\overline{ADSP}) or address status cache controller(\overline{ADSC}) inputs. Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance(\overline{ADV}) input.

\overline{LBO} pin is DC operated and determines burst sequence(linear or interleaved).

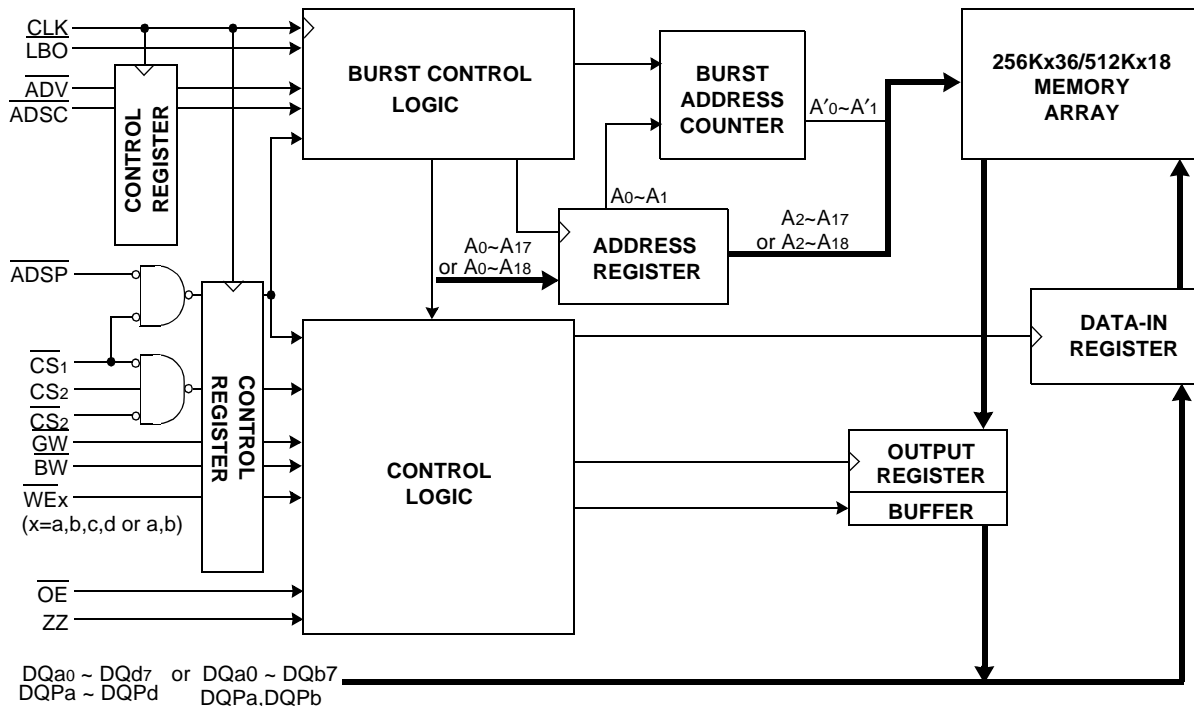
\overline{ZZ} pin controls Power Down State and reduces Stand-by current regardless of CLK.

The KM736V889 and KM718V989 are fabricated using SAMSUNG's high performance CMOS technology and is available in a 100pin TQFP and 119BGA package. Multiple power and ground pins are utilized to minimize ground bounce.

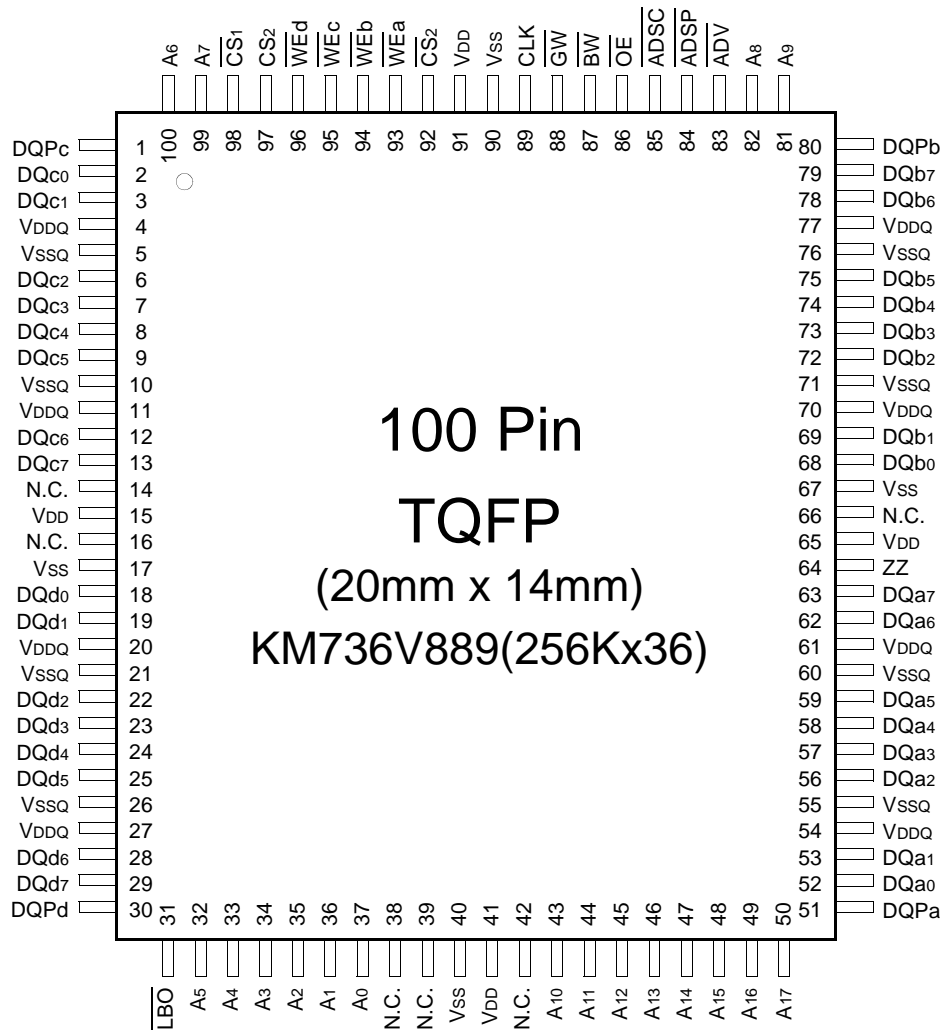
FAST ACCESS TIMES

Parameter	Symbol	-60	-67	-72	-10	Unit
Cycle Time	tcyc	6.0	6.7	7.2	10	ns
Clock Access Time	tcd	3.5	3.8	4.0	4.5	ns
Output Enable Access Time	toe	3.5	3.8	4.0	4.5	ns

LOGIC BLOCK DIAGRAM



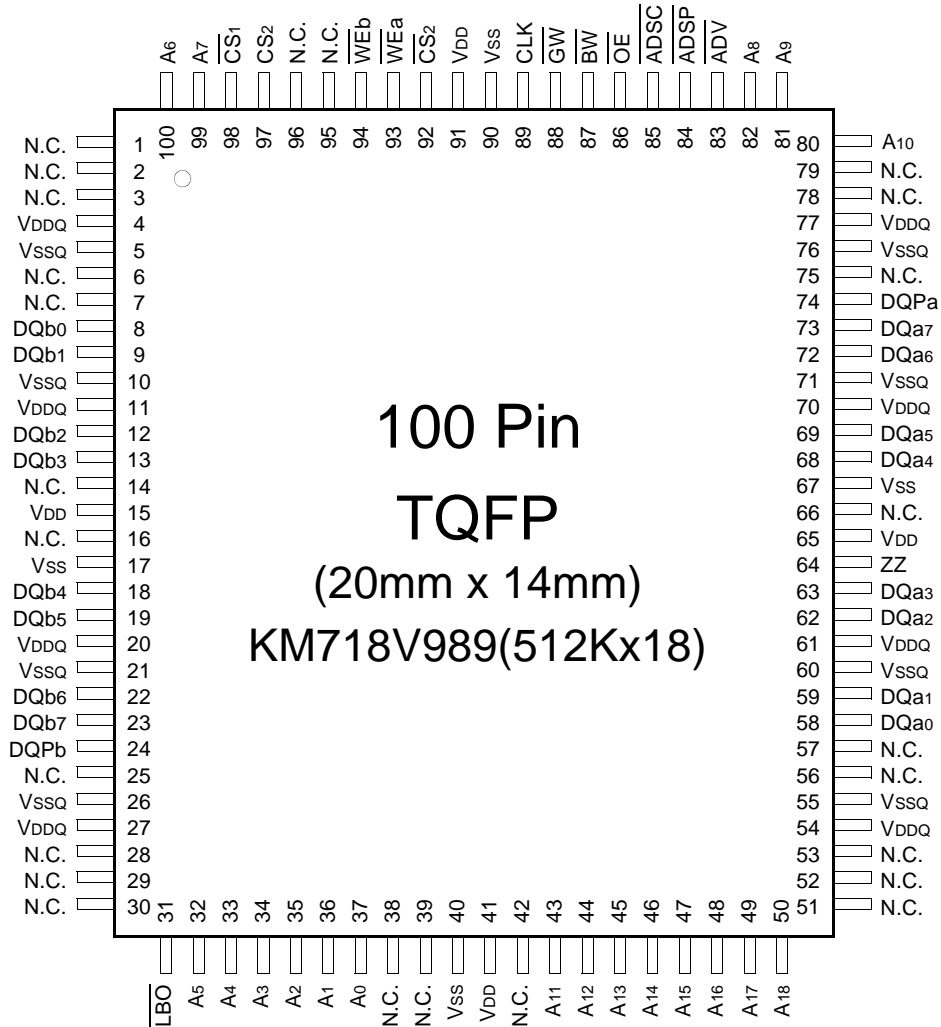
PIN CONFIGURATION(TOP VIEW)



PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A0 - A17	Address Inputs	32,33,34,35,36,37,43 44,45,46,47,48,49,50 81,82,99,100	VDD	Power Supply(+3.3V)	15,41,65,91
			VSS	Ground	17,40,67,90
			N.C.	No Connect	14,16,38,39,42,66
ADV	Burst Address Advance	83	DQa0~a7	Data Inputs/Outputs	52,53,56,57,58,59,62,63
ADSP	Address Status Processor	84	DQb0~b7		68,69,72,73,74,75,78,79
ADSC	Address Status Controller	85	DQc0~c7		2,3,6,7,8,9,12,13
CLK	Clock	89	DQd0~d7		18,19,22,23,24,25,28,29
CS1	Chip Select	98	DQP a~P d		51,80,1,30
CS2	Chip Select	97	VDDQ	Output Power Supply (+3.3V)	4,11,20,27,54,61,70,77
CS2	Chip Select	92	VSSQ	Output Ground	5,10,21,26,55,60,71,76
WEx(x=a,b,c,d)	Byte Write Inputs	93,94,95,96			
OE	Output Enable	86			
GW	Global Write Enable	88			
BW	Byte Write Enable	87			
ZZ	Power Down Input	64			
LBO	Burst Mode Control	31			

PIN CONFIGURATION(TOP VIEW)



PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A0 - A18	Address Inputs	32,33,34,35,36,37,43 44,45,46,47,48,49,50 80,81,82,99,100	VDD	Power Supply(+3.3V)	15,41,65,91
			VSS	Ground	17,40,67,90
			N.C.	No Connect	1,2,3,6,7,14,16,25,28,29, 30,38,39,42,51,52,53,56, 57,66,75,78,79,95,96
ADV	Burst Address Advance	83			
ADSP	Address Status Processor	84	DQa0 ~ a7	Data Inputs/Outputs	58,59,62,63,68,69,72,73
ADSC	Address Status Controller	85	DQb0 ~ b7		8,9,12,13,18,19,22,23
CLK	Clock	89	DQPa, Pb		74,24
CS1	Chip Select	98	VDDQ	Output Power Supply (+3.3V)	4,11,20,27,54,61,70,77
CS2	Chip Select	97	VSSQ	Output Ground	5,10,21,26,55,60,71,76
CS2	Chip Select	92			
WEx	Byte Write Inputs	93,94			
OE	Output Enable	86			
GW	Global Write Enable	88			
BW	Byte Write Enable	87			
ZZ	Power Down Input	64			
LBO	Burst Mode Control	31			

119BGA PACKAGE PIN CONFIGURATIONS(TOP VIEW)

KM736V889(256Kx36)

	1	2	3	4	5	6	7
A	VDDQ	A13	A10	$\overline{\text{ADSP}}$	A7	A4	VDDQ
B	NC	CS2	A9	$\overline{\text{ADSC}}$	A8	A17	NC
C	NC	A12	A11	VDD	A6	A5	NC
D	DQC7	DQPc	VSS	NC	VSS	DQPb	DQb7
E	DQc5	DQc6	VSS	$\overline{\text{CS1}}$	VSS	DQb6	DQb5
F	VDDQ	DQC4	VSS	$\overline{\text{OE}}$	VSS	DQb4	VDDQ
G	DQC2	DQC3	$\overline{\text{WEc}}$	$\overline{\text{ADV}}$	$\overline{\text{WEb}}$	DQb3	DQb2
H	DQc0	DQC1	VSS	$\overline{\text{GW}}$	VSS	DQb1	DQb0
J	VDDQ	VDD	NC	VDD	NC	VDD	VDDQ
K	DQd0	DQd1	VSS	CLK	VSS	DQa1	DQa0
L	DQd2	DQd3	$\overline{\text{WEd}}$	NC	$\overline{\text{WEa}}$	DQa3	DQa2
M	VDDQ	DQd4	VSS	$\overline{\text{BW}}$	VSS	DQa4	VDDQ
N	DQd5	DQd6	VSS	A1	VSS	DQa6	DQa5
P	DQd7	DQPd	VSS	A0	VSS	DQPa	DQa7
R	NC	A15	$\overline{\text{LBO}}$	VDD	NC	A2	NC
T	NC	NC	A14	A16	A3	NC	ZZ
U	VDDQ	NC	NC	NC	NC	NC	VDDQ

PIN NAME

SYMBOL	PIN NAME	BGA PIN NO.	SYMBOL	PIN NAME	BGA PIN NO.
A0 - A17	Address Inputs	4P,4N,6R,5T,6A,6C 5C,5A,5B,3B,3A,3C 2C,2A,3T,2R,4T,6B	VDD	Power Supply(+3.3V)	4C,2J,4J,6J,4R
			VSS	Ground	3D,5D,3E,5E,3F,5F,3H,5H 3K,5K,3M,5M,3N,5N,3P,5P
$\overline{\text{ADV}}$	Burst Address Advance	4G	N.C.	No Connect	1B,7B,1C,7C,4D,3J,5J,4L 1R,5R,7R,1T,2T,6T,2U,3U 4U,5U,6U
$\overline{\text{ADSP}}$	Address Status Processor	4A			
ADSC	Address Status Controller	4B			
CLK	Clock	4K	DQa0~a7	Data Inputs/Outputs	7K,6K,7L,6L,6M,6N,7N,7P 7H,6H,7G,6G,6F,7E,6E,7D
$\overline{\text{CS1}}$	Chip Select	4E	DQb0~b7		1H,2H,1G,2G,2F,1E,2E,1D
$\overline{\text{CS2}}$	Chip Selectt	2B	DQC0~c7		1K,2K,1L,2L,2M,1N,2N,1P
WEx	Byte Write Inputs	5L,5G,3G,3L	DQd0~d7		6P,6D,2D,2P
(x=a,b,c,d)			DQPa~Pd	Output Power Supply (+3.3V)	1A,7A,1F,7F,1J,7J,1M,7M 1U,7U
			VDDQ		
$\overline{\text{OE}}$	Output Enable	4F			
$\overline{\text{GW}}$	Global Write Enable	4H			
BW	Byte Write Enable	4M			
ZZ	Power Down Input	7T			
$\overline{\text{LBO}}$	Burst Mode Control	3R			

119BGA PACKAGE PIN CONFIGURATIONS(TOP VIEW)

KM718V989(512Kx18)

	1	2	3	4	5	6	7
A	VDDQ	A13	A10	$\overline{\text{ADSP}}$	A7	A4	VDDQ
B	NC	CS2	A9	$\overline{\text{ADSC}}$	A8	A18	NC
C	NC	A12	A11	VDD	A6	A5	NC
D	DQb0	NC	VSS	NC	VSS	DQPa	NC
E	NC	DQb1	VSS	$\overline{\text{CS1}}$	VSS	NC	DQa7
F	VDDQ	NC	VSS	$\overline{\text{OE}}$	VSS	DQa6	VDDQ
G	NC	DQb2	$\overline{\text{WEb}}$	$\overline{\text{ADV}}$	VSS	NC	DQa5
H	DQb3	NC	VSS	$\overline{\text{GW}}$	VSS	DQa4	NC
J	VDDQ	VDD	NC	VDD	NC	VDD	VDDQ
K	NC	DQb4	VSS	CLK	VSS	NC	DQa3
L	DQb5	NC	VSS	NC	$\overline{\text{WEa}}$	DQa2	NC
M	VDDQ	DQb6	VSS	$\overline{\text{BW}}$	VSS	NC	VDDQ
N	DQb7	NC	VSS	A1	VSS	DQa1	NC
P	NC	DQPb	VSS	A0	VSS	NC	DQa0
R	NC	A15	$\overline{\text{LBO}}$	VDD	NC	A2	NC
T	NC	A17	A14	NC	A3	A16	ZZ
U	VDDQ	NC	NC	NC	NC	NC	VDDQ

PIN NAME

SYMBOL	PIN NAME	BGA PIN NO.	SYMBOL	PIN NAME	BGA PIN NO.
A0 - A18	Address Inputs	4P, 4N, 6R, 5T, 6A, 6C 5C, 5A, 5B, 3B, 3A, 3C 2C, 2A, 3T, 2R, 6B, 6T 2T	VDD	Power Supply(+3.3V)	4C, 2J, 4J, 6J, 4R
			VSS	Ground	3D, 5D, 3E, 5E, 3F, 5F, 5G, 3H 5H, 3K, 5K, 3L, 3M, 5M, 3N, 5N 3P, 5P
$\overline{\text{ADV}}$	Burst Address Advance	4G	N.C.	No Connect	1B, 7B, 1C, 7C, 2D, 4D, 7D, 1E 6E, 2F, 1G, 6G, 2H, 7H, 3J, 5J 1K, 6K, 2L, 4L, 7L, 6M, 2N, 7N 1P, 6P, 1R, 5R, 7R, 1T, 4T, 2U 3U, 4U, 5U, 6U
$\overline{\text{ADSP}}$	Address Status Processor	4A	DQa0~a7	Data Inputs/Outputs	7P, 6N, 6L, 7K, 6H, 7G, 6F, 7E 1D, 2E, 2G, 1H, 2K, 1L, 2M, 1N 6D, 2P
$\overline{\text{ADSC}}$	Address Status Controller	4B	DQb0~b7		
CLK	Clock	4K	DQPa, DQPb		
$\overline{\text{CS1}}$	Chip Select	4E	VDDQ	Output Power Supply (+3.3V)	1A, 7A, 1F, 7F, 1J, 7J, 1M, 7M 1U, 7U
$\overline{\text{CS2}}$	Chip Select	2B			
$\overline{\text{WEx}}$ (x=a,b)	Byte Write Inputs	5L, 3G			
$\overline{\text{OE}}$	Output Enable	4F			
$\overline{\text{GW}}$	Global Write Enable	4H			
$\overline{\text{BW}}$	Byte Write Enable	4M			
$\overline{\text{ZZ}}$	Power Down Input	7T			
$\overline{\text{LBO}}$	Burst Mode Control	3R			

FUNCTION DESCRIPTION

The KM736V889 and KM718V989 are synchronous SRAM designed to support the burst address accessing sequence of the Power PC based microprocessor. All inputs (with the exception of \overline{OE} , \overline{LBO} and \overline{ZZ}) are sampled on rising clock edges. The start and duration of the burst access is controlled by \overline{ADSC} , \overline{ADSP} and \overline{ADV} and chip select pins.

The accesses are enabled with the chip select signals and output enabled signals. Wait states are inserted into the access with \overline{ADV} .

When \overline{ZZ} is pulled high, the SRAM will enter a Power Down State. At this time, internal state of the SRAM is preserved. When \overline{ZZ} returns to low, the SRAM normally operates after 2cycles of wake up time. \overline{ZZ} pin is pulled down internally.

Read cycles are initiated with \overline{ADSP} (regardless of \overline{WEx} and \overline{ADSC})using the new external address clocked into the on-chip address register whenever \overline{ADSP} is sampled low, the chip selects are sampled active, and the output buffer is enabled with \overline{OE} . In read operation the data of cell array accessed by the current address, registered in the Data-out registers by the positive edge of \overline{CLK} , are carried to the Data-out buffer by the next positive edge of \overline{CLK} . The data, registered in the Data-out buffer, are projected to the output pins. \overline{ADV} is ignored on the clock edge that samples \overline{ADSP} asserted, but is sampled on the subsequent clock edges. The address increases internally for the next access of the burst when \overline{WEx} are sampled High and \overline{ADV} is sampled low. And \overline{ADSP} is blocked to control signals by disabling $\overline{CS1}$.

All byte write is done by \overline{GW} (regardless of \overline{BW} and \overline{WEx}), and each byte write is performed by the combination of \overline{BW} and \overline{WEx} when \overline{GW} is high.

Write cycles are performed by disabling the output buffers with \overline{OE} and asserting \overline{WEx} . \overline{WEx} are ignored on the clock edge that samples \overline{ADSP} low, but are sampled on the subsequent clock edges. The output buffers are disabled when \overline{WEx} are sampled Low (regardless of \overline{OE}). Data is clocked into the data input register when \overline{WEx} sampled Low. The address increases internally to the next address of burst, if both \overline{WEx} and \overline{ADV} are sampled Low. Individual byte write cycles are performed by any one or more byte write enable signals(\overline{WEa} , \overline{WEb} , \overline{WEc} or \overline{WEd}) sampled low. The \overline{WEa} control $\overline{DQa0} \sim \overline{DQa7}$ and $\overline{DQP a}$, \overline{WEb} controls $\overline{DQb0} \sim \overline{DQb7}$ and $\overline{DQP b}$, \overline{WEc} controls $\overline{DQc0} \sim \overline{DQc7}$ and $\overline{DQP c}$, and \overline{WEd} control $\overline{DQd0} \sim \overline{DQd7}$ and $\overline{DQP d}$. Read or write cycle may also be initiated with \overline{ADSC} , instead of \overline{ADSP} . The differences between cycles initiated with \overline{ADSC} and \overline{ADSP} as are follows;

\overline{ADSP} must be sampled high when \overline{ADSC} is sampled low to initiate a cycle with \overline{ADSC} .
 \overline{WEx} are sampled on the same clock edge that sampled \overline{ADSC} low (and \overline{ADSP} high).

Addresses are generated for the burst access as shown below, The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the \overline{LBO} pin. When this pin is Low, linear burst sequence is selected. When this pin is High, Interleaved burst sequence is selected.

BURST SEQUENCE TABLE

(Interleaved Burst)

\overline{LBO} PIN	HIGH	Case 1		Case 2		Case 3		Case 4	
		A1	A0	A1	A0	A1	A0	A1	A0
	First Address	0	0	0	1	1	0	1	1
	↓	0	1	0	0	1	1	1	0
	↓	1	0	1	1	0	0	0	1
	Fourth Address	1	1	1	0	0	1	0	0

(Linear Burst)

\overline{LBO} PIN	LOW	Case 1		Case 2		Case 3		Case 4	
		A1	A0	A1	A0	A1	A0	A1	A0
	First Address	0	0	0	1	1	0	1	1
	↓	0	1	1	0	1	1	0	0
	↓	1	0	1	1	0	0	0	1
	Fourth Address	1	1	0	0	0	1	1	0

NOTE : 1. \overline{LBO} pin must be tied to High or Low, and Floating State must not be allowed.

TRUTH TABLES

SYNCHRONOUS TRUTH TABLE

\overline{CS}_1	\overline{CS}_2	\overline{CS}_2	\overline{ADSP}	\overline{ADSC}	\overline{ADV}	\overline{WRITE}	CLK	Address Accessed	Operation
H	X	X	X	L	X	X	↑	N/A	Not Selected
L	L	X	L	X	X	X	↑	N/A	Not Selected
L	X	H	L	X	X	X	↑	N/A	Not Selected
L	L	X	X	L	X	X	↑	N/A	Not Selected
L	X	H	X	L	X	X	↑	N/A	Not Selected
L	H	L	L	X	X	X	↑	External Address	Begin Burst Read Cycle
L	H	L	H	L	X	L	↑	External Address	Begin Burst Write Cycle
L	H	L	H	L	X	H	↑	External Address	Begin Burst Read Cycle
X	X	X	H	H	L	H	↑	Next Address	Continue Burst Read Cycle
H	X	X	X	H	L	H	↑	Next Address	Continue Burst Read Cycle
X	X	X	H	H	L	L	↑	Next Address	Continue Burst Write Cycle
H	X	X	X	H	L	L	↑	Next Address	Continue Burst Write Cycle
X	X	X	H	H	H	H	↑	Current Address	Suspend Burst Read Cycle
H	X	X	X	H	H	H	↑	Current Address	Suspend Burst Read Cycle
X	X	X	H	H	H	L	↑	Current Address	Suspend Burst Write Cycle
H	X	X	X	H	H	L	↑	Current Address	Suspend Burst Write Cycle

- NOTE :** 1. X means "Don't Care". 2. The rising edge of clock is symbolized by ↑.
 3. $\overline{WRITE} = L$ means Write operation in WRITE TRUTH TABLE.
 $\overline{WRITE} = H$ means Read operation in WRITE TRUTH TABLE.
 4. Operation finally depends on status of asynchronous input pins(ZZ and \overline{OE}).

WRITE TRUTH TABLE

\overline{GW}	\overline{BW}	\overline{WEa}	\overline{WEb}	\overline{WEc}	\overline{WEd}	Operation
H	H	X	X	X	X	READ
H	L	H	H	H	H	READ
H	L	L	H	H	H	WRITE BYTE a
H	L	H	L	H	H	WRITE BYTE b
H	L	H	H	L	L	WRITE BYTE c and d
H	L	L	L	L	L	WRITE ALL BYTES
L	X	X	X	X	X	WRITE ALL BYTES

- NOTE :** 1. X means "Don't Care".
 2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

ASYNCHRONOUS TRUTH TABLE

(See Notes 1 and 2):

Operation	ZZ	\overline{OE}	I/O Status
Sleep Mode	H	X	High-Z
Read	L	L	DQ
	L	H	High-Z
Write	L	X	Din, High-Z
Deselected	L	X	High-Z

NOTE

1. X means "Don't Care".
2. ZZ pin is pulled down internally
3. For write cycles that following read cycles, the output buffers must be disabled with \overline{OE} , otherwise data bus contention will occur.
4. Sleep Mode means power down state of which stand-by current does not depend on cycle time.
5. Deselected means power down state of which stand-by current depends on cycle time.

PASS-THROUGH TRUTH TABLE

Previous Cycle		Present Cycle				Next Cycle
Operation	$\overline{\text{WRITE}}$	Operation	$\overline{\text{CS}}_1$	$\overline{\text{WRITE}}$	$\overline{\text{OE}}$	
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	Initiate Read Cycle Address=An Data=Qn-1 for all bytes	L	H	L	Read Cycle Data=Qn
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	No new cycle Data=Qn-1 for all bytes	H	H	L	No carryover from previous cycle
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	No new cycle Data=High-Z	H	H	H	No carryover from previous cycle
Write Cycle, One byte Address=An-1, Data=Dn-1	One L	Initiate Read Cycle Address=An Data=Qn-1 for one byte	L	H	L	Read Cycle Data=Qn
Write Cycle, One byte Address=An-1, Data=Dn-1	One L	No new cycle Data=Qn-1 for one byte	H	H	L	No carryover from previous cycle

NOTE : 1. This operation makes written data immediately available at output during a read cycle preceded by a write cycle.

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on VDD Supply Relative to VSS	VDD	-0.3 to 4.6	V
Voltage on VDDQ Supply Relative to VSS	VDDQ	VDD	V
Voltage on Input Pin Relative to VSS	VIN	-0.3 to 4.6	V
Voltage on I/O Pin Relative to VSS	VIO	-0.3 to VDDQ+0.5	V
Power Dissipation	PD	1.6	W
Storage Temperature	TSTG	-65 to 150	°C
Operating Temperature	TOPR	0 to 70	°C
Storage Temperature Range Under Bias	TBIAS	-10 to 85	°C

***NOTE** : Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS(0°C ≤ TA ≤ 70°C)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	VDD	3.135	3.3	3.465	V
	VDDQ	3.135	3.3	3.465	V
Ground	VSS	0	0	0	V

***NOTE** : VDD and VDDQ must be supplied with identical voltage levels.

CAPACITANCE*(TA=25°C, f=1MHz)

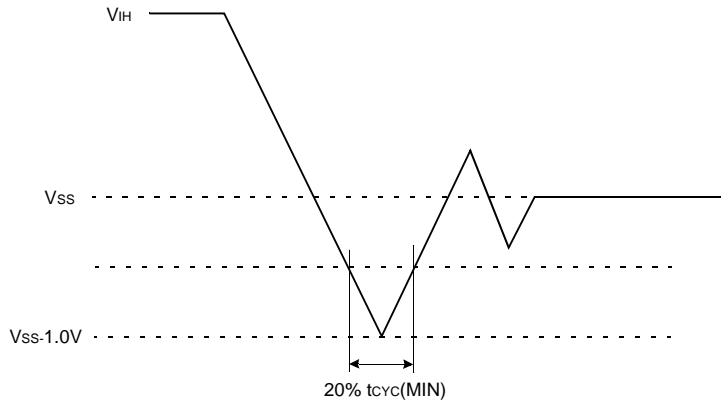
Parameter	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	CIN	VIN=0V	-	6	pF
Output Capacitance	COUT	VOUT=0V	-	8	pF

***NOTE** : Sampled not 100% tested.

DC ELECTRICAL CHARACTERISTICS($V_{DD}=3.3V\pm 5\%$, $T_A=0^{\circ}C$ to $+70^{\circ}C$)

Parameter	Symbol	Test Conditions	Min	Max	Unit	
Input Leakage Current(except ZZ)	IIL	$V_{DD} = \text{Max}$; $V_{IN}=V_{SS}$ to V_{DD}	-2	+2	μA	
Output Leakage Current	IOL	Output Disabled, $V_{OUT}=V_{SS}$ to V_{DDQ}	-2	+2	μA	
Operating Current	ICC	Device Selected, $I_{OUT}=0mA$, $ZZ\leq V_{IL}$, All Inputs= V_{IL} or V_{IH} Cycle Time $\geq t_{CYC}$ Min	-60	-	425	mA
			-67	-	400	
			-72	-	375	
			-10	-	300	
Standby Current	ISB	Device deselected, $I_{OUT}=0mA$, $ZZ\leq V_{IL}$, $f=\text{Max}$, All Inputs $\leq 0.2V$ or $\geq V_{DD}-0.2V$	-60	-	130	mA
			-67	-	120	
			-72	-	110	
			-10	-	100	
	ISB1	Device deselected, $I_{OUT}=0mA$, $ZZ\leq 0.2V$, $f = 0$, All Inputs=fixed ($V_{DD}-0.2V$ or $0.2V$)	-	30	mA	
	ISB2	Device deselected, $I_{OUT}=0mA$, $ZZ\geq V_{DD}-0.2V$, $f=\text{Max}$, All Inputs $\leq V_{IL}$ or $\geq V_{IH}$	-	30	mA	
Output Low Voltage	VOL	$I_{OL}=8.0mA$	-	0.4	V	
Output High Voltage	VOH	$I_{OH}=-4.0mA$	2.4	-	V	
Input Low Voltage	VIL		-0.5*	0.8	V	
Input High Voltage	VIH		2.0	$V_{DD}+0.5^{**}$	V	

** In Case of I/O Pins, the Max. $V_{IH}=V_{DDQ}+0.5V$



TEST CONDITIONS

($T_A=0$ to $70^{\circ}C$, $V_{DD}=3.3\pm 5\%$, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time(Measured at 0.3V and 2.7V)	2ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig. 1

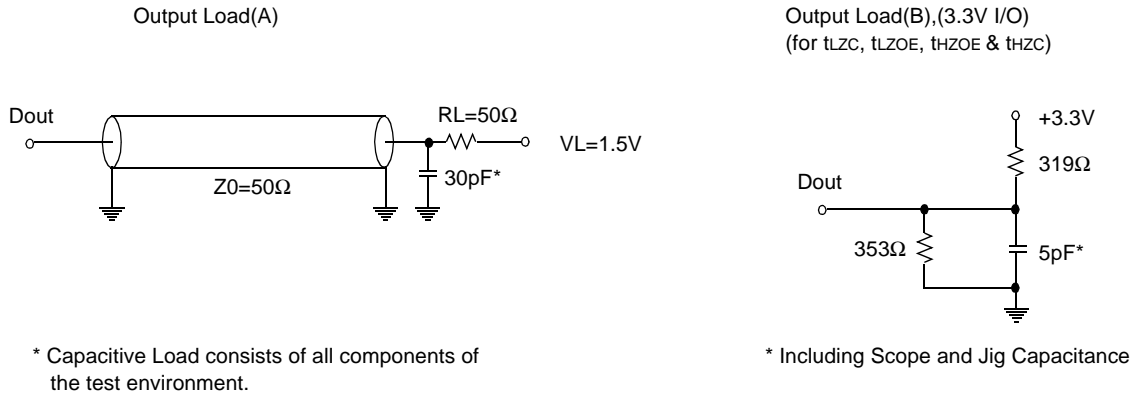


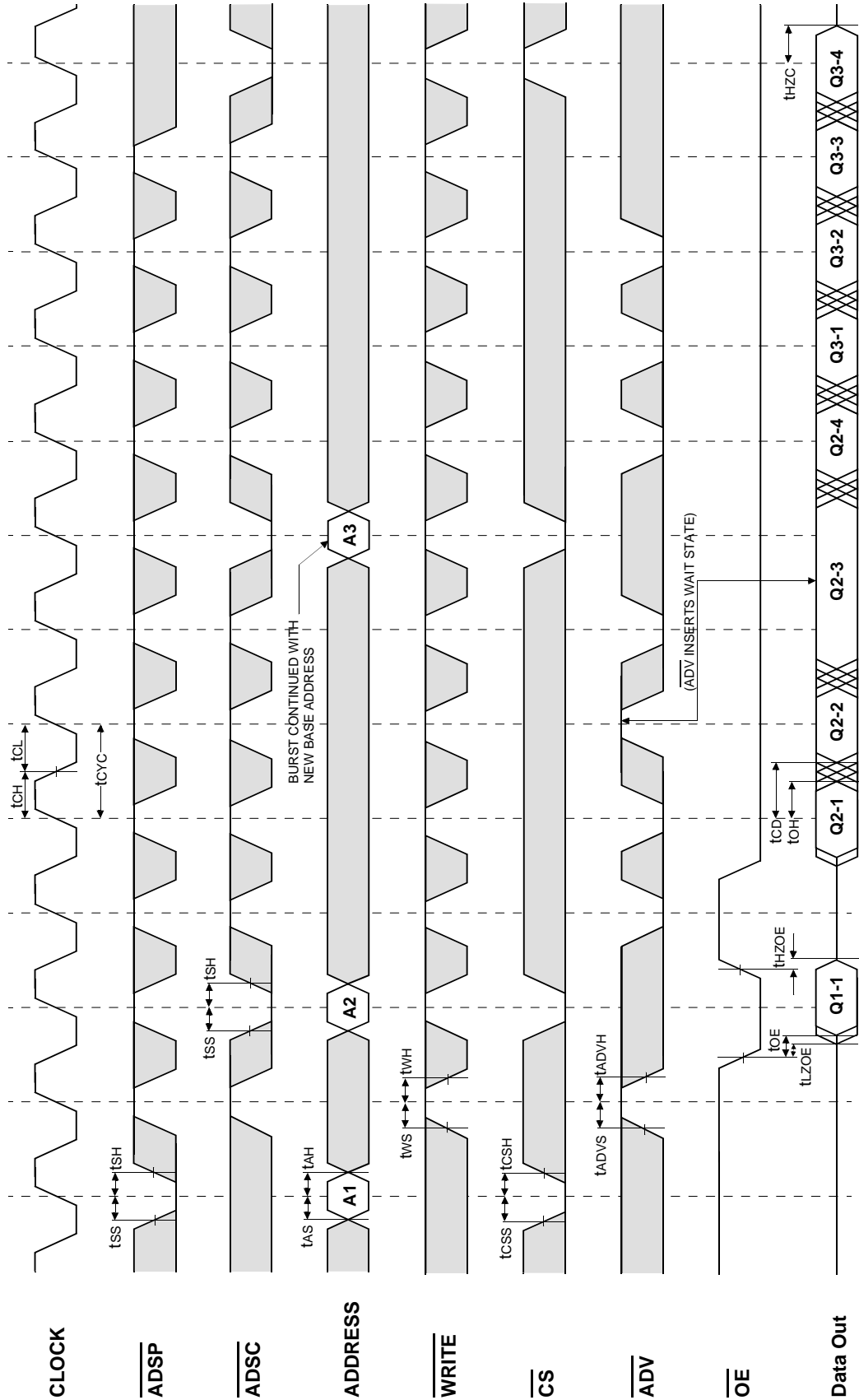
Fig. 1

AC TIMING CHARACTERISTICS($V_{DD}=3.3V\pm 5\%$, $T_A=0^{\circ}C$ to $+70^{\circ}C$)

Parameter	Symbol	-60		-67		-72		-10		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Cycle Time	tCYC	6.0	-	6.7	-	7.2	-	10	-	ns
Clock Access Time	tCD	-	3.5	-	3.8	-	4.0	-	4.5	ns
Output Enable to Data Valid	tOE	-	3.5	-	3.8	-	4.0	-	4.5	ns
Clock High to Output Low-Z	tLZC	0	-	0	-	0	-	0	-	ns
Output Hold from Clock High	tOH	1.5	-	1.5	-	1.5	-	1.5	-	ns
Output Enable Low to Output Low-Z	tLZOE	0	-	0	-	0	-	0	-	ns
Output Enable High to Output High-Z	tHZOE	-	3.0	-	3.0	-	3.5	-	4.0	ns
Clock High to Output High-Z	tHZC	1.5	3.0	1.5	3.0	1.5	3.5	1.5	4.0	ns
Clock High Pulse Width	tCH	2.0	-	2.3	-	2.5	-	3.0	-	ns
Clock Low Pulse Width	tCL	2.0	-	2.3	-	2.5	-	3.0	-	ns
Address Setup to Clock High	tAS	1.5	-	1.5	-	1.5	-	1.5	-	ns
Address Status Setup to Clock High	tSS	1.5	-	1.5	-	1.5	-	1.5	-	ns
Data Setup to Clock High	tDS	1.5	-	1.5	-	1.5	-	1.5	-	ns
Write Setup to Clock High (\overline{GW} , \overline{BW} , \overline{WEx})	tWS	1.5	-	1.5	-	1.5	-	1.5	-	ns
Address Advance Setup to Clock High	tADVS	1.5	-	1.5	-	1.5	-	1.5	-	ns
Chip Select Setup to Clock High	tCSS	1.5	-	1.5	-	1.5	-	1.5	-	ns
Address Hold from Clock High	tAH	0.5	-	0.5	-	0.5	-	0.5	-	ns
Address Status Hold from Clock High	tSH	0.5	-	0.5	-	0.5	-	0.5	-	ns
Data Hold from Clock High	tDH	0.5	-	0.5	-	0.5	-	0.5	-	ns
Write Hold from Clock High (\overline{GW} , \overline{BW} , \overline{WEx})	tWH	0.5	-	0.5	-	0.5	-	0.5	-	ns
Address Advance Hold from Clock High	tADVH	0.5	-	0.5	-	0.5	-	0.5	-	ns
Chip Select Hold from Clock High	tCSH	0.5	-	0.5	-	0.5	-	0.5	-	ns
ZZ High to Power Down	tPDS	2	-	2	-	2	-	2	-	cycle
ZZ Low to Power Up	tPUS	2	-	2	-	2	-	2	-	cycle

NOTE : 1. All address inputs must meet the specified setup and hold times for all rising clock edges whenever ADSC and/or ADSP is sampled low and CS is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.
2. Both chip selects must be active whenever ADSC or ADSP is sampled low in order for the this device to remain enabled.
3. ADSC or ADSP must not be asserted for at least 2 Clock after leaving ZZ state.

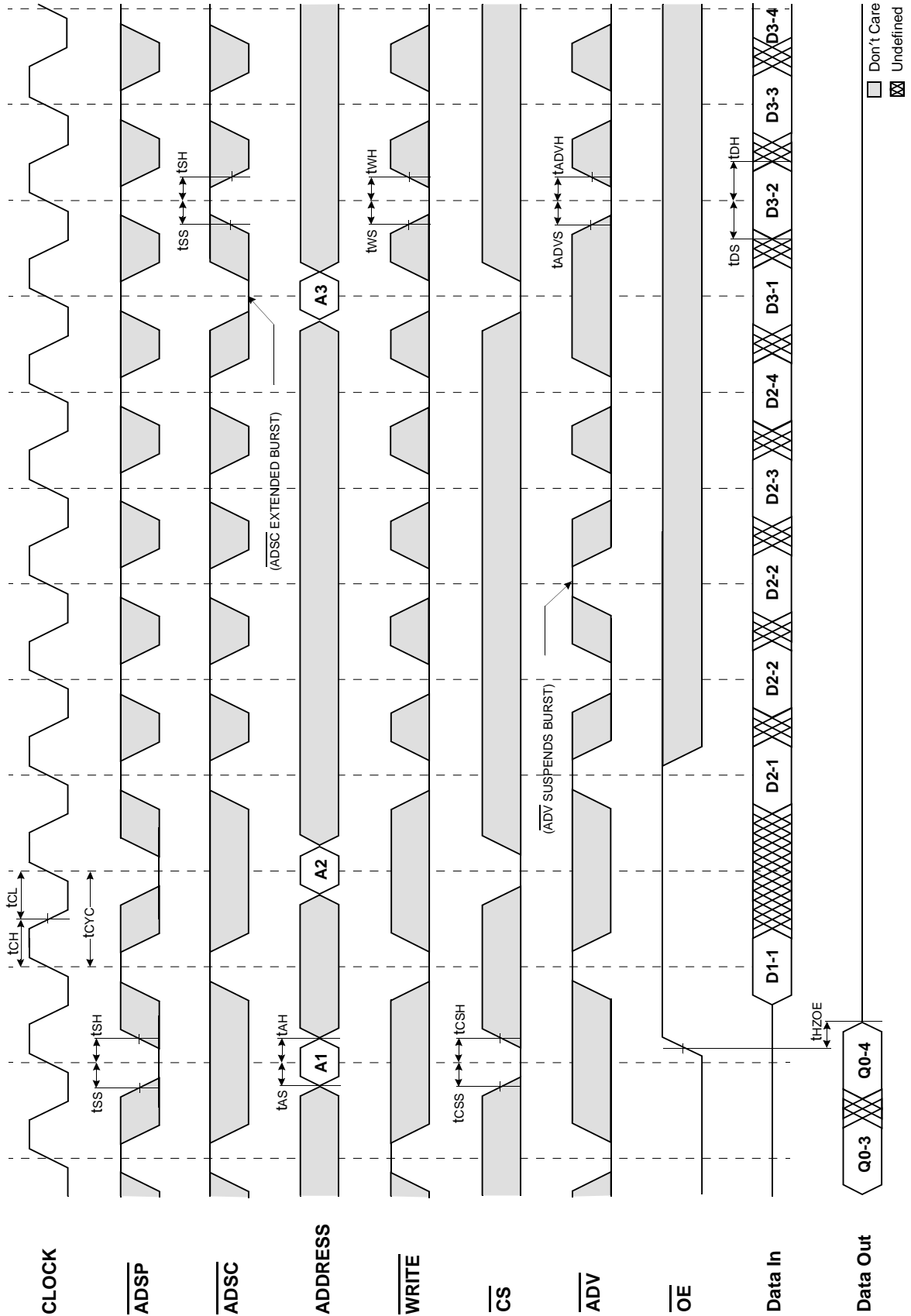
TIMING WAVEFORM OF READ CYCLE



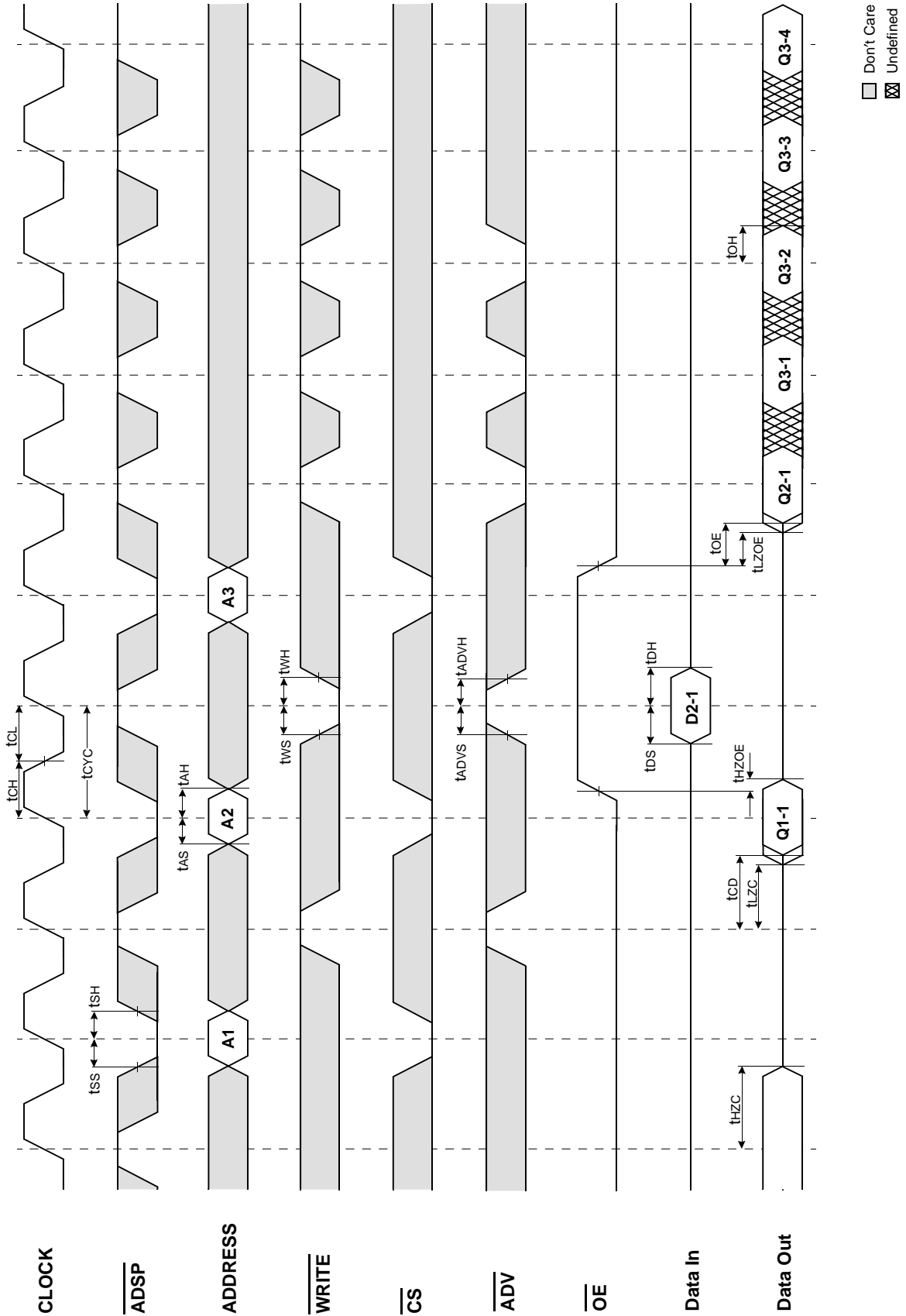
□ Don't Care
⊗ Undefined

NOTES: $\overline{WRITE} = L$ means $\overline{GW} = L$, or $\overline{GW} = H, \overline{BW} = L, \overline{WE} = L$
 $\overline{CS} = L$ means $\overline{CS1} = L, \overline{CS2} = H$ and $\overline{CS2} = L$
 $\overline{CS} = H$ means $\overline{CS1} = H$, or $\overline{CS1} = L$ and $\overline{CS2} = H$, or $\overline{CS1} = L$, and $\overline{CS2} = L$

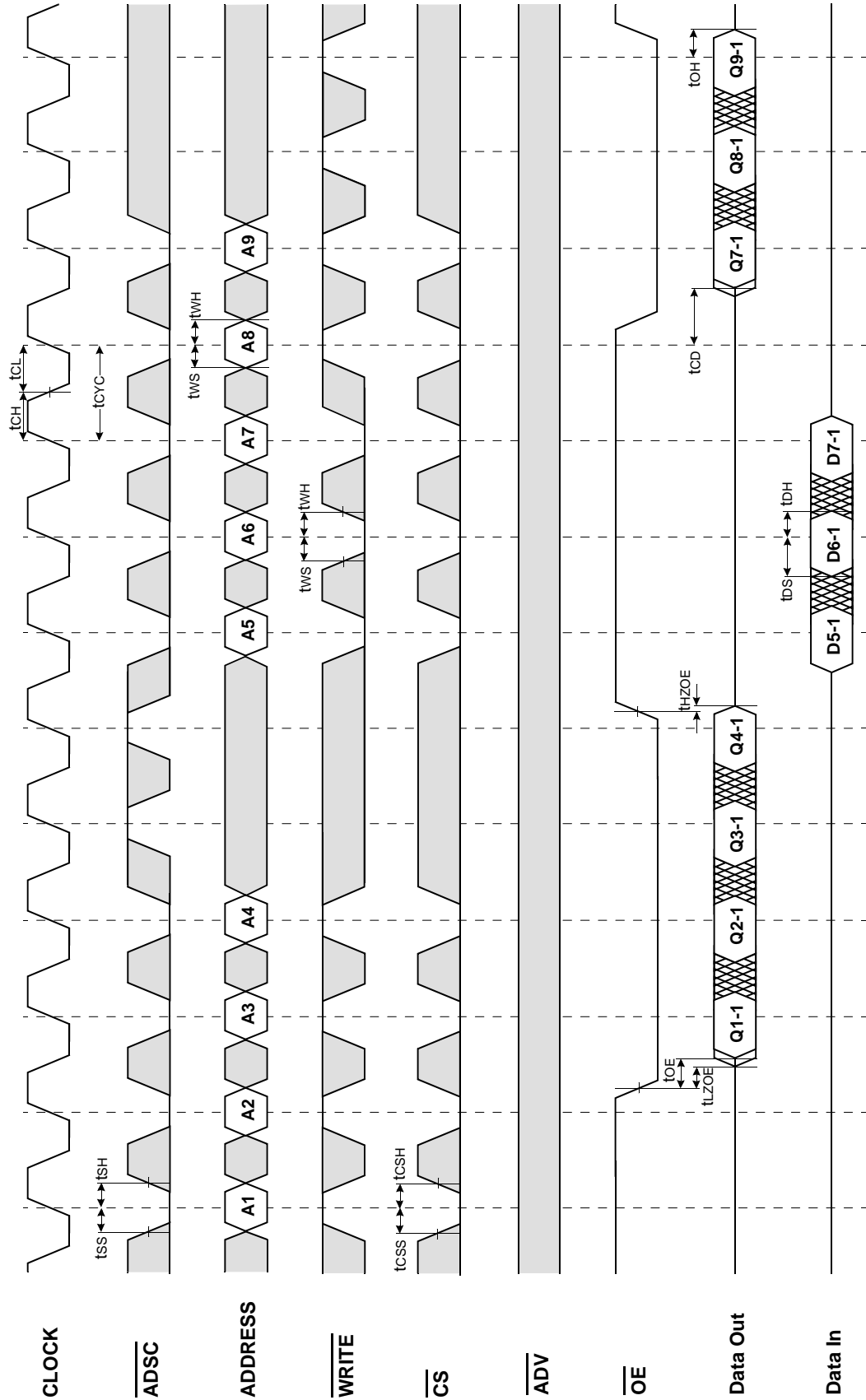
TIMING WAVEFORM OF WRTE CYCLE



TIMING WAVEFORM OF COMBINATION READ/WRITE CYCLE(ADSP CONTROLLED, $\overline{\text{ADSC}}=\text{HIGH}$)

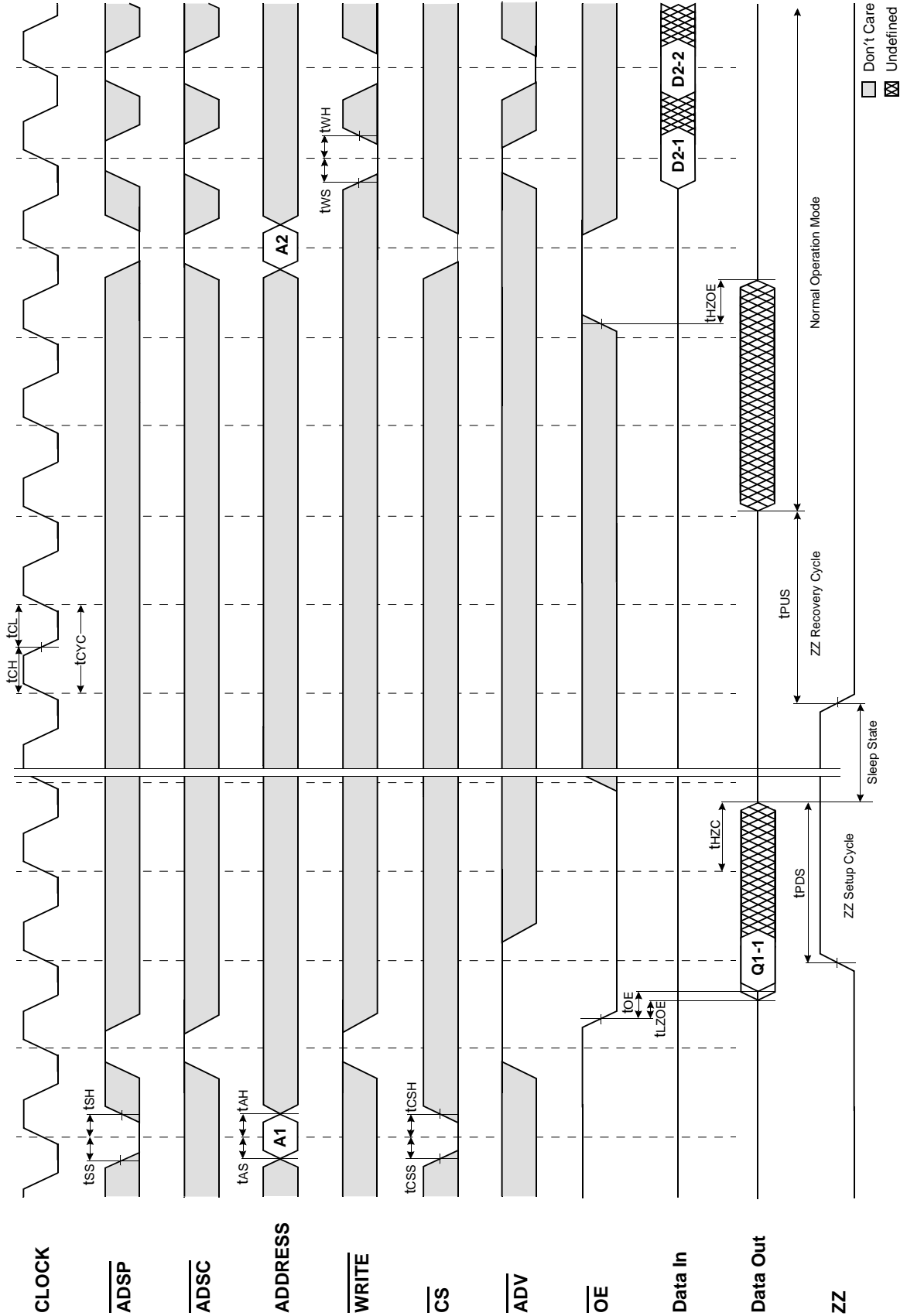


TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE(ADSC CONTROLLED, $\overline{\text{ADSP}}=\text{HIGH}$)



□ Don't Care
⊠ Undefined

TIMING WAVEFORM OF POWER DOWN CYCLE

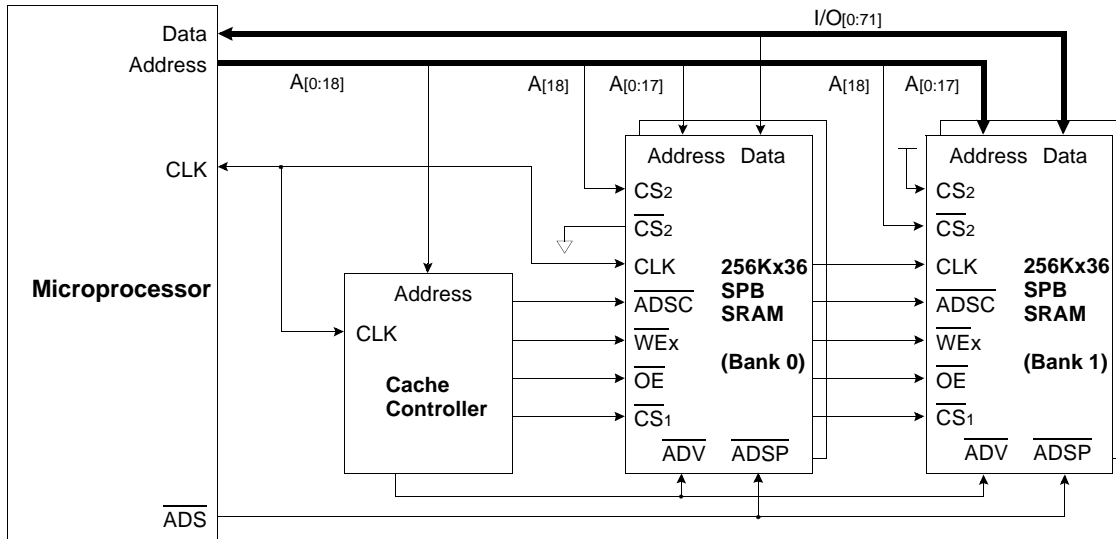


□ Don't Care
⊠ Undefined

APPLICATION INFORMATION

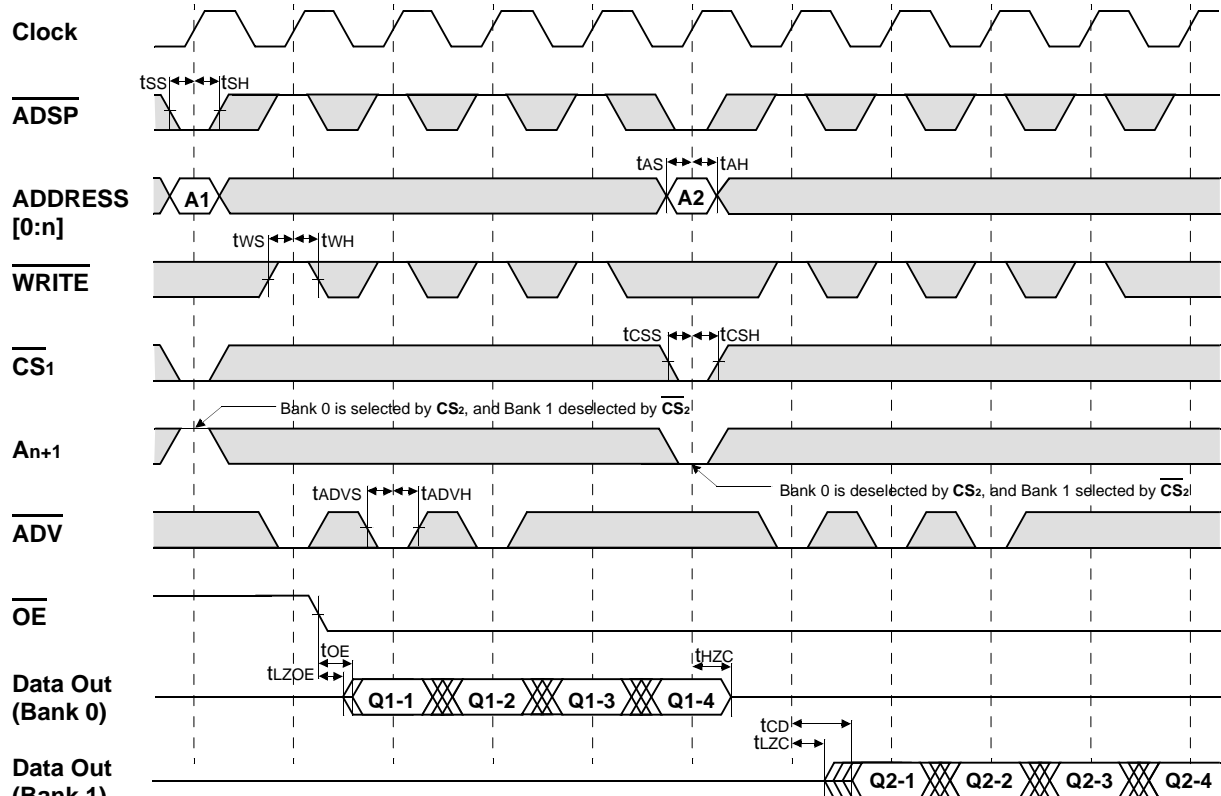
DEPTH EXPANSION

The Samsung 256Kx36 Synchronous Pipelined Burst SRAM has two additional chip selects for simple depth expansion. This permits easy secondary cache upgrades from 256K depth to 512K depth without extra logic.



INTERLEAVE READ TIMING (Refer to non-interleave write timing for interleave write timing)

(ADSP CONTROLLED , ADSC=HIGH)



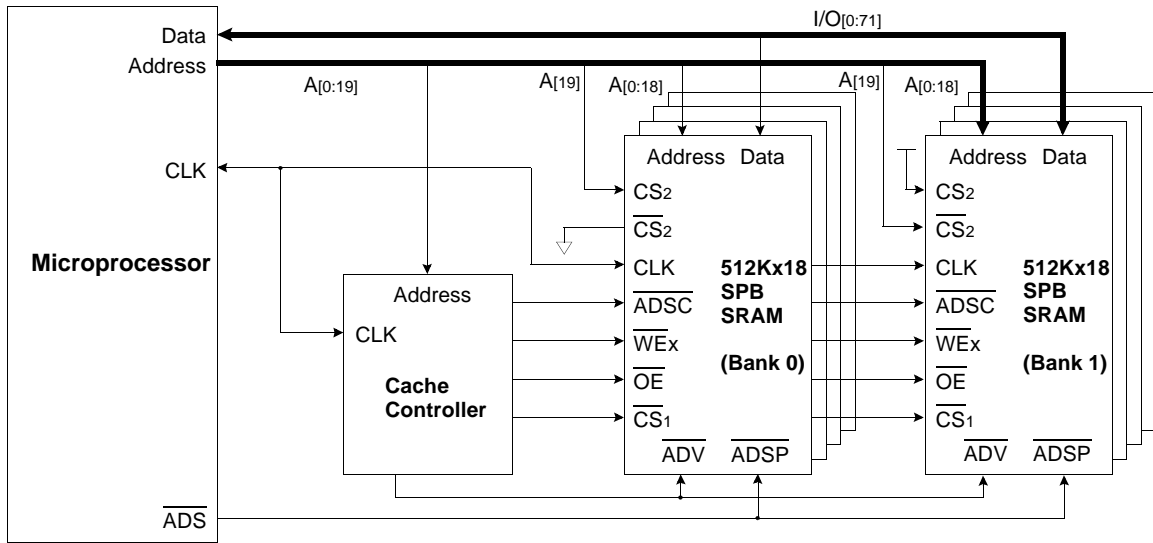
*NOTES n = 14 32K depth
15 64K depth
16 128K depth
17 256K depth
18 512K depth
19 1024K depth

□ Don't Care ⊗ Undefined

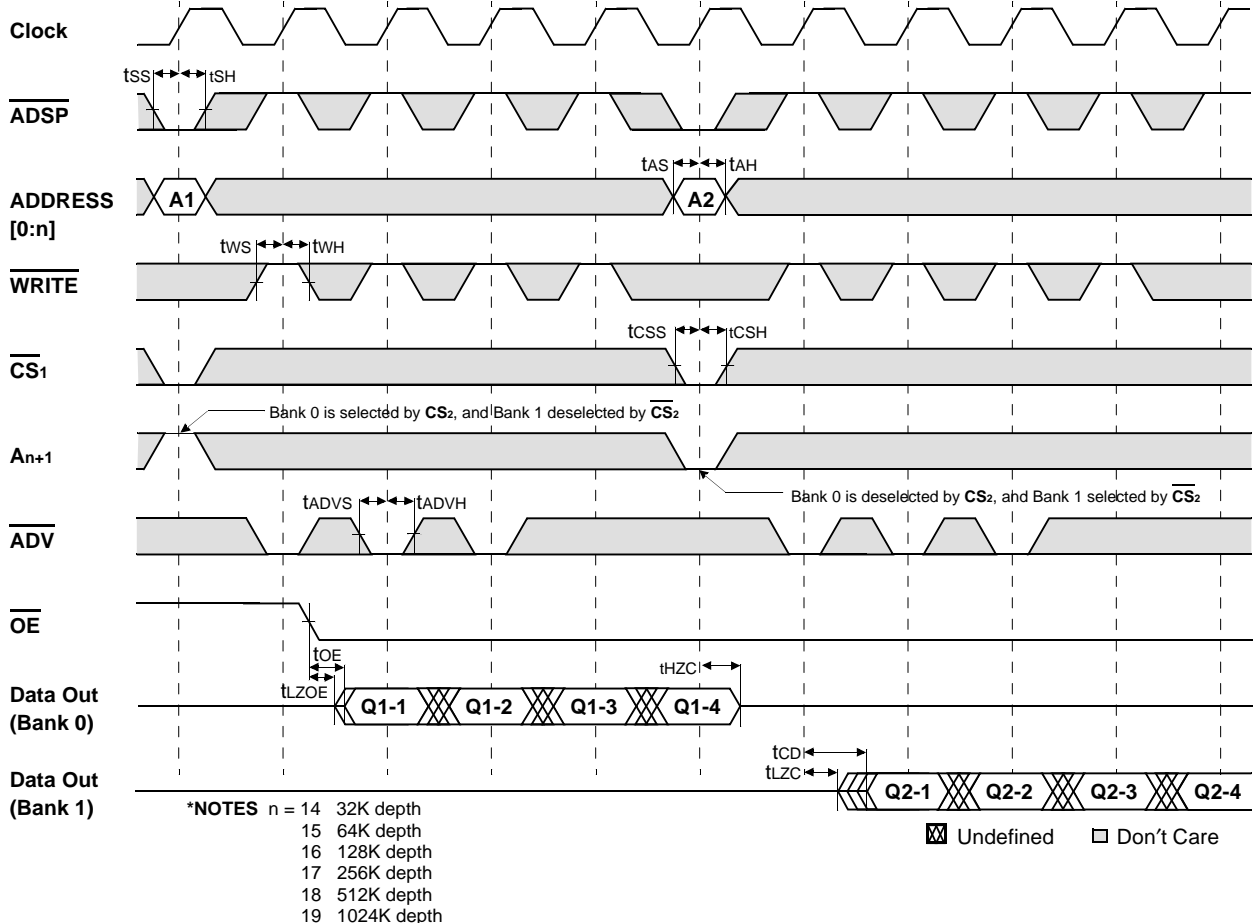
APPLICATION INFORMATION

DEPTH EXPANSION

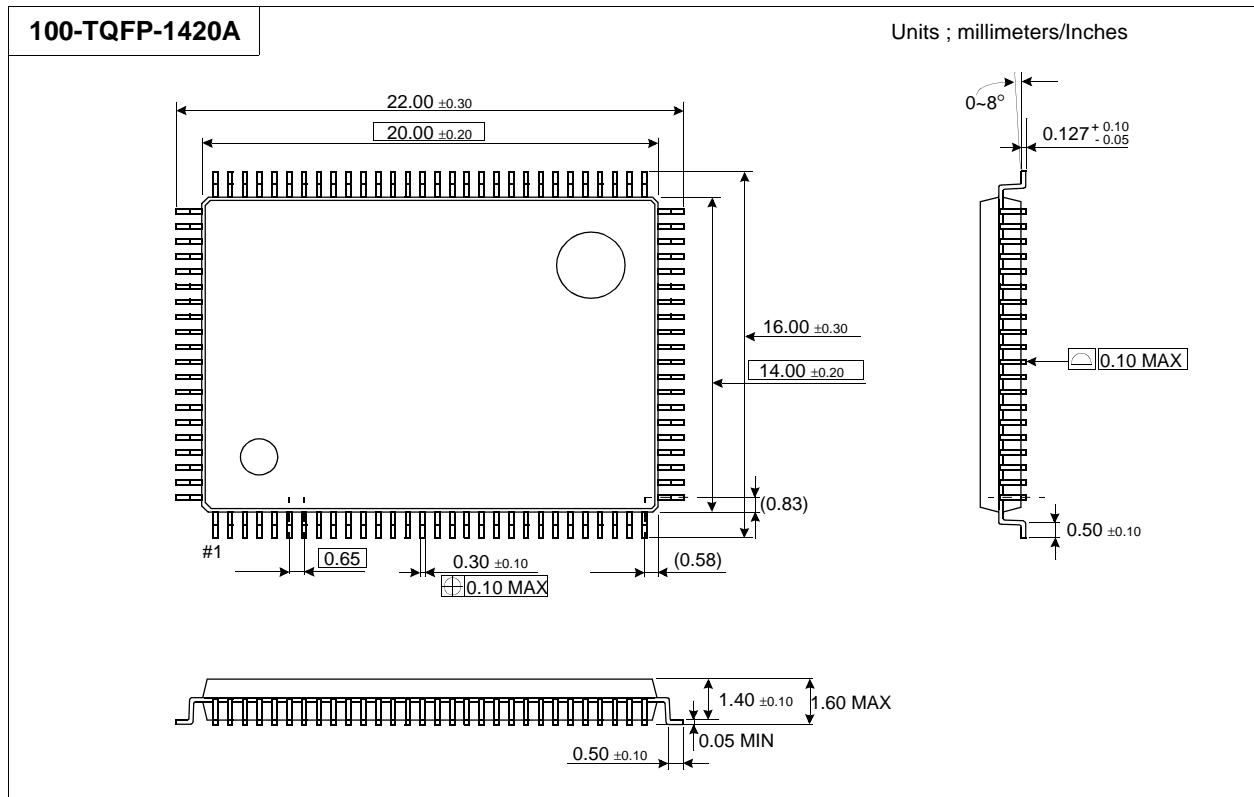
The Samsung 512Kx18 Synchronous Pipelined Burst SRAM has two additional chip selects for simple depth expansion. This permits easy secondary cache upgrades from 512K depth to 1024K depth without extra logic.



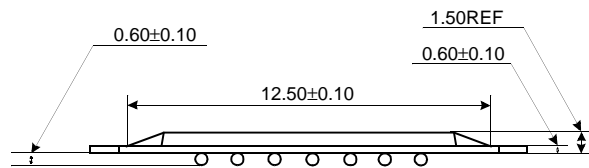
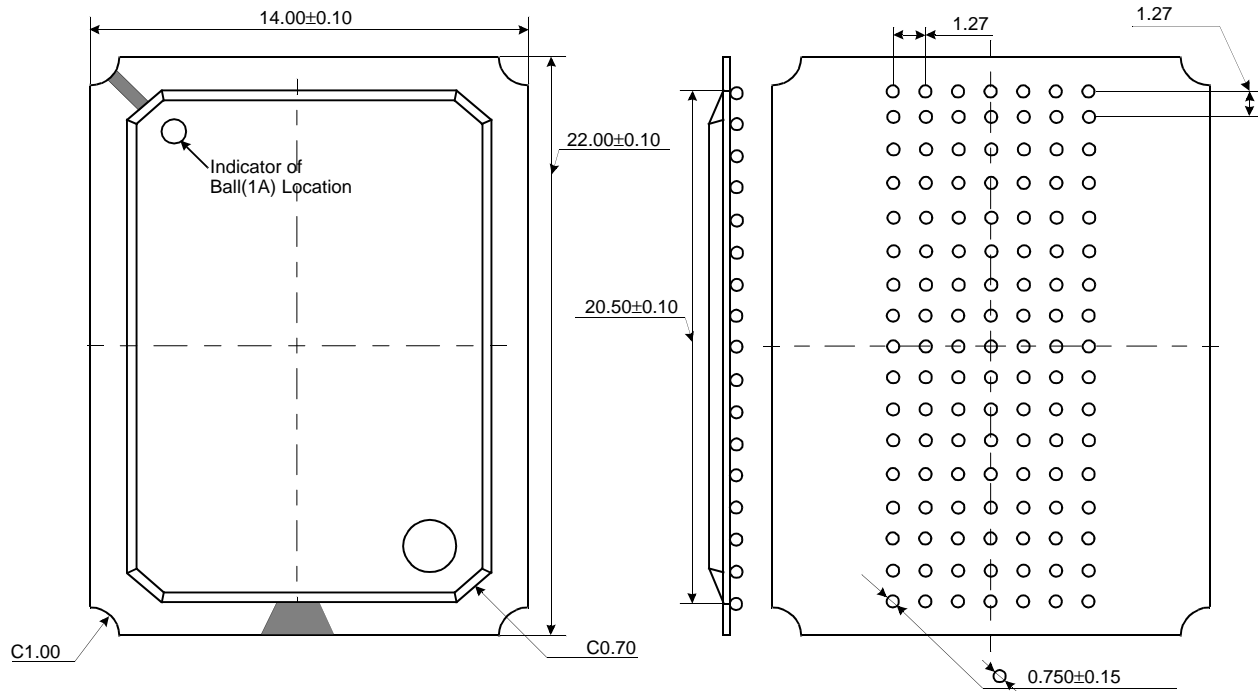
INTERLEAVE READ TIMING (Refer to non-interleave write timing for interleave write timing)
(ADSP CONTROLLED , ADSC=HIGH)



PACKAGE DIMENSIONS



119 BGA PACKAGE DIMENSIONS



NOTE :

1. All Dimensions are in Millimeters.
2. Solder Ball to PCB Offset : 0.10 MAX.
3. PCB to Cavity Offset : 0.10 MAX.