LOW-POWER 5.0 VOLT SINGLE-CHIP READ CHANNEL for DISK DRIVES

User Manual

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1.0 Nomenclature

Lowercase signal names correspond to internal signals.

Uppercase signal names correspond to signals accessible through package pins.

References to VDD and VSS apply also to AVDDx and AVSSx.

Register bit abbreviation is RX[dy] where X = register number and y = bit number.

All signals are active high unless shown with a bar, e.g. $\overline{\text{signal}}$.

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2.0 Overview

The IMP62C548 is a high-speed, low-power, fully-integrated read-channel IC intended for disk-drive applications. The chip uses a single power supply. The architecture of the chip provides maximum flexibility while minimizing the number of external components required. It contains all of the read-channel electronics, excluding the preamplifier and controller, on a single CMOS chip. Data rates can range from 15 Mbs to 48 Mbs. Low-power operation is achieved by employing low-voltage design techniques, CMOS technology, and a sophisticated power-down scheme. The device accommodates constant-density recording and embedded servo functions without need for any additional external components. The on-chip frequency synthesizer enables changes in the transfer rate and the on-chip filter tracks the data rate, with asymmetrical (or symmetrical) pulse slimming. These features, and more, are programmable through the serial interface.

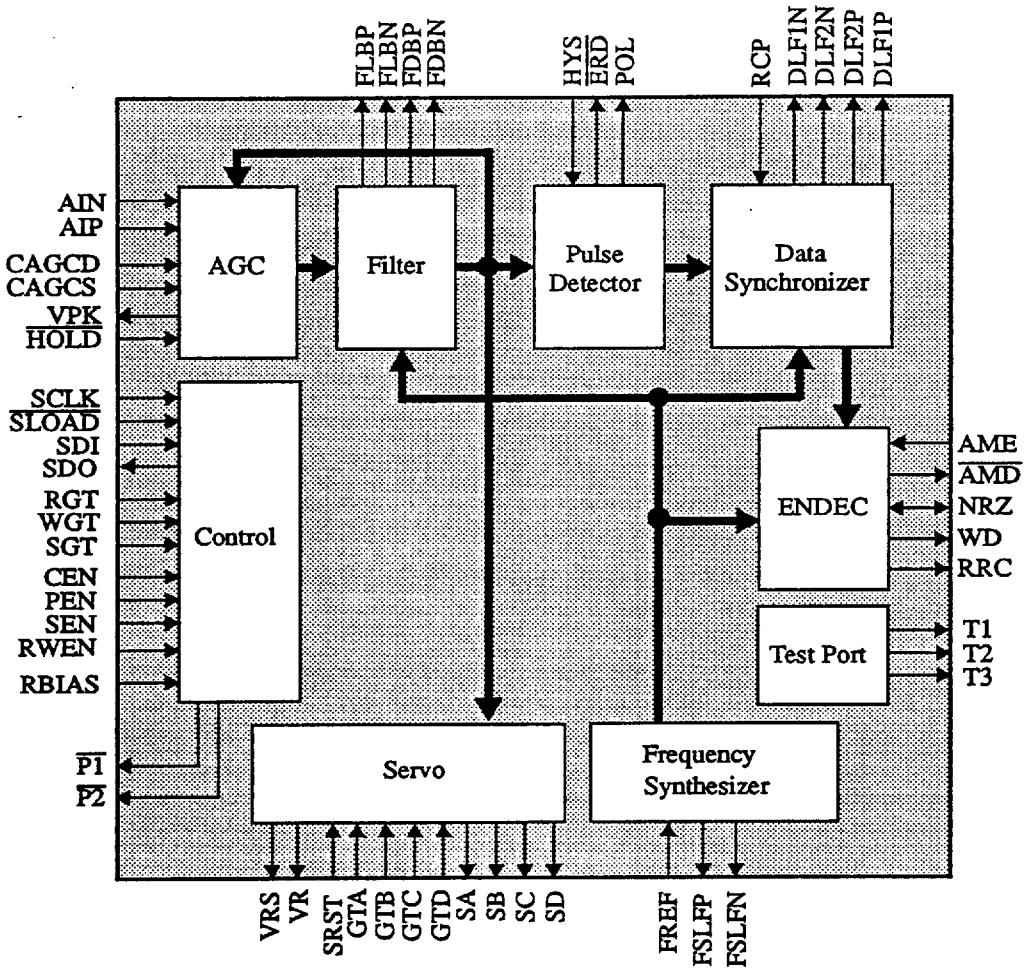

Figure 1. Block Diagram

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3.0 Functional Description

3.1 Control Block

The chip interfaces to the controller through a simple serial interface. Data is organized in 16-bit sequences. An 8-bit address is shifted in first, followed by eight bits of data (MSB first). Only 4 bits of the address word are used to support the 16 internal registers, thus leaving the remaining address space to allocate to other circuits sharing the serial control lines. Address and data are clocked in on the rising edge of SCLK and loaded to one of the internal registers on the rising edge of $\overline{\text{SLOAD}}$.

The Readback function can be used to verify register programming. To obtain information from the chip's internal registers, shift in the readback address (0000 1111) followed by the address of the register to be read back in the 8 bit data field as shown in the table in section 6.15. During Readback, eight bits of data are shifted out on the SDO pin on the falling edge of SCLK. After the eighth rising edge of SCLK, preceded by the first falling edge of SCLK after $\overline{\text{SLOAD}}$ transitions high, the SDO output will become high impedance.

The Control-Logic block allows any of seven power modes to be selected through combinations of chip inputs (CEN with PEN, SEN or RWEN), *logical OR*, by writing to the Mode-Control register through the serial interface. Table 1 defines how the power modes are enabled, and what circuits are activated by these modes. Some setup time is required when switching between modes as specified in section 5.3.

In sleep mode (Sleep) all functions are inactive except the Serial Interface *(readback is inactive also during Sleep)*. This mode could be used when the head is unloaded or the spindle motor is stopped. During this mode the AGC integrator caps, servo detector caps, filter tuning PLL, frequency synthesizer PLL, and data synchronizer PLL are initialized. All programmed internal register values are preserved.

One of two Idle modes may be used during a seek or a condition when neither data or servo is being read; however, the read channel is in a state that may be quickly activated. If the PEN input is inactive then a low power idle mode (Idle) is activated. In this mode only the bias circuits are active. The charge on the AGC integrator caps, filter tuning, frequency synthesizer and data synchronizer PLL filters is preserved with minimal leakage. A medium power idle mode (Idle w/ PLLs) may be enabled when PEN is active. In this mode the bias circuits, filter tuning PLL, frequency synthesizer and data synchronizer PLL are active. This mode would be used to minimize the time required from RWEN active to the data field.

The servo-tracking mode (Servo) is used when only servo data is being read. The AGC, Filter, Servo and Pulse Detector are active. A servo with PLLs active mode (Servo w/PLLs) is available that also keeps the PLLs active.

The read/write mode (Read/Write) is used for either reading or writing data. In this mode, the AGC, Filter and Filter Tuning, Pulse Detector, Data Separator, Frequency Synthesizer, and ENDEC functions are all active. When a servo frame is encountered, servo with read/write mode (Servo w/ RW) is used which activates the Servo functions along with the functions listed above.

The Reference block generates the reference voltages and currents needed by the rest of the chip. Currents are derived from an external resistor connected to the RBIAS pin.

A power-on-reset signal, *por*, is provided to reset registers to the default state shown in Section 6.1.

Two programmable *Bounce Barrier*™ digital outputs are provided, $\overline{\text{P1}}$ and $\overline{\text{P2}}$. These low noise, ground-bounce-immune outputs may be used as low-noise preamp select controls. Writing a "1" to R13[d4] causes the impedance switch to turn on for a time equal to the WGT delay set in R1[d2,d3]. This reduces the settling time of the AGC input coupling capacitors due to offset changes when switching head-preamps using the $\overline{\text{P1}}$ and $\overline{\text{P2}}$ outputs.

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Table 1: Power Mode Definitions

Power Mode	RWEN	PEN	SEN	CEN	Circuits Active
Sleep	X	X	X	0	Serial Interface (write only)
Idle	0	0	0	1	Serial Interface Bias circuits
Idle w/PLLs	0	1	0	1	Serial Interface Bias circuits Filter Tuning PLL Frequency Synthesizer PLL Data Synchronizer PLL
Servo	0	0	1	1	Serial interface Bias circuits AGC Filter Pulse Detector Servo
Servo w/PLLs	0	1	1	1	Serial interface Bias circuits AGC Filter Pulse Detector Servo Filter Tuning PLL Frequency Synthesizer PLL Data Synchronizer PLL
Servo w/RW	1	X	1	1	Serial interface Bias circuits AGC Filter Pulse Detector Servo Filter Tuning Frequency Synthesizer Data Synchronizer ENDEC
Read/Write (no servo)	1	X	0	1	Serial interface Bias circuits AGC Filter Pulse Detector Filter Tuning Frequency Synthesizer Data Synchronizer ENDEC

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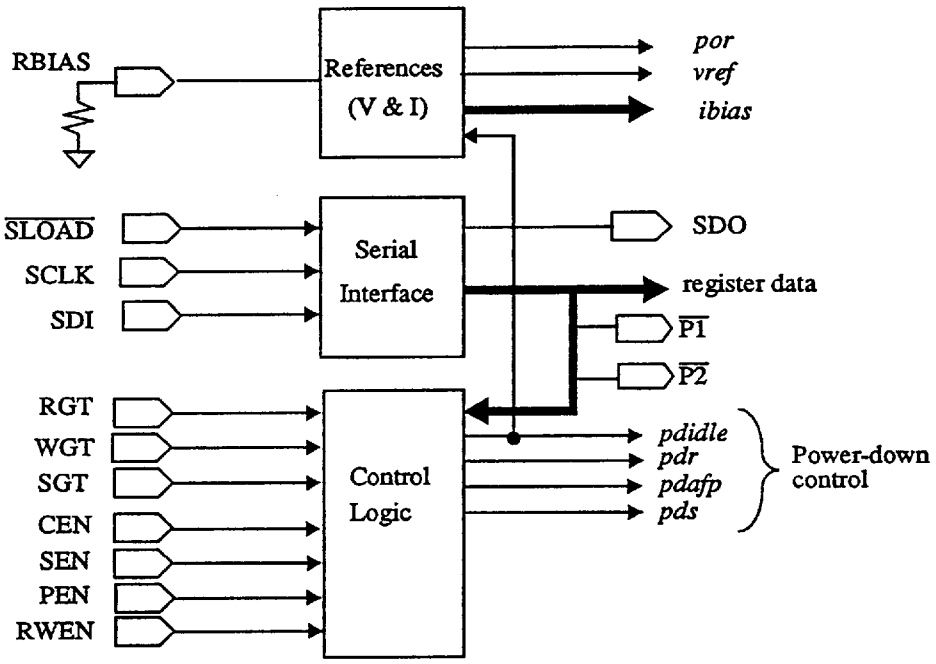

Figure 2. Control Block Diagram

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3.2 AGC

The AGC is used to control the input signal level of the Filter. It includes the voltage-controlled, variable-gain amplifier (VGA), the integrator, and the peak detector. A gain stage is provided to extend the effective control range, and an impedance switch for quick recovery between writing and reading. The AGC has special controls selectable through the serial interface, (*zdly, droop, gain & agc disable*) to provide flexibility.

The input to the AGC is the ac-coupled output of the external preamplifier. When WGT is active, the AGC's differential inputs are shorted through a low-impedance path to an internally-generated analog ground (*vcm*) while the AGC control voltage is held constant. This mode will continue after WGT becomes inactive until a programmable time-out occurs. This allows the input signal from the external preamplifier to settle before enabling the AGC. When the $\overline{\text{HOLD}}$ input is active the AGC control voltage will be held constant, permitting the AGC loop to hold its gain during periods of embedded servo bursts.

The input level range is controlled by programming the gain stage through the serial interface. The VGA has a 16dB automatic-gain range. The VGA may be programmed into an AGC disabled mode in which the VGA is forced to a fixed mid-range gain.

The AGC has effectively two control loops. A separate integrating capacitor(CAGCS) is used when SGT is active and a different capacitor(CAGCD) is used when SGT is inactive. This reduces the AGC settling time when switching between servo and data frames. The gain of the AGC is adjusted by comparing the differential peak-to-peak voltage at the *flpp* and *flpn* outputs of the Filter to an internally-generated reference voltage (*vrh*). The result is integrated on an external capacitor at either the CAGCS or CAGCD pin.

The master-slave peak detector is used to drive the AGC integrator and optionally the hysteresis control circuitry of the Pulse Detector. The output of the peak detector tracks the peak magnitude of the input signal with minimum droop between peaks. The master is a traditional peak detector that has its droop set by an internal current source and capacitor. The slave is also a peak detector that is only allowed to droop when the master is charging. This implementation results in minimum droop during periods of no data or few data transitions while allowing a fast response to actual changes in peak signal levels. Under normal conditions of reading data, the droop of the master cell is controlled to allow a limited amount of droop during the longest permissible string of zeros in the input signal. When the input signal drops suddenly to zero, the master detector doesn't charge and no discharge of the slave detector occurs. The slave detector will hold its level until the master detector has decayed to 10% of *vrh* in which it will be rapidly discharged and the AGC gain goes to a maximum limit. When a signal appears again the input to the peak detector is over-driven. While the master peak detector output is driven greater than 25% of the normal AGC level (125% of *vrh*), the master droop rate is increased by 3. This gives a droop time less dependent upon the over-driven level. The droop of the master detector is independently programmable for servo and data mode operation. Selection is made by SGT. If the slave peak detector output voltage (VPK) is greater than 125% of *vrh*, the integrator gain is also boosted by 3 to provide an AGC fast attack mode. Normal attack and decay of the control voltage for the VGA are symmetrical.

When CEN has been inactive, and then activated, the capacitors on the CAGCD and CAGCS pins are pre-charged to a mid gain condition for faster recovery. The Peak detector is also reset.

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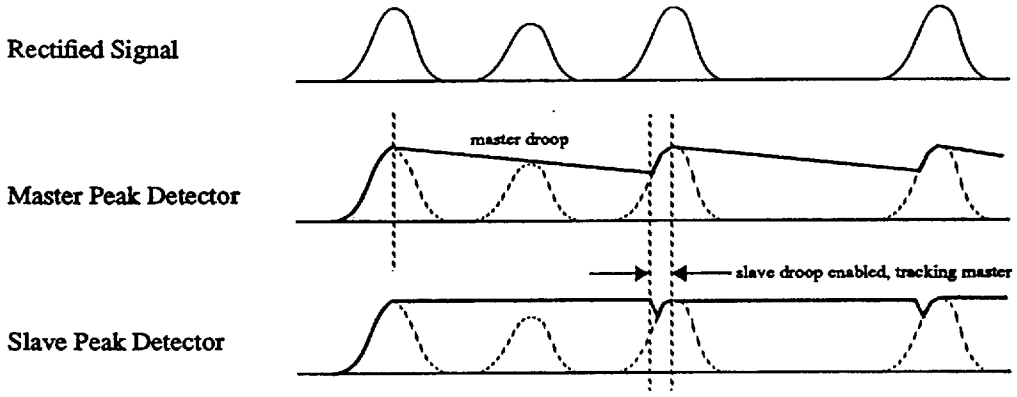

Figure 3. AGC Waveforms

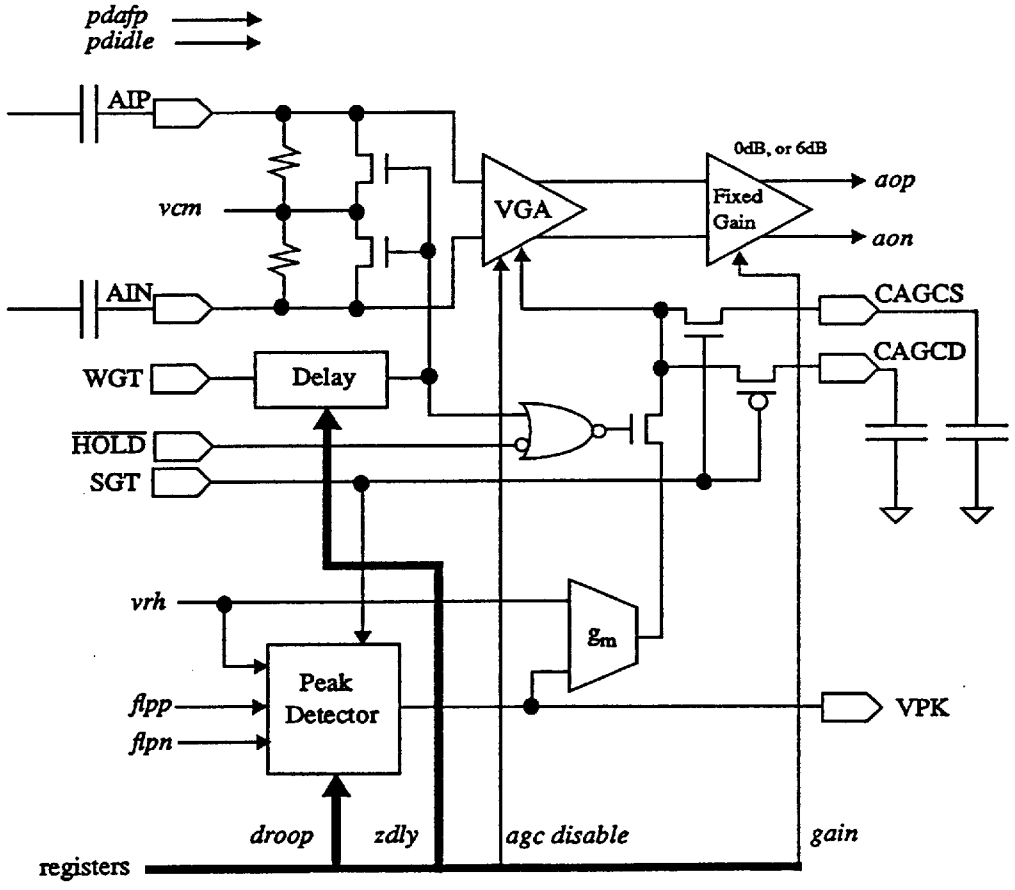

Figure 4. AGC

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3.3 Filter

The filter utilizes a CMOS g_m/C technology to provide amplitude and phase equalization of the read signal. It consists of a 6th-order, linear-phase, 0.05° equiripple, low-pass response with programmable cutoff and asymmetrical pulse slimming. The filter is master-slave tuned to the synthesized write reference clock, *wclk*. The Filter Tuning Control circuit provides both coarse tuning (capacitor bank setting) and fine tuning (transconductance setting) control of the cutoff frequency.

Since the servo cutoff frequency can be different from that required for data, asserting SGT selects: 1) the separate pulse-slimming register values, 2) a separate register containing a fixed servo coarse-tuning control value, and 3) the fine tuning is set to a constant value *vb* (a mid-range transconductance setting). This allows the filter response to be quickly changed during the servo mode. The value of the servo coarse-tuning register is set during a servo-tuning mode (*see Application Note iAN-9, Programming the Filter Cutoff for Servo Mode*). During this servo-tuning mode the frequency synthesizer is programmed to provide an appropriate frequency of *wclk* for scaling to the desired servo filter cutoff. The tuning circuit stores the state of the coarse-tuning control at the conclusion of the servo-tuning mode.

The filter tuning PLL, frequency synthesizer and frequency scaling register settings are not used during the actual servo mode of the filter (SGT active).

Coarse tuning can be always enabled, always disabled, or disabled only when RGT is active under control of the serial interface (see section 6.4). The Filter Tuning Control circuit is only enabled when PEN or RWEN is active.

To block differential offset on the filter input and outputs, DC cancellation circuits are used. This adds 2 high pass poles that are low enough not to distort the group delay.

The transfer function of the slave filter is the following:

$$H_{Norm} = \left(\frac{\omega_{P_1}^2}{s^2 + s\frac{\omega_{P_1}}{Q_{P_1}} + \omega_{P_1}^2} \right) \left(\frac{\omega_{P_2}^2 \left(1 + \frac{s}{\omega_{z_a}}\right)}{s^2 + s\frac{\omega_{P_2}}{Q_{P_2}} + \omega_{P_2}^2} \right) \left(\frac{\omega_{P_3}^2 \left(1 - \frac{s}{\omega_{z_b}}\right)}{s^2 + s\frac{\omega_{P_3}}{Q_{P_3}} + \omega_{P_3}^2} \right)$$

$$H_{Diff} = S \cdot H_{Norm}$$

The poles of the low-pass response are given in the following table:

Biquad	ω_p	Q_p
1	2.074	1.686
2	1.470	0.893
3	0.981	0.551

Note: ω_c normalized to 1 rad/sec

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The programmable zeros ω_{za} and ω_{zb} provide the pulse slimming. They are programmed as follows:

$$\omega_{z_a} = 0.58 \cdot \frac{15}{n_a} \cdot \omega_c \qquad n_a \in (0...15)$$

$$\omega_{z_b} = 0.58 \cdot \frac{15}{n_b} \cdot \omega_c \qquad n_b \in (0...15)$$

When $\omega_{za} = \omega_{zb}$, symmetrical pulse slimming results. Asymmetrical slimming can be achieved by manipulating the ratio of ω_{za} and ω_{zb}.

The filter cutoff is 1/3 *wclk* by default at power-up. This frequency scaling ratio is programmable (see section 6.5).

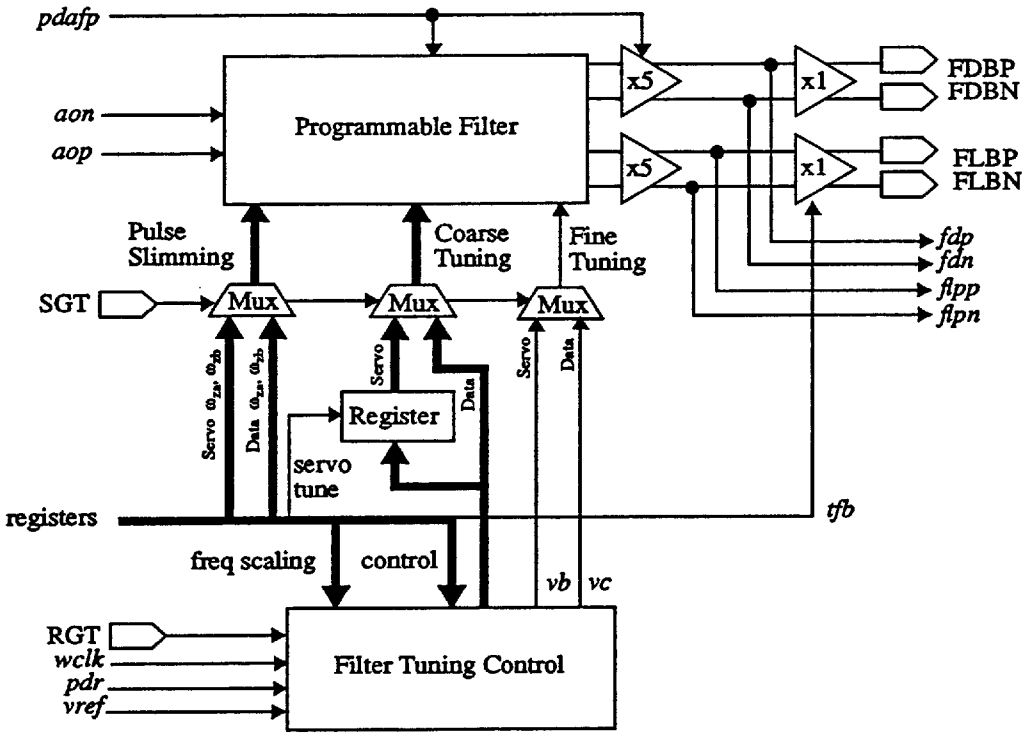

Figure 5. Filter Block Diagram

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3.4 Servo

The servo detector can be used for either burst-pattern, interlace-pattern, or quadrature detection. The input signal for the Servo Detector block is taken from the low-pass output of the Filter. It is full-wave rectified and peak detected, thus providing subsequently decreasing time window gates to an internal current source. For improved noise rejection this current source, not the input signal, charges the on-chip detector holding capacitor with a constant slew rate (consult with IMP Applications Engineering regarding slew rate values available through metal mask programming). Selection of the desired detector holding capacitor is by external control. The four detected burst levels are provided on the buffered outputs, SA, SB, SC and SD, which are referenced to an internally-generated voltage, VRS. The buffers on these outputs are powered when SEN is activated and remain powered until the servo reset input, SRST, is activated.

To properly set the servo gain, the AGC should be enabled during the servo normalization field, SN. Before the end of the servo normalization field, the gain of the AGC should be held by activating the $\overline{\text{HOLD}}$ pin. The AGC gain will then remain constant during the Sync, Gray Code and Servo Burst fields (in Fig. 6 "G" denotes the Sync and Gray Code fields, A, B, C, and D are the servo bursts).

A level shifter generates VRS (used as the servo-reference voltage), *vrh* (used by the AGC and Pulse detector), and VR (used as a reference for an external servo A/D). Though VRS is typically 45% VDD, the differential reference output VR-VRS is stable. The ground reference of the external servo A/D is typically connected to VRS, and the full scale reference to VR.

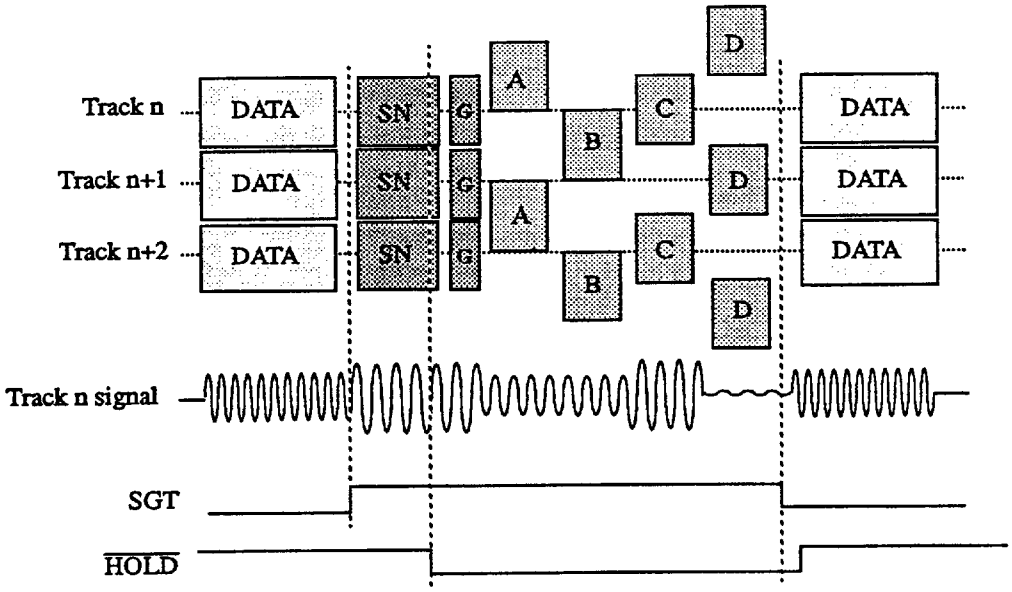

Figure 6. Quadrature Servo Burst Pattern

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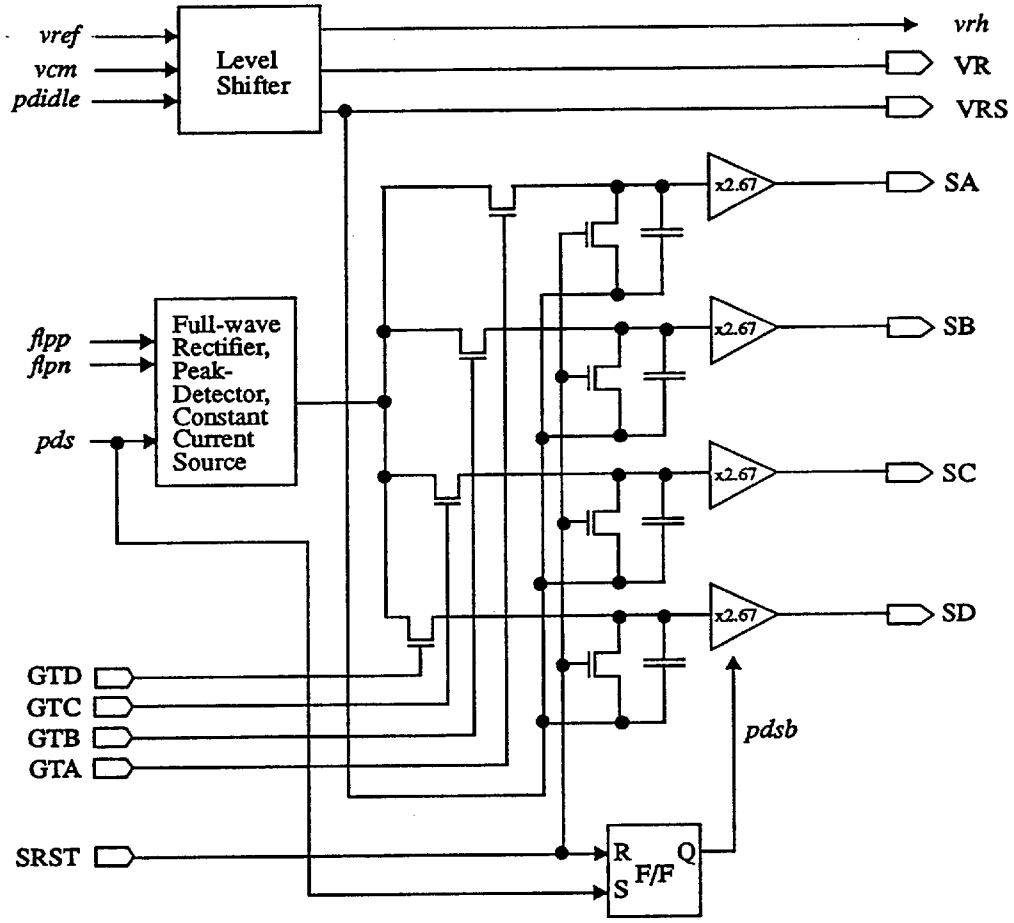

Figure 7. Servo Detector

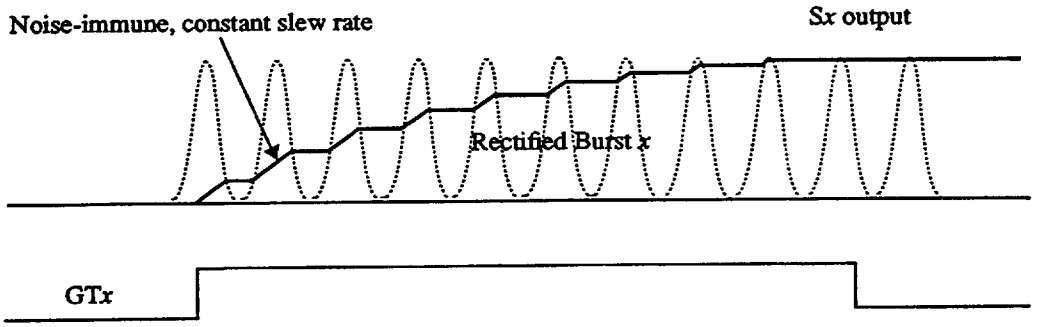

Figure 7a. Typical Burst Acquisition

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3.5 Pulse Detector

The pulse detector consists of a zero-crossing comparator, a hysteresis comparator, qualification logic and a monostable. Pulses are provided on the encoded read data output, $\overline{ERD}$, in which the falling edge of the pulse corresponds to the peak of the filtered data signal. POL indicates the polarity of the these pulses. Depending on the setting of R13[d0], the $\overline{ERD}$ and POL signals are available only when SGT is active (thus reducing on-chip noise generation during data mode), or always available (i.e., for test purposes). The zero-crossing detector is driven by the differentiated outputs of the filter (*fdp* & *fdn*). Either a maximum or minimum of the filtered-data signal (*flpp* & *flpn*) is indicated when the differentiated signal crosses zero. The comparator with hysteresis provides an amplitude qualification of the zero crossings of the differentiated signal to prevent false triggering by baseline noise.

Separate hysteresis levels may be programmed for servo and data. Servo hysteresis is enabled when SGT is active and data hysteresis is enabled when SGT is inactive. The hysteresis levels are programmable through the serial interface. The levels may be scaled to a fixed reference voltage, *vrh*, or dynamically by connecting the HYS pin to an RC-integrator driven by the VPK pin. Selection of the hysteresis reference is programmed through the serial interface.

Polarity qualified data signals generate a pulse for each detected peak. An additional polarity qualification is then applied. A qualified peak of one polarity must be followed by a qualified peak of the opposite polarity before another peak of the same polarity is allowed.

A threshold qualified servo signal (R13[d1]=1) generates a pulse for each detected peak.

A polarity qualified servo signal (R13[d1]=0) generates a pulse for each detected peak. An additional polarity qualification is then applied. A qualified peak of one polarity must be followed by a qualified peak of the opposite polarity before another peak of the same polarity is allowed.

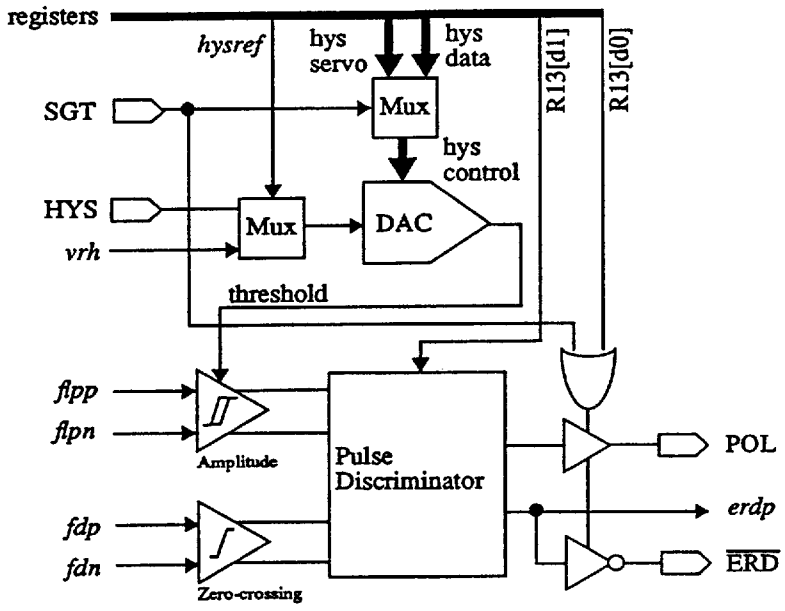

Figure 8. Pulse Detector Block Diagram

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3.6 Frequency Synthesizer

The frequency synthesizer generates clock references that are used in the Filter, Data Synchronizer and ENDEC. The input to the frequency synthesizer is the reference clock (FREF) and its output is *wclk*, where:

$$wclk = \frac{M}{N} \times FREF$$

The scaling coefficients, M and N, are programmed through the serial interface with 7-bit precision. The center frequency (f_{CTR}) of the frequency synthesizer's VCO is also programmed through the serial interface.

The frequency synthesizer provides a bias current used in the Data Synchronizer to set the center frequency of its PLL and to scale the delay of its Delay Cells accordingly. The programmability of the frequency synthesizer is useful in zoned recording applications.

The phase detector is a type IV detector (detects both phase and frequency). The charge pump current is referenced to the RBIAS resistor. The external loop filter is fully-differential and balanced to suppress common-mode noise.

Equations for calculating the PLL filter components are found in Application Note iAN-8, *IMP62Cx3x Loop Filter Design*. An easy to use PC-compatible program is also available. Please consult with IMP Applications Engineering.

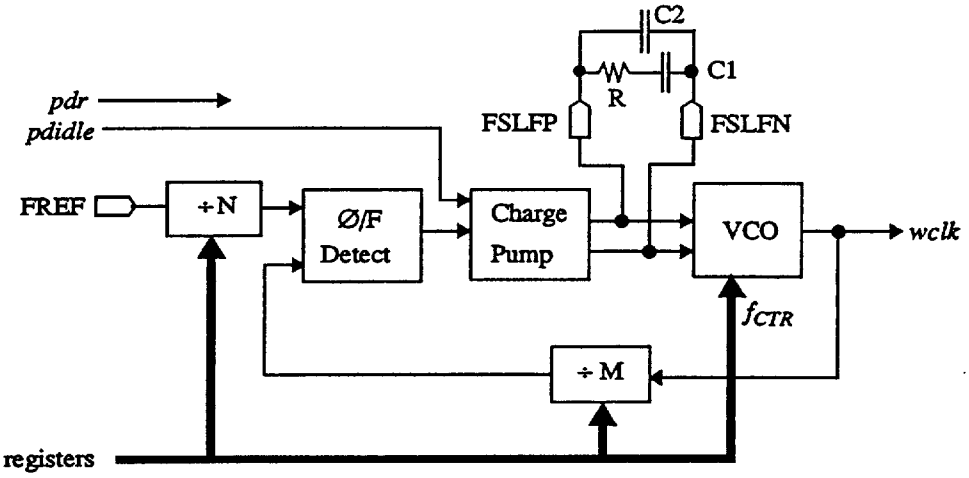

Figure 9. Frequency Synthesizer Block Diagram

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3.7 Data Synchronizer

The output of the Pulse Detector (*erdp*) is fed into the Data Synchronizer block, which extracts the clock (*rclk*), and uses it to synchronize the data (*syncdata*). Control of the Data Synchronizer is provided by the ENDEC block and is defined in that section (3.8).

The two delay line cells track the frequency synthesizer's bias current and have a delay nominally one half the window (*wclk* period). The delay line cells, together with the data align circuit, provide window adjustment for margin testing. Window adjustment does not disturb the PLL since it is outside the loop.

When the window adjustment is bypassed, R9[d5:d0] = all zeros, *syncdata* is taken from the output of the Pulse Gate. When the window adjustment is enabled, R9[d5:d0] = non-zero, window adjustment may be used to correct for window centering errors. Either mode may be used during a read operation.

An external, fully-differential and balanced loop filter is used to suppress common-mode noise. The loop filter is driven by two separate pairs of charge pump outputs. The programmable charge pump allows the loop characteristics to be optimized for each zone in a zoned-recording application.

The programmable charge pump has a current multiplier, K_S, which is used to speed up the PLL during the preamble sequence. A second current multiplier, K_G, programs the gain of the loop while reading data and is used to control the loop parameters when switching between zones. The gain switches automatically from K_S to K_G after successful acquisition and detection of the preamble.

The first two current multipliers are duplicated in the IDLF2 path, which controls the current at the DLF2 pins and are used to scale the loop compensation zero. A constant ratio of loop bandwidth to loop zero is automatically maintained to give a constant damping factor. The charge pump current is scaled by an external resistor connected to the RCP pin.

The VCO has a linear transfer characteristic, and its center frequency is set by the Frequency Synthesizer. Zero phase restart is used to speed up the acquisition time when switching from the reference write clock (*wclk*) to data (*erdp*) and back again. The output of the VCO is fed back to the phase detector to close the loop.

Equations for calculating the PLL filter components are found in Application Note iAN-8, *IMP62Cx3x Loop Filter Design*. An easy to use PC-compatible program is also available. Please consult with IMP Applications Engineering.

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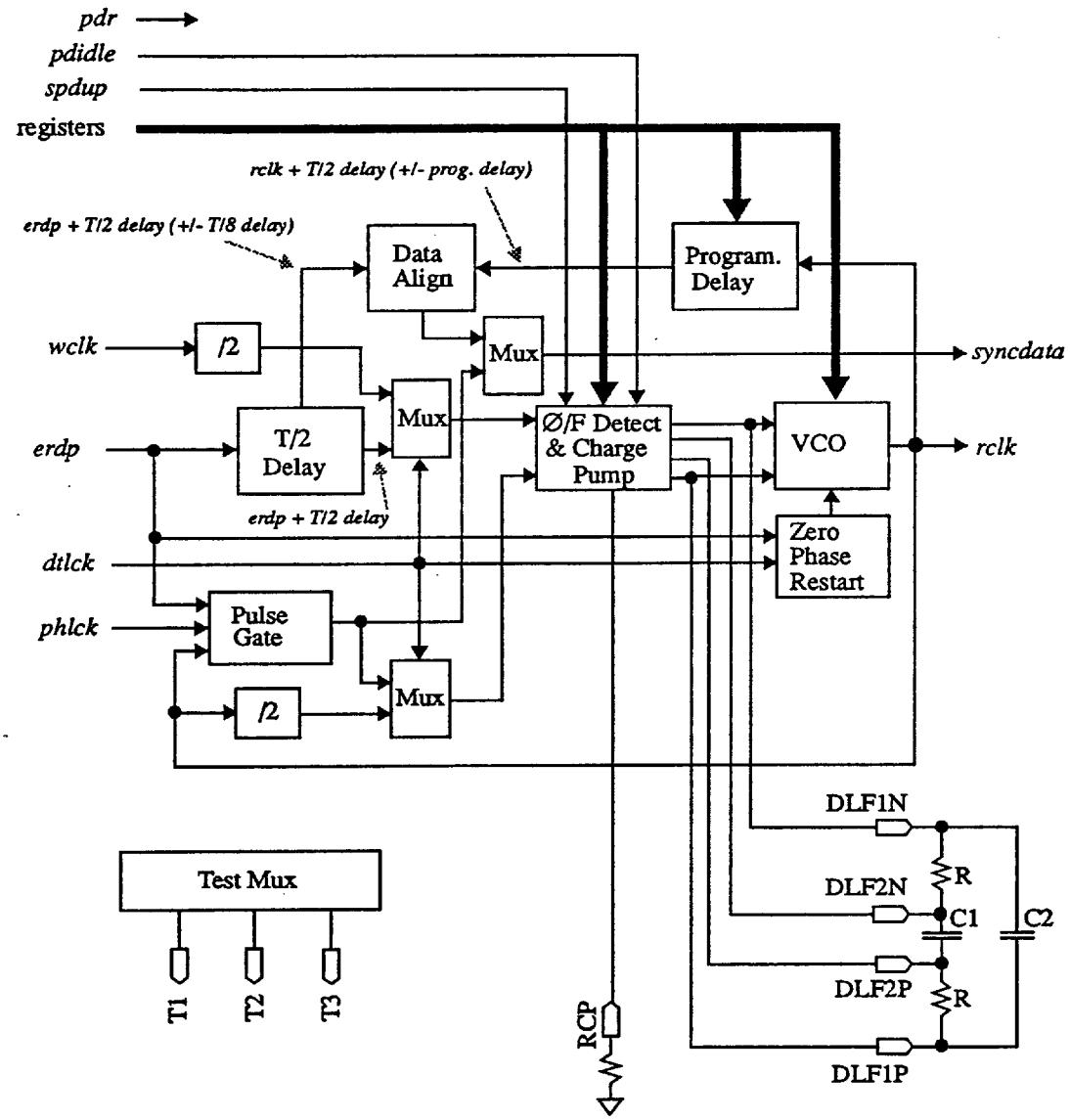

Figure 10. Data Synchronizer Block Diagram

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3.8 ENDEC

The ENDEC block consists of the (1,7) encoder and decoder, read reference clock generation and address mark detection. The decoder's input data is the *syncdata* signal generated by the Data Synchronizer. The data is clocked-in with *rclk*, decoded, and is then clocked-out by the read reference clock output. The decoder block is enabled by RGT and *predct* signals. The NRZ data is made available to the controller on the bi-directional NRZ pin when RGT is active.

In a write operation, the controller provides the NRZ data on the NRZ pin. This data is clocked out of the controller by the RRC output of the read channel. In Write mode, RRC is derived from the *wclk* signal provided by the Frequency Synthesizer block. The data is then encoded at the *wclk* rate, and provided at the WD output of the ENDEC. After WGT goes active, the controller must provide consecutive "01" data bits for the duration of the sync field. This pattern is encoded to provide the 3T(010) preamble pattern. After the first two bits "01" are shifted into the chip, encoding begins. After completion of the preamble pattern, data may follow with no restrictions on the remaining bits.

Initially the data synchronizer PLL is locked to *wclk/2* in a frequency-lock-mode. A hard sectored read operation begins when the read gate, RGT, becomes active. The preamble detector then starts to count the 3T(010) patterns on *erdp*. Upon the first *erdp* after RGT goes active, *dtlck* signal becomes active, the Ø/F detector is switched to the delayed read data and the VCO is restarted. At this time, a phase-lock mode is enabled if R0[d6] = "0", otherwise the loop continues to operate in a frequency-lock-mode until completion of the preamble synchronization. Changing the detector to its phase-detection mode is done by enabling the pulse-gating function. In the frequency-lock-to-data mode, the VCO output, *rclk*, is divided by 3. After counting an additional programmable number of consecutive 3T patterns, framing of the decoder is enabled. Upon completion of framing, the input of the divider which generates RRC, is switched from *wclk* to the output of the VCO, *rclk*. At that time the data PLL is assumed to be locked, *predct* is activated, and if R0[d6] = "1", the pulse gate block is switched to phase-lock mode. The RRC period may increase up to an equivalent of 2 normal RRC clock periods during the RRC switching; however, no short duration glitches will occur. The number of 3T patterns counted may be programmed to either 8, 12, 16, or 20 through the serial interface (does not include the three 3Ts of a soft address mark). Upon RGT going inactive, the input of the divider which generates RRC, is switched from the output of the VCO back to *wclk* without glitching, and the Data Synchronizer is switched from *erdp* to *wclk/2* and its VCO is restarted.

A soft sector write operation is initiated by activating the AME input while WGT is active. Operation is the same as for hard sector operation except that an 8T 8T 12T 12T sequence is inserted when AME goes active. At the completion of this sequence, an additional three 3T patterns are encoded from the incoming NRZ data. The complete address mark consists of the 8T 8T 12T 12T sequence inserted by the read channel and the 3T 3T 3T encoded from incoming data provided by the external datapath controller.

A soft sector read operation is initiated by activating the AME input. An address mark must be first detected before the read lock sequence can be started. A complete address mark consists of an 8T 8T 12T 12T 3T 3T 3T pattern. Detection of this pattern is considered successful when the following 3 conditions are met:

1. Detect a "1" followed by at least 6 consecutive "0"s (i.e. 1000000...),
2. Detect a "1" followed by at least 9 consecutive "0"s (i.e. 1000000000...) with no more than 36 *wclk* clocks from the detection of sequence 1,
3. Detect a "1" followed by three consecutive 3T patterns (i.e. 1001001001) in less than 36 *wclk* clocks from the detection of sequence 2. A valid 3T pattern must be within the range of 2 to 4 *wclk* clocks.

Violation of any of these 3 conditions will cause the address search operation to be restarted. Preamble detection begins upon the successful completion of sequence 2. $\overline{\text{AMD}}$ is activated upon the successful completion of sequence 3. RGT must be activated prior to completion of the

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preamble detection, or within 12 *wclk* clocks after $\overline{\text{AMD}}$ becomes active. If RGT was not activated, the address mark search will be restarted. If AME becomes inactive before the completion of sequence 3, then the address mark search will be stopped.

The ENDEC may be bypassed by setting a bit in the mode register, *edbp*. This causes the RRC clock divider to be disabled, thus RRC is switched to either *wclk* for writing or *rclk* for reading. When RGT and WGT are inactive, RRC is *wclk*.

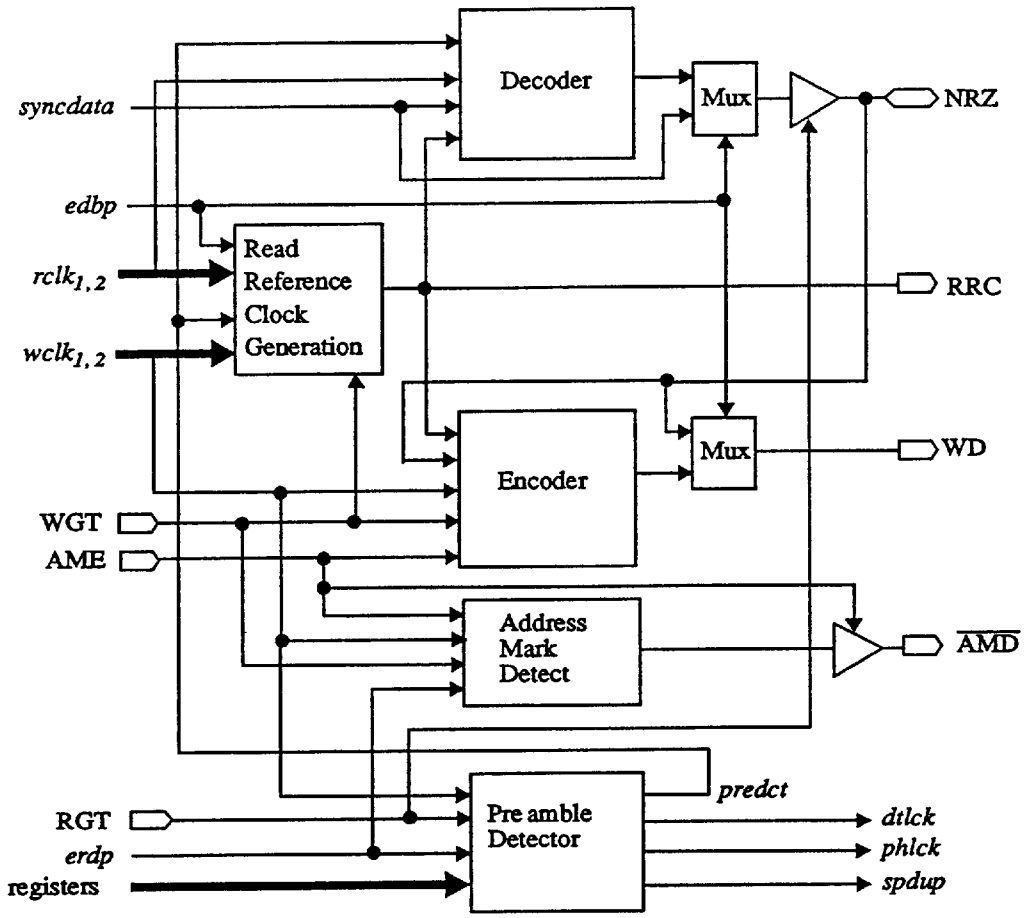

Figure 11. (1,7) ENDEC

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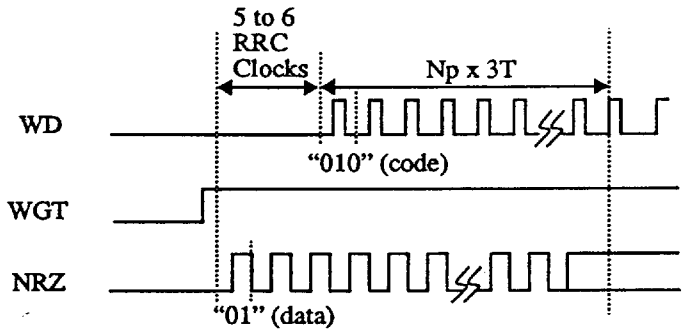

Figure 12. Hard-Sectored Write

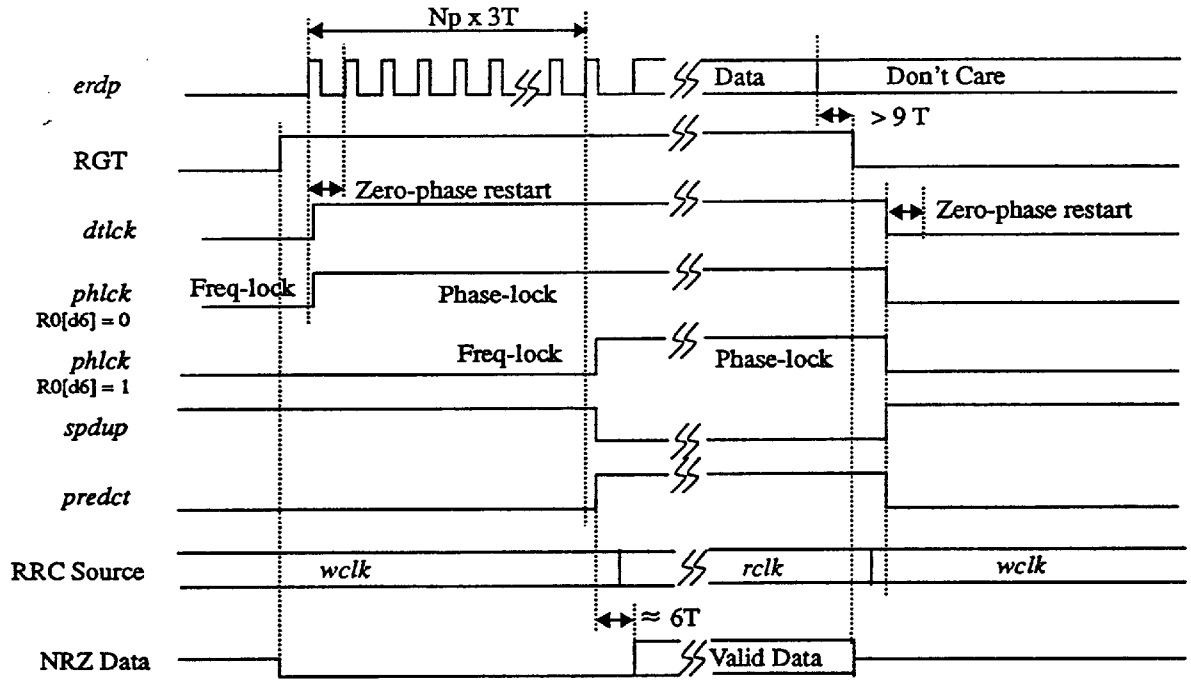

Figure 13. Hard-Sectored Read

Np = Programmable 3T Preamble Length

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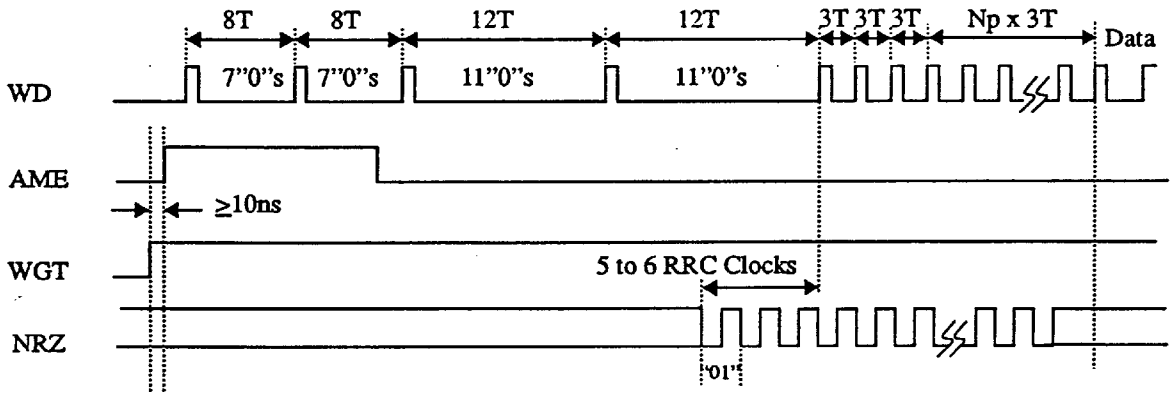

Figure 14. Soft-Sectored Address Mark Write

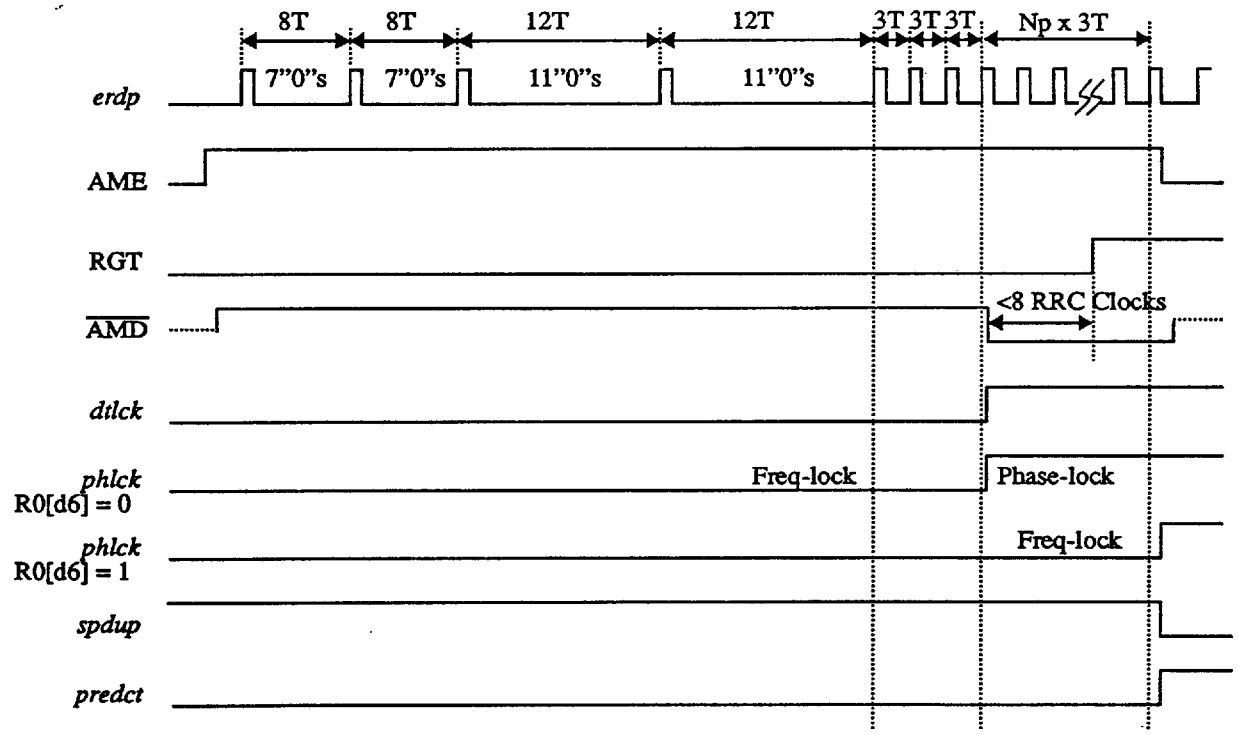

Figure 15. Soft-Sectored Address Mark Read

Np = Programmable 3T Preamble Length

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4.0 Pin Descriptions

4.1 Control

Pin	Name	Description
7	SCLK	Input, Used to clock in serial programming data
6	$\overline{\text{SLOAD}}$	Input, Used to latch serial data to internal registers. Data may be shifted in when $\overline{\text{SLOAD}}$ is low. Data is latched when $\overline{\text{SLOAD}}$ transitions high.
5	SDI	Input, Data is clocked on a low-to-high transition of SCLK.
4	SDO	Output, Used for shifting out programming data stored in internal registers. Data changes on a high-to-low transition of SCLK. Output is high impedance until the high transition of $\overline{\text{SLOAD}}$ occurs after writing to the readback address.
18	RBIAS	External resister connected to ground provides a current reference for internal use. It sets the power dissipation of the chip vs. the maximum data rate, as well as the Frequency Synthesizer charge pump current, Droop rates, Write delays, Kvco, $\overline{\text{ERD}}$ pulse width, AGC response time (see section 5.0).
63	SGT	Input, Active high, Enables servo mode if CEN is active
2	RGT	Input, Active high, Enables read mode if CEN is active
3	WGT	Input, Active high, Enables write mode if CEN is active
51	SEN	Input, Active high, Enables servo track mode if CEN is active
50	RWEN	Input, Active high, Enables read/write power mode if CEN is active
52	PEN	Input, Active high, Enables power to PLL circuits if CEN is active
53	CEN	Input, Active high, A low level places the chip in a low power sleep mode regardless SEN, PEN, or RWEN. A high level combined with SEN, PEN and RWEN places the chip in the other available power modes (see table 1).
39 40	$\overline{\text{P1}}$ $\overline{\text{P2}}$	Programmable outputs

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4.2 AGC

Pin	Name	Description
31 30	AIN AIP	AGC differential signal inputs
28	CAGCS	External capacitor for AGC loop filter used for servo mode
29	CAGCD	External capacitor for AGC loop filter used for data mode
27	VPK	Peak detector output
15	$\overline{\text{HOLD}}$	Input, Active low, Enables AGC hold mode

4.3 Filter

Pin	Name	Description
38 37	FLBP FLBN	Buffered differential signal from filter low-pass outputs. Normally outputs are in an inactive high impedance condition since these outputs are provided primarily for testing of the filter and AGC.
36 35	FDBP FDBN	Buffered differential signal from filter differentiated outputs. Normally outputs are in an inactive high impedance condition since these outputs are provided primarily for testing of the filter.

4.4 Servo

Pin	Name	Description
10 11 12 13	GTA GTB GTC GTD	Input, Active high, Enables servo detectors and selection of detectors
21 22 23 24	SA SB SC SD	Buffered output of servo detectors
14	SRST	Input, Active high, asynchronously resets all peak detectors
19	VRS	Output, Servo low reference voltage (45%VDD)
20	VR	Output, Servo high reference voltage (relative to VRS)

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4.5 Pulse Detector

Pin	Name	Description
26	HYS	Input for setting the hysteresis threshold for pulse amplitude qualification. Must be left floating when not in use.
8	$\overline{ERD}$	Encoded read data output from pulse detector. Falling edge of pulse corresponds to data transition. Output status is controlled by R13[d0].
9	POL	Polarity output of pulse amplitude qualification logic. Output status is controlled by R13[d0].

4.6 Frequency Synthesizer

Pin	Name	Description
57	FREF	External reference clock input to the frequency synthesizer block.
47 46	FSLFP FSLFN	Frequency Synthesizer differential loop filter pins.

4.7 Data Synchronizer

Pin	Name	Description
45	RCP	External resister connected to ground provides a current reference for data PLL charge pump.
43 44	DLF1P DLF1N	Data Synchronizer, differential loop filter 1 pins. Used for setting loop bandwidth. Input to VCO.
42 41	DLF2P DLF2N	Data Synchronizer, differential loop filter 2 pins. Used for setting loop zero frequency.
54	T1 (1)	Test output for: *erdp + T/2 delay* output for Window Centering testing, *rclk + T/2 delay (+/- prog delay)* output for Window Strobe Adjustment (fine) testing, or, *erdp + T/2 delay (+/- T/8 delay)* output for Window Strobe Adjustment (coarse) testing.
55	T2 (1)	Test output for either the *erdp* output or the *rclk* output.
56	T3 (1)	Test output for *wclk* for *rclk*.

(1) See sections 6.9 and 6.14 for additional information.

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4.8 ENDEC

Pin	Name	Description
61	RRC	Read Reference Clock. Output of the ENDEC block, used by the datapath controller as its clock input to read and write data.
62	NRZ	Bidirectional NRZ data. When RGT is inactive and WGT is active, NRZ is an input and data is clocked into the encoder from the datapath controller on the rising edge of RRC. When RGT is active and WGT is inactive, NRZ is an output and NRZ data is clocked out of the decoder into the datapath controller on the falling edge of RRC.
60	AME	Input, active high. Address Mark Enable. Used to enable the soft-sector address mark detection and address mark generation circuitry.
59	$\overline{\text{AMD}}$	Three-state output, active low. Soft-sector Address Mark Detect. Goes to a high impedance state when WGT is high or AME is low. A low level indicates that an address mark has been detected.
58	WD	Output of encoder (write data)

4.9 Power Supply

Pin	Name	Description
64 1	VDD VSS	Digital positive power supply Digital ground
16 17	AVDD1 AVSS1	Analog positive supply Analog ground Used for the Servo and Pulse detector
32 33	AVDD2 AVSS2	Analog positive supply Analog ground Used for the AGC and Filter
25 34	VSUB VSUB	Substrate connections
48 49	AVDD3 AVSS3	Analog positive supply Analog ground Used for the Data Synchronizer and Frequency Synthesizer

Important Note: All VSS-type pins and all VSUB-type pins must be connected together externally using short wide traces to individual PCB thru-holes directly to **one single ground plane.** All VDD-type pins must be connected together externally using short wide traces to individual PCB thru-holes directly to **one single power plane.** All supplies must be decoupled (typically 0.1µF) as close to the device package pins as physically possible with low-inductance trace layout techniques (typically wide, straight, and short).

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5.0 Electrical Characteristics

5.1 Absolute Maximum Ratings (1)

Parameter	Conditions	Min	Nom	Max	Units
Supply Voltage	VDD-VSS	0		7.0	V
Voltage on any input	min relative to VSS max relative to VDD	-0.3		 0.3	V V
Storage temperature		-65		150	°C

(1) Stresses above the Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other condition above those indicated in the operational sections of the specification is not implied.

5.2 Recommended Operating Conditions

Parameter	Conditions	Min	Nom	Max	Units
Supply Voltage	VDD-VSS, IMP62C548	4.5	5.0	5.5	V
Ambient operating temperature		0	25	70	°C

OD Data Rate	Conditions (2)	RBIAS			
		Min	Nom	Max	Units
24 Mbs	IMP62C548-24		2.00		kΩ
32 Mbs	IMP62C548-32		2.00		kΩ
36 Mbs	IMP62C548-36		2.00		kΩ
40 Mbs	IMP62C548-40		2.00		kΩ
48 Mbs	IMP62C548-48		1.67		kΩ

(2) Consult with IMP Applications Engineering regarding the optimization of RBIAS for OD data rates now shown.

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5.3 General

Parameter	Conditions	Min	Nom	Max	Units
Supply Current IMP62C548	VDD = 5.0V, IMP62C548-24 thru 40 RBIAS = 2.00kohm, full output loading,				
	Read/Write mode		132	156	mA
	Servo mode		86	104	mA
	Servo mode w/PLLs		142	178	mA
	Servo mode w/RW		142	178	mA
	Idle mode		9	24	mA
	Idle mode w/PLLs		71	88	mA
	Sleep mode		0.07(1)	6	mA
	VDD = 5.0V, IMP62C548-48 full output loading, RBIAS = 1.75kohm,				
	Read/Write mode		150	180	mA
	Servo mode		95	114	mA
	Servo mode w/PLLs		160	193	mA
	Servo mode w/RW		160	193	mA
	Idle mode		10	25	mA
	Idle mode w/PLLs		80	93	mA
	Sleep mode		0.08(1)	6	mA

(1) Nominal Sleep Mode -- supply current at power-up with no output loading and no FREF clock.

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Parameter	Conditions	Min	Nom	Max	Units
High level input voltage	Digital inputs	2.0			V
Low level input voltage	Digital inputs			0.8	V
High level output voltage	Digital outputs, I_{OH} = -100µA I_{OH} = -2mA	 90% 2.4			 VDD V
Low level output voltage	Digital outputs, I_{OL} = 100µA I_{OL} = 3.2mA			 10% 0.4	 VDD V
Input rise, fall time	Digital inputs			10	ns
Input capacitance	Digital inputs			10	pF
Digital output Fall Time (except $\overline{P1}$, $\overline{P2}$)	2.0V to 0.8V, C_L < 20pF			5	ns
Digital output Rise Time (except $\overline{P1}$, $\overline{P2}$)	0.8V to 2.0V, C_L < 20pF			5	ns
Capacitance loading on RBIAS pin				20	pF
CEN active to SEN active		100			µs
SEN active to Servo frame	SEN inactive > 1ms SEN inactive ≤ 1ms	500 10			µs µs
RWEN active to Data frame	RWEN inactive > 1ms RWEN inactive ≤ 1ms PEN active	150 10 10			µs µs µs
SGT inactive to RGT active	Usage guideline	10			ns
SGT inactive to WGT active	Usage guideline	10			ns
RGT inactive to SGT active	Usage guideline	10			ns
WGT inactive to SGT active	Usage guideline	10			ns
WGT active to AME active	Usage guideline	10			ns

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5.4 AGC

Parameter	Conditions	Min	Nom	Max	Units
Input signal level range	Differential, Gain Stage = 0dB Gain Stage = 6dB	 50 40		 280 140	 mVp-p mVp-p
Input impedance	Differential, WGT inactive WGT active	 4		 100	 kΩ Ω
Input referred noise	BW = 10kHz to 16MHz, Gain Stage = 0dB, Min VGA gain Max VGA gain Gain Stage = 6dB, Min VGA gain Max VGA gain		 769 68 700 65		 μV_{RMS} μV_{RMS} μV_{RMS} μV_{RMS}
Low input impedance hold time tolerance	From WGT falling edge			±20	%
Peak Detector droop time tolerance				±20	%
Gain decay time (Normal)	CAGCS, CAGCD = 1000pF, RBIAS = 2.00kohm, Master droop = 200ns, f = 8MHz, $f_c \geq$ 12MHz, 50% drop in input level to 90% of final gain		7.5	10	µs
Gain attack time (Fast)	CAGCS, CAGCD = 1000pF, RBIAS = 2.00kohm, Master droop = 200ns, f = 8MHz, $f_c \geq$ 12MHz, 200% increase in input level to 110% of final gain		2.5	5	µs
DC erase recovery	CAGCS, CAGCD = 1000pF, RBIAS = 2.00kohm, Master droop = 200ns, f = 8MHz, $f_c \geq$ 12MHz, no signal to maximum input of range to 110% of final gain		3	7.5	µs

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Parameter	Conditions	Min	Nom	Max	Units
AGC gain drift during hold	1 ms			±3	dB
Resistive load on VPK output	R to VRS	2			kΩ
Capacitive load VPK output	C to VSS			25	pF

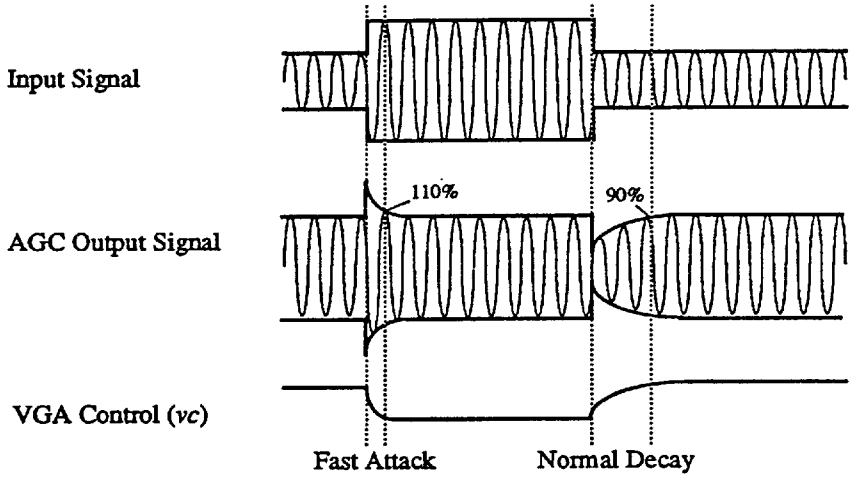

Figure 16. AGC Gain Response

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5.5 Filter

Parameter	Conditions	Min	Nom	Max	Units
Filter unboosted cutoff frequency (f_c) range	-24 -32 -36 -40 -48	3.5 3.5 3.5 4.0 5.0		11.0 14.4 16.0 18.0 21.0	MHz MHz MHz MHz MHz
Filter cutoff frequency accuracy	Read mode Servo mode			± 10 ± 20	% %
fdp, fdn gain	f = 0.67 f_c Relative to LP gain		±0.7	±2	dB
Programmable boost range at f_c		0		12	dB
Boost accuracy	Data mode, Boost setting ≤ 9dB Boost setting > 9dB Servo mode, Boost setting ≤ 9dB Boost setting > 9dB			 ± 1.5 ± 2.0 ± 3.0 ± 4.0	 dB dB dB dB
Output impedance of buffered filter outputs	Differential		60		Ω
Capacitive load on buffered filter outputs	C to VSS			25	pF
Tuning PLL lock capture time	Full range of *wclk* Change in *wclk* of +/-50%			500 100	µs µs

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5.6 AGC + Filter

Parameter	Conditions	Min	Nom	Max	Units
Differential group delay without boost	RGT active, f_c = max, f = f_c /6 to f_c -24, -32, -36 -40, -48			 ±1.2 ±1.0	 ns ns
Differential group delay with full boost	RGT active, f_c = max, f = f_c /6 to f_c -24, -32, -36 -40, -48			 ±1.2 ±1.0	 ns ns
flpp and flpn harmonic distortion	output ≤ $1.5V_{pp\text{-}diff}$ (AGC reference level) No boost, f = 0.67 f_c 2nd harmonic 3rd harmonic			 -30 -30	 dB dB
fdp and fdn harmonic distortion	output ≤ $1.5V_{pp\text{-}diff}$ (AGC reference level) No boost, f = 0.67 f_c 2nd harmonic			 -30	 dB
Gain with fixed AGC gain	VDD = 5.0V, 0dB 6dB		 19 25		 dB dB
Filter output level variation over valid AGC input range	Measured at FLBP/FLBN with AGC recovered and settled for valid input signal range			±0.5	dB
Filter output level	Measured at FLBP/FLBN with AGC enabled		1.35		$V_{pp\text{-}diff}$
Input common-mode rejection	5MHz, differential rejection measured at flpp and flpn to input	50			dB
Power supply rejection	VDD, 5MHz, differential rejection measured at flpp and flpn	35			dB
Settling time from switching between servo and data modes	Usage guideline, data to servo servo to data			 1 1	 µs µs

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5.7 Servo

Parameter	Conditions	Min	Nom	Max	Units
Full-scale level on SA, SB, SC & SD outputs	AGC enabled, Relative to VRS		1		V
Amplitude mismatch between servo outputs	50% full scale			±30	mV
Non-linearity	Input range $^{1}/_{10}$ to $^{9}/_{10}$ of full scale			±3	%
Minimum time between GTx pulses (t_{gap})		20			ns
Slew rate of A, B, C & D detectors	RBIAS = 2.00kohm RBIAS = 1.75kohm		3.2 3.7		mV/ns mV/ns
Droop rate of A, B, C & D detectors				±5	V/s
Minimum width of SRST pulse (t_{srst})		200			ns
Capacitive load on SA, SB, SC & SD outputs	C to VSS			50	pF
vrh reference voltage	Relative to VRS		375		mV
Servo signal reference at the VRS pin.		40%	45%	50%	VDD
Reference at the VR pin.	Relative to VRS	.95	1	1.05	V
Resistive load on VR output	R to VRS	2			kΩ
Capacitive load VRS & VR outputs	C to VSS			50	pF

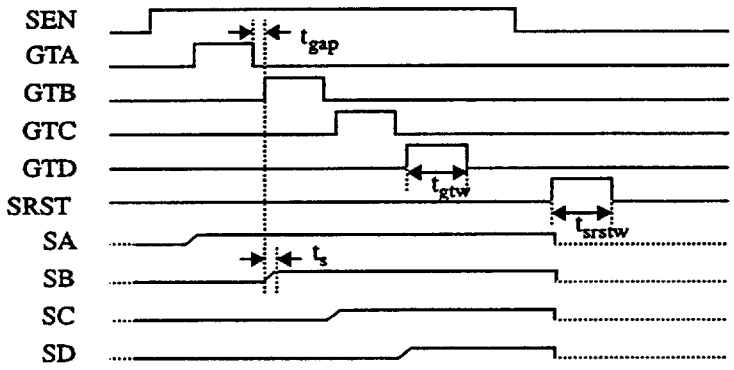

Figure 17. Servo Waveforms

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5.8 Pulse Detector

Parameter	Conditions	Min	Nom	Max	Units
$\overline{ERD}$ pulse width	Pulse width @ 0.4V, C_L < 15pF, RBIAS = 2.00kohm		15	20	ns
Programmable hysteresis accuracy	See section 6.7			±1.6	%
Combined effect of pulse pairing and ERD jitter	Sine wave input, f = 15MHz @ 90mV_{pp}, f_c = 18MHz, AGC fixed gain = 6dB, 1 sigma			±600	ps

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5.9 Frequency Synthesizer

Parameter	Conditions	Min	Nom	Max	Units
Encoded data write frequency, *wclk*	-24 -32 -36 -40 -48	15 15 17 19 23		36 48 54 60 72	MHz MHz MHz MHz MHz
Reference frequency, FREF		0.13		48	MHz
Programmable divisors, M and N	M and N	2		128	
VCO center frequency accuracy				±25	%
Charge pump current	RBIAS = 2.00kΩ RBIAS = 1.75kΩ		0.5 0.57		mA mA
Charge pump leakage				±100	nA
VCO gain constant (K_{VCO})	RBIAS = 2.00kΩ RBIAS = 1.75kΩ		10.5 12.0		MHz/V MHz/V

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5.10 Data Synchronizer

Parameter	Conditions	Min	Nom	Max	Units
Window shift / Tvco[1] Range			±27.5		%
Window shift resolution/ Tvco			1		%
Window centering accuracy	Average of window early and window late, Fixed shift mode		±.5		ns
Window width loss	3 sigma confidence		.75	1.05	ns
RGT low timing width	Split sector operation	TBD			ns
Charge Pump current	With maximum user setting of K_S, K_G RCP = 2.00kΩ, Measured at DLF1 Measured at DLF2		0.313 0.938		mA mA
Charge pump leakage				±100	nA
VCO gain constant (K_{VCO})	RBIAS = 2.00kΩ RBIAS = 1.75kΩ		3.2 3.7		MHz/V MHz/V
VCO frequency range	RBIAS = 2.00kΩ RBIAS = 1.75kΩ	18 21		63 74	MHz MHz
f_{CTR} / *wclk* [2]		0.95	1.0	1.05	
VCO restart error	First *erdp* pulse edge after *dtlck* transition			±3	ns
Capacitance loading on RCP pin				20	pF
Voltage at RCP pin			1.25		V

[1] Tvco is the period of the VCO used to reference the delay line.

[2] f_{CTR} is the center frequency of the Data Synchronizer's VCO.

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5.11 ENDEC

Parameter	Conditions	Min	Nom	Max	Units
RRC duty cycle		40		60	%
NRZ input set up time before rising edge of RRC	RGT inactive			3	ns
NRZ input hold time after rising edge of RRC	RGT inactive	3			ns
NRZ output delay relative to RRC falling edge	RGT active	-5		5	ns
WD jitter	*wclk* = 36MHz, 1 sigma, M=16 M=32 M=64 M=128		 90 125 175 240		 ps ps ps ps

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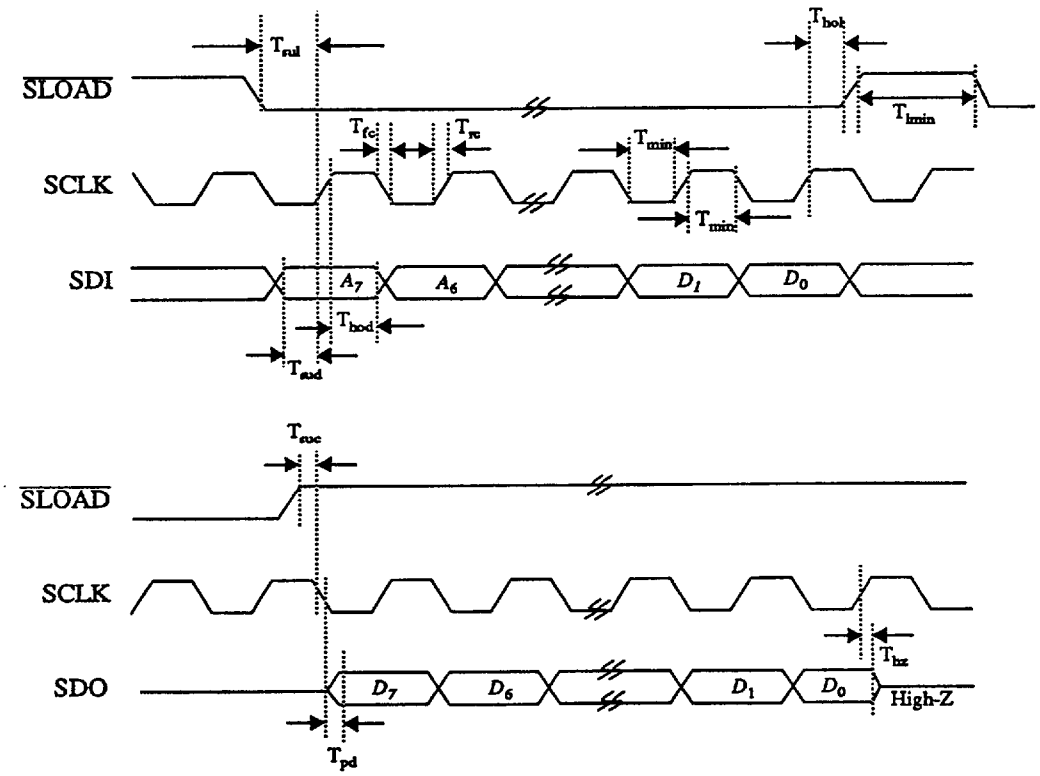
5.12 Serial Interface Timing



Note: All parameters are specified at V_{IH} min. and V_{IL} max.

Figure 18. Serial Interface Timing Diagram

Parameter	Conditions	Min	Max	Units
T_{sul}	$\overline{SLOAD}$ setup time to SCLK	15		ns
T_{hol}	$\overline{SLOAD}$ hold time after SCLK	30		ns
T_{rc}	SCLK rise time		10	ns
T_{fc}	SCLK fall time		10	ns
T_{min}	SCLK high time and low time	25		ns
T_{sud}	SDI setup time to SCLK	15		ns
T_{hod}	SDI hold time after SCLK	10		ns
T_{suc}	$\overline{SLOAD}$ high to SCLK falling edge	40		ns
T_{lmin}	$\overline{SLOAD}$ high time	50		ns
T_{pd}	SDO delay		30	ns
T_{hz}	SDO hold time after SCLK	0		ns

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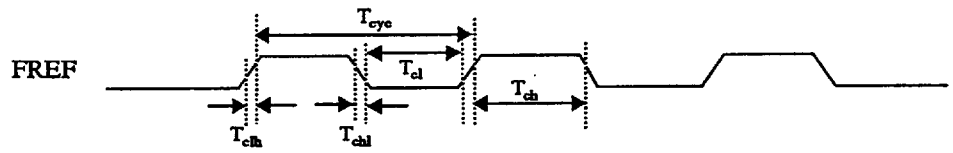
5.13 Control Timing



Note: All parameters are specified at VIH min. and VIL max.

Figure 19. FREF Timing Diagram

Parameter	Conditions	Min	Max	Units
T_{clh}	FREF rise time		10	ns
T_{chl}	FREF fall time		10	ns
T_{ch}	FREF high time	5		ns
T_{cl}	FREF low time	5		ns
T_{cye}	FREF cycle time	20		ns

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6.0 Programming

6.1 Registers

Register	Address	Function	Bits	Default[1]
0	0000 0000	Mode Control	7	0000 0000
1	0000 0001	AGC Control	4	0000 0000
2	0000 0010	Filter Control	3	0000 0000
3	0000 0011	Filter Frequency Scaling Ratio (*FSR*)	4	0000 0010
4	0000 0100	Filter Pulse-Slimming Boost for Data Mode (ω_{za}, ω_{zb})	8	0000 0000
5	0000 0101	Data Mode Hysteresis/Droop	8	1110 1111
6	0000 0110	Servo Mode Hysteresis/Droop	8	1110 1111
7	0000 0111	Filter Pulse-Slimming Boost for Servo Mode (ω_{za}, ω_{zb})	8	0000 0000
8	0000 1000	PLL Loop Filter BW	6	0000 1111
9	0000 1001	PLL Window Adjustment	8	0100 0000
10	0000 1010	Frequency Synthesis Num (M)	7	0000 0001
11	0000 1011	Frequency Synthesis Den (N)	7	0000 0001
12	0000 1100	Frequency Synthesis VCO Center Frequency (f_{CTR})	5	0001 1111
13	0000 1101	Auxiliary Control	5	0000 0000
14	0000 1110	Test	8	0000 0000
15	0000 1111	Readback	n/a	n/a

[1] Power-on-reset forced setting. Underline indicates active bits used.

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6.2 Mode Control (Address 0)

d3 RWEN	d2 PEN	d1 SEN	d0 CEN	Mode
0	0	0	0	Sleep *(default)*
0	0	0	1	Idle
0	0	1	1	Servo read
0	1	0	1	Idle with PLLs active
0	1	1	1	Servo read with PLLs active
1	X	0	1	Read/Write
1	X	1	1	Servo with Read/Write circuitry active

d4	Hysteresis Reference Selection *(hysref)*
0	*vrh* internal reference *(default)*.
1	HYS pin.

d5	ENDEC Operation *(edbp)*
0	Normal ENDEC operation *(default)*.
1	ENDEC bypass.

d6	PLL Mode
0	Phase-lock to data during sychronization *(default)*.
1	Frequency-lock to data during sychronization.

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6.3 AGC Control (Address 1)

d0	Gain Stage
0	0dB *(default)*
1	6dB

d1	AGC Operation
0	Normal AGC operating mode *(default)*.
1	Disable AGC mode and fix VGA gain.

d3	d2	WGT Delay	
		RBIAS = 2.00kΩ	RBIAS = 1.75kΩ
0	0	1.0µs *(default)*	0.9µs *(default)*
0	1	1.8µs	1.6µs
1	0	3.3µs	2.9µs
1	1	6.0µs	5.3µs

6.4 Filter Control (Address 2)

d2	d1	d0	Cutoff Frequency Coarse Tuning
0	0	0	Filter coarse tuning enabled always *(default)*.
0	0	1	Filter coarse tuning disabled always.
0	1	0	Filter coarse tuning disabled when RGT is active *(preferred usage mode; consult with IMP Applications Engineering)*.
1	X	X	Servo-tuning mode enabled, coarse tuning is enabled.
0	X	X	Servo-tuning mode disabled.

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6.5 Filter Frequency Scaling Ratio (Address 3)

d3	d2	d1	d0	Cutoff Frequency
0	0	0	0	0.396 *wclk*
0	0	0	1	0.352 *wclk*
0	0	1	0	0.316 *wclk (default)*
0	0	1	1	0.288 *wclk*
0	1	0	0	0.264 *wclk*
0	1	0	1	0.243 *wclk*
0	1	1	0	0.226 *wclk*
0	1	1	1	0.211 *wclk*
1	0	0	0	0.199 *wclk*
1	0	0	1	0.176 *wclk*
1	0	1	0	0.159 *wclk*
1	0	1	1	0.144 *wclk*
1	1	0	0	0.132 *wclk*
1	1	0	1	0.122 *wclk*
1	1	1	0	0.113 *wclk*
1	1	1	1	0.105 *wclk*

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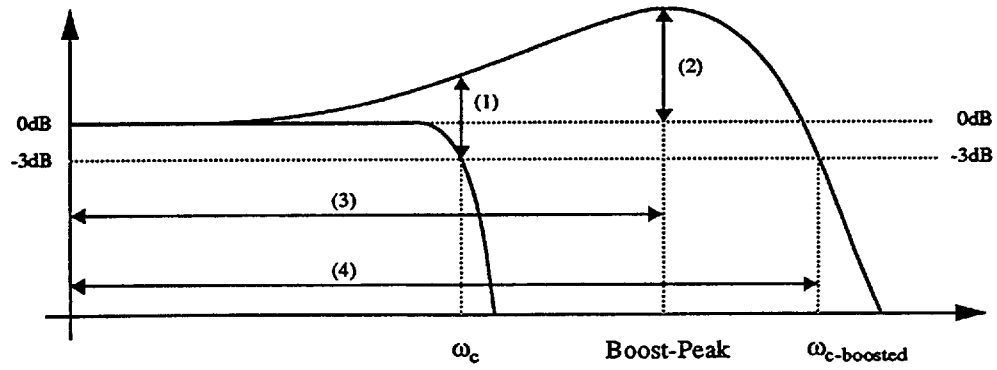
6.6 Filter Pulse-Slimming Boost For Data Mode (Address 4)
Filter Pulse-Slimming Boost For Servo Mode (Address 7)

d3	d2	d1	d0	ω_{za}	Boost at ω_{-3dB} (1)	Boost at Peak (2)	Boost-Peak Freq. (3)	Boosted ω_{-3dB} (4)
d7	d6	d5	d4	ω_{zb}				
0	0	0	0	∞	0 *(default)*			1.00 ω_c
0	0	0	1	8.70 ω_c	0.11 dB			1.03 ω_c
0	0	1	0	4.35 ω_c	0.45 dB			1.08 ω_c
0	0	1	1	2.90 ω_c	0.98 dB			1.20 ω_c
0	1	0	0	2.18 ω_c	1.67 dB			1.38 ω_c
0	1	0	1	1.74 ω_c	2.48 dB			1.63 ω_c
0	1	1	0	1.45 ω_c	3.38 dB	0.41 dB	0.87 ω_c	1.85 ω_c
0	1	1	1	1.24 ω_c	4.34 dB	1.37 dB	1.10 ω_c	2.03 ω_c
1	0	0	0	1.09 ω_c	5.32 dB	2.53 dB	1.23 ω_c	2.16 ω_c
1	0	0	1	0.97 ω_c	6.32 dB	3.77 dB	1.31 ω_c	2.28 ω_c
1	0	1	0	0.87 ω_c	7.31 dB	5.01 dB	1.36 ω_c	2.38 ω_c
1	0	1	1	0.79 ω_c	8.29 dB	6.23 dB	1.41 ω_c	2.47 ω_c
1	1	0	0	0.73 ω_c	9.26 dB	7.40 dB	1.42 ω_c	2.56 ω_c
1	1	0	1	0.67 ω_c	10.19 dB	8.53 dB	1.45 ω_c	2.64 ω_c
1	1	1	0	0.62 ω_c	11.10 dB	9.61 dB	1.48 ω_c	2.72 ω_c
1	1	1	1	0.58 ω_c	11.98 dB	10.64 dB	1.50 ω_c	2.80 ω_c

(1) Symmetrical boost. Boost values are relative to the -3dB frequency, ω_c.
(2) Boost at Peak values are relative to 0dB.
(3) Boost-Peak frequency values are relative to the -3dB frequency, ω_c.
(4) Boosted -3dB frequency, $\omega_{c\text{-boosted}}$, relative to the unboosted -3dB frequency, ω_c.



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6.7 Data Mode Hysteresis/Droop (Address 5)
Servo Mode Hysteresis/Droop (Address 6)

d4	d3	d2	d1	d0	Threshold Voltage V_{TH} [V] (2)	Percent Threshold Level $\%_{TH}$ [%] (4)
0	0	0	0	0	0% V_H (3)	$\%_{TH} = [x\%](4V_H / V_{pp\text{-}diff})$
0	0	0	0	1	6.1% V_H	
0	0	0	1	0	9.1% V_H	
0	0	0	1	1	12.1% V_H	
D_{HD} (1)					$V_{TH} = [x\%]\ V_H = [((D_{HD}+1) / 0.33)\%]\ V_H$	
1	1	1	0	0	87.9% V_H	
1	1	1	0	1	90.9% V_H	
1	1	1	1	0	93.9% V_H	
1	1	1	1	1	97.0% V_H	

(1) D_{HD} is the binary value of the register (default = 48.5%).

(2) Absolute threshold voltage derived from reference voltage.

(3) V_H is either the voltage on the HYS pin, or the internal fixed reference *vrh*, depending on R0[d4] (see section 6.2).

(4) Threshold level relative to the filter output amplitude $V_{pp\text{-}diff}$. Typically *vrh* = 375mV (see section 5.7), and $V_{pp\text{-}diff}$ = 1.35V (see section 5.6).

d7	d6	d5	AGC Master Peak Detector Droop(5)	
			RBIAS = 2.00kΩ	RBIAS = 1.75kΩ
0	0	0	200ns	175ns
0	0	1	258ns	226ns
0	1	0	334ns	292ns
0	1	1	431ns	377ns
1	0	0	557ns	487ns
1	0	1	719ns	629ns
1	1	0	929ns	813ns
1	1	1	1200ns *(default)*	1050ns *(default)*

(5) Droop is defined as the nominal time for VPK to hold the peak of an isolated pulse before resetting.

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6.8 PLL Loop Filter Bandwidth (Address 8)

d3	d2	d1	d0	K_G Programmable Charge Pump Gain Multiplier
0	0	0	0	1.000
0	0	0	1	1.067
0	0	1	0	1.133
0	0	1	1	1.200
0	1	0	0	1.267
0	1	0	1	1.333
0	1	1	0	1.400
0	1	1	1	1.467
1	0	0	0	1.533
1	0	0	1	1.600
1	0	1	0	1.667
1	0	1	1	1.733
1	1	0	0	1.800
1	1	0	1	1.867
1	1	1	0	1.933
1	1	1	1	2.000 *(default)*

d5	d4	K_S Programmable Charge Pump Gain Multiplier for Acquisition
0	0	1 *(default)*
0	1	1.5
1	0	2
1	1	Reserved, do not use.

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6.9 PLL Window Adjustment (Address 9)

d5 sign	d4 range	d3	d2	d1	d0	Window Adjustment as a Percentage of the Window (1)
0	0	0	0	0	0	+0% (adjustment bypassed - *default*) (*syncdata* mux'd from Pulse Gate)
1	0	0	0	0	0	-0% (+/- prog delay; fine adjust) (*syncdata* mux'd from Data Align)
0/1	0	0	0	0	1	+/-1% (+ = data late; - = data early)
0/1	0	0	0	1	0	+/-2%
0/1	0	0	0	1	1	+/-3%
0/1	0	0	1	0	0	+/-4%
0/1	0	0	1	0	1	+/-5%
0/1	0	0	1	1	0	+/-6%
0/1	0	0	1	1	1	+/-7%
0/1	0	1	0	0	0	+/-8%
0/1	0	1	0	0	1	+/-9%
0/1	0	1	0	1	0	+/-10%
0/1	0	1	0	1	1	+/-11%
0/1	0	1	1	0	0	+/-12%
0/1	0	1	1	0	1	+/-13%
0/1	0	1	1	1	0	+/-14%
0/1	0	1	1	1	1	+/-15%
0/1	1	0	0	0	0	+/-12.5% (+/- T/8; coarse adjust)
0/1	1	0	0	0	1	+/-13.5%
0/1	1	0	0	1	0	+/-14.5%
0/1	1	0	0	1	1	+/-15.5%
0/1	1	0	1	0	0	+/-16.5%
0/1	1	0	1	0	1	+/-17.5%
0/1	1	0	1	1	0	+/-18.5%
0/1	1	0	1	1	1	+/-19.5%
0/1	1	1	0	0	0	+/-20.5%
0/1	1	1	0	0	1	+/-21.5%
0/1	1	1	0	1	0	+/-22.5%
0/1	1	1	0	1	1	+/-23.5%
0/1	1	1	1	0	0	+/-24.5%
0/1	1	1	1	0	1	+/-25.5%
0/1	1	1	1	1	0	+/-26.5%
0/1	1	1	1	1	1	+/-27.5%

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(1) **Test Port**

Test Status	Conditions	T1 (54)	T2 (55)	T3 (56)
Outputs OFF, & ENDEC enabled	R0[d5] = 0 R14[d5] = 0	Low	Low	High
Outputs ON, & WGT active	R14[d5] = 1			*wclk*
Window Centering (RGT active)	R9[d5:d0] = all zeros R14[d5] = 1	*erdp + T/2 delay*	*erdp*	*rclk*
Window Strobe-Fine Adjust (RGT active)	R9[d5,d3,d2,d1,d0] = non-zero R9[d4] = 0 R14[d5] = 1	*rclk + T/2 (+/- prog delay)*	*rclk*	*rclk*
Window Strobe-Coarse Adjust (RGT active)	R9[d5, d3,d2,d1,d0] = non-zero R9[d4] = 1 R14[d5] = 1	*erdp + T/2 delay (+/- T/8)*	*erdp*	*rclk*

d7	d6	**Preamble Detection Length -- Np (number of 3T patterns in preamble; loop gain is K_S)**
0	0	8
0	1	12 *(default)*
1	0	16
1	1	20

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6.10 Frequency Synthesizer Numerator (Address 10)

d6	d5	d4	d3	d2	d1	d0	M
0	0	0	0	0	0	0	Not allowed
0	0	0	0	0	0	1	2 *(default)*
0	0	0	0	0	1	0	3
D_M[1]							D_M+1
1	1	1	1	1	1	1	128

[1] D_M is the binary value of the register.

6.11 Frequency Synthesizer Denominator (Address 11)

d6	d5	d4	d3	d2	d1	d0	N
0	0	0	0	0	0	0	Not allowed
0	0	0	0	0	0	1	2 *(default)*
0	0	0	0	0	1	0	3
D_N[2]							D_N+1
1	1	1	1	1	1	1	128

[2] D_N is the binary value of the register.

6.12 Frequency Synthesizer VCO Center Frequency (Address 12)

d4	d3	d2	d1	d0	Target f_{CTR} of VCO [3]		
						RBIAS = 2.00kΩ	RBIAS = 1.75kΩ
0	0	0	0	0		18.8MHz	22.5MHz
0	0	0	0	1		20.1MHz	24.1MHz
0	0	0	1	0		21.4MHz	25.7MHz
D_{fc}					$(f_{CTR\text{-}min} + (D_{fc} * (f_{CTR\text{-}max} - f_{CTR\text{-}min}) / 31))$MHz		
1	1	1	1	1		60.0MHz *(def)*	72.0MHz *(def)*

[3] f_{CTR} is approximately equal to *wclk*.

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6.13 Auxiliary Control (Address 13)

d0	Pulse Detector Outputs
0	Enables $\overline{ERD}$ and POL outputs only when SGT is active (*default*).
1	Enables $\overline{ERD}$ and POL outputs continuously.

d1	Servo Qualification Mode
0	Enable both polarity and threshold qualification (*default*).
1	Disable polarity qualification; threshold qualification only.

d4	Impedance Switch
0	Has no effect on the impedance switch (*default*).
1	Causes the impedance switch to be turned on upon writing to register 13. The time equals the WGT delay set in R1[d3, d2].

d7	d6	$\overline{P1}$ and $\overline{P2}$ Digital Outputs
X	0	$\overline{P1} = 1$ (*default*)
X	1	$\overline{P1} = 0$
0	X	$\overline{P2} = 1$ (*default*)
1	X	$\overline{P2} = 0$

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6.14 Test (Address 14)

d3 Buffer I/O	d2 Buffer Enable	d1 Filter Bypass	d0 AGC Bypass	Operation
0	0	0	0	Normal operation. *(default)*
0	X	X	1	AGC bypassed.
0	X	1	X	Filter bypassed.
0	1	X	X	Enable buffer power-up of the filter LP and DIFF outputs.
0	1	1	1	AIN and AIP pin inputs are multiplexed to both the LP and DIFF output buffers for calibrating measurement equipment. Power-up of buffers at the filter LP and DIFF outputs are enabled.
1	X	X	X	Buffers on the filter LP and DIFF outputs are powered down and these pins are now used as inputs to the pulse detector and servo.

d4	Operation
0	Normal operation *(default)*.
1	The $\overline{\text{ERD}}$ buffer goes high impedance and the $\overline{\text{ERD}}$ pin then used as an external digital input to the data synchronizer for test purposes.

d5	Operation
0	Test Port disabled. T1, T2 outputs forced low, T3 forced high *(default)*.
1	Test Port enabled. T1, T2, T3 outputs enabled. To observe *wclk* on T3, WGT must be active. To observe *rclk* on T3, RGT must be active.

d7	d6	Data Synchronizer Operation	Frequency Synthesizer Operation
0	0	Normal operation *(default)*.	Normal operation *(default)*.
0	1	Programmable charge pump static +Iout test mode with speedup.	Charge pump static +Iout test mode. Counter M input is switched to FREF and output is switched to T3 pin.
1	0	Programmable charge pump static -Iout test mode with speedup.	Charge pump static -Iout test mode. Counter N input is FREF and output is switched to T3 pin.
1	1	Programmable charge pump disable for static leakage test.	Charge pump disable for static leakage test.

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6.15 Readback (Address 15)

Data	Function
0000 0000	Mode Control
0000 0001	AGC Control
0000 0010	Filter Control
0000 0011	Filter Frequency Scaling Ratio (*FSR*)
0000 0100	Filter Pulse-Slimming Boost for Data Mode (ω_{za}, ω_{zb})
0000 0101	Data Mode Hysteresis/Droop
0000 0110	Servo Mode Hysteresis/Droop
0000 0111	Filter Pulse-Slimming Boost for Servo Mode (ω_{za}, ω_{zb})
0000 1000	PLL Loop Filter BW
0000 1001	PLL Window Adjustment
0000 1010	Frequency Synthesis Num (M)
0000 1011	Frequency Synthesis Den (N)
0000 1100	Frequency Synthesis VCO Center Frequency (f_{CTR})
0000 1101	Auxiliary Control
0000 1110	Test
0000 1111	Readback

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7.0 Package

64 pin TQFP

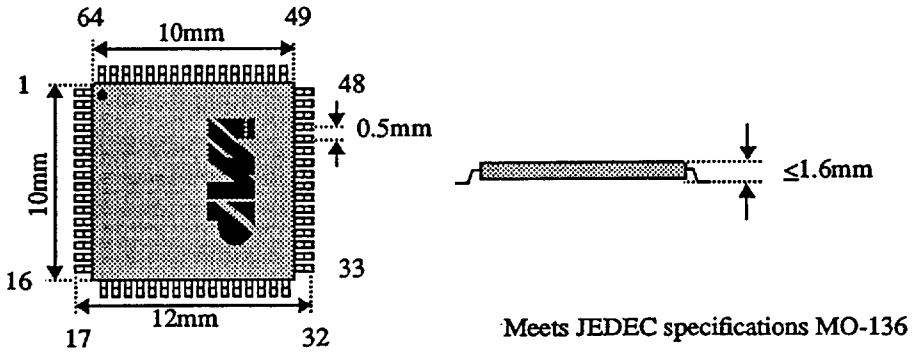

Figure 20. Package Diagram

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8.0 Application Configuration

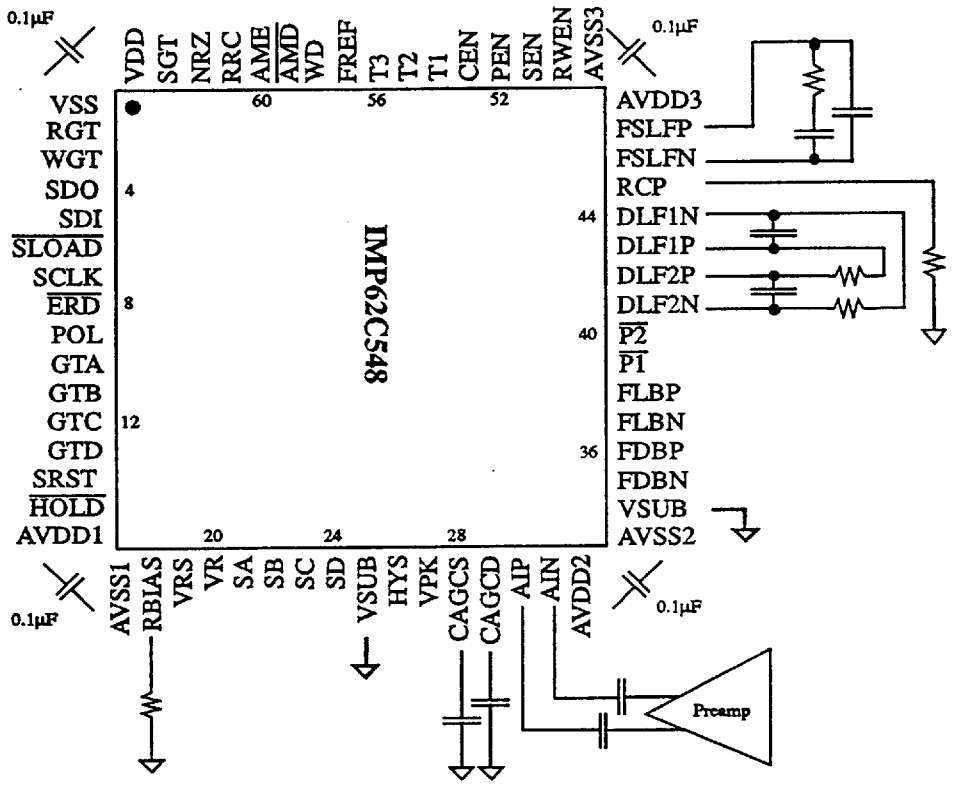

Figure 21. Pinout and Typical External Components

The HYS pin *(an analog input)* must float if not used.
All unused digital input pins must be tied to an appropriate high or low level.

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