



## N-Channel 30-V (D-S) 175°C MOSFET

### PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ ( $\Omega$ )	$I_D$ (A)
30	0.016 @ $V_{GS} = 10$ V	55
	0.024 @ $V_{GS} = 4.5$ V	45

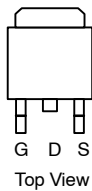
### FEATURES

- TrenchFET® Power MOSFET
- 175°C Junction Temperature
- PWM Optimized
- 100%  $R_g$  Tested

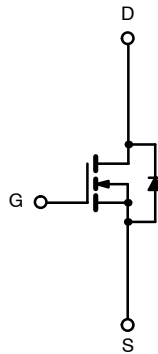
### APPLICATIONS

- High-Side Core DC/DC
  - Desktop
  - Server
- DDR DC/DC Converter

TO-263



DRAIN connected to TAB



Ordering Information: SUM55N03-16P—E3 (Lead Free)

N-Channel MOSFET

### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	30	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	
Continuous Drain Current ( $T_J = 175^\circ\text{C}$ )	$I_D$	$T_C = 25^\circ\text{C}$	55
		$T_C = 100^\circ\text{C}$	39
Pulsed Drain Current	$I_{DM}$	50	A
Avalanche Current	$I_{AR}$	25	
Repetitive Avalanche Energy <sup>a</sup>	$E_{AR}$	31.25	mJ
Maximum Power Dissipation <sup>a</sup>	$P_D$	$T_C = 25^\circ\text{C}$	93 <sup>b</sup>
		$T_A = 25^\circ\text{C}$ <sup>d</sup>	3.75
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to 175	$^\circ\text{C}$

### THERMAL RESISTANCE RATINGS

Parameter	Symbol	Limit	Unit
Junction-to-Ambient	$R_{thJA}$	40	$^\circ\text{C/W}$
Junction-to-Case	$R_{thJC}$	1.6	

Notes

- Duty cycle  $\leq 1\%$ .
- See SOA curve for voltage derating.
- When mounted on 1" square PCB (FR-4 material).

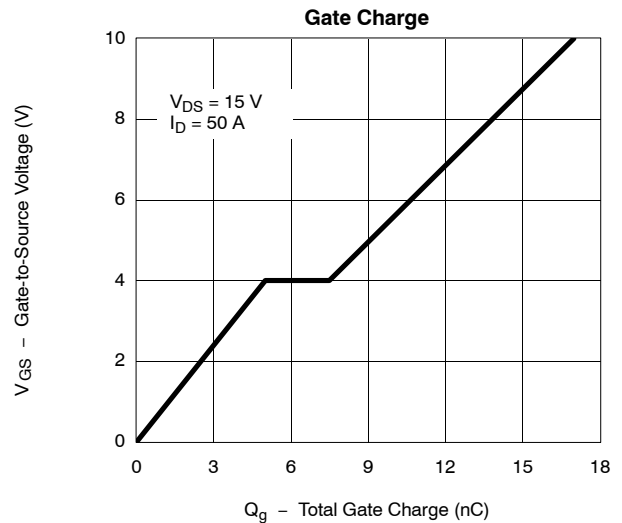
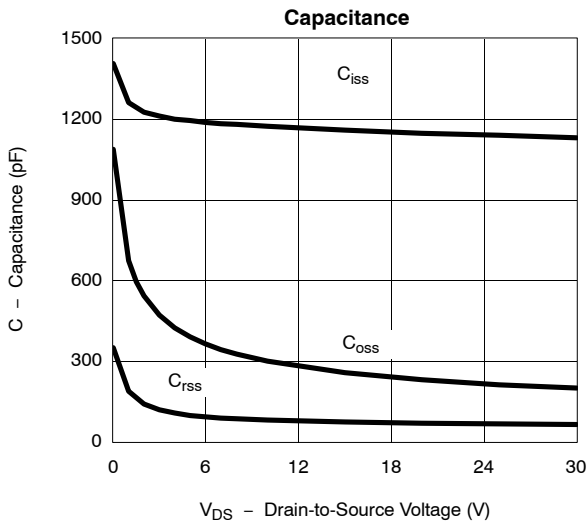
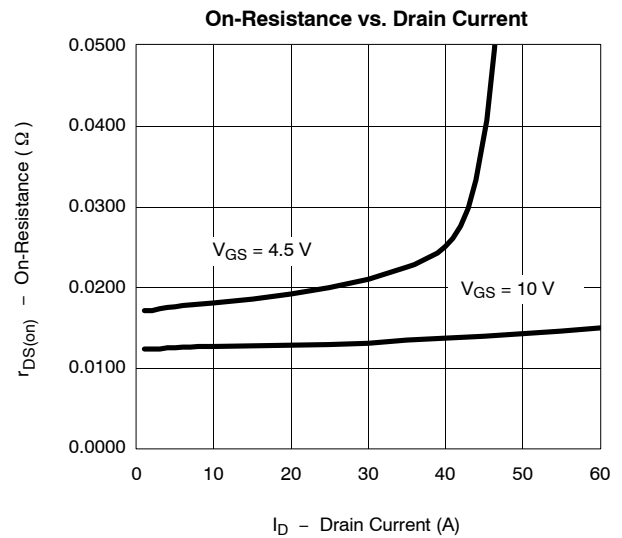
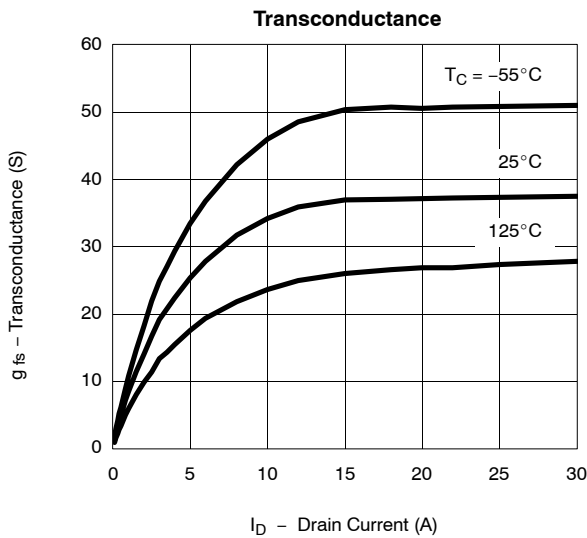
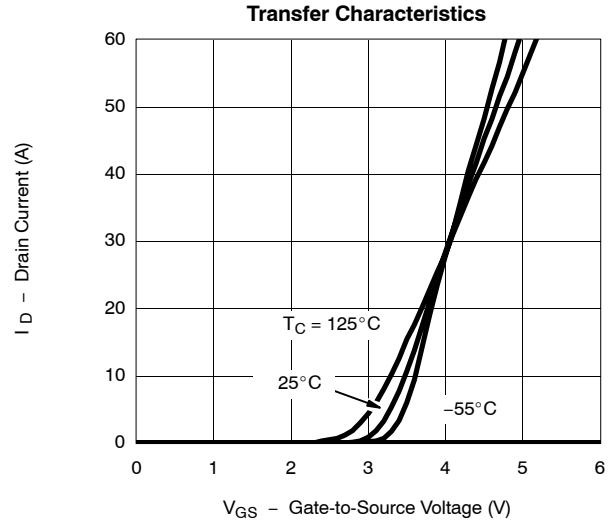
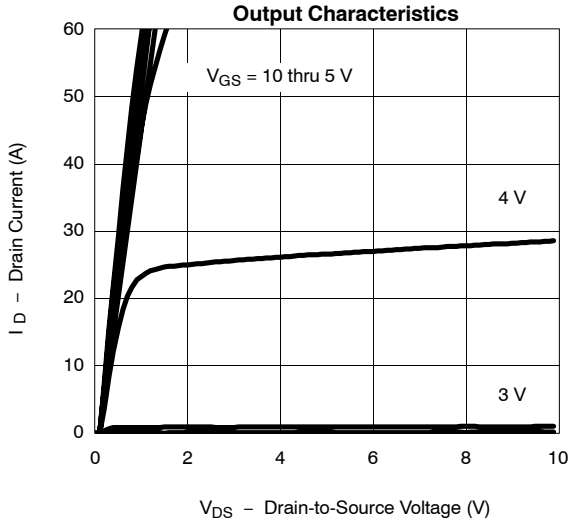
SPECIFICATIONS (T <sub>J</sub> = 25 °C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>DS</sub> = 0 V, I <sub>D</sub> = 250 μA	30			V
Gate-Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	1		3	
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V			1	μA
		V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C			50	
		V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 175 °C			250	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≥ 5 V, V <sub>GS</sub> = 10 V	50			A
Drain-Source On-State Resistance <sup>a</sup>	r <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 15 A		0.0128	0.016	Ω
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 15 A, T <sub>J</sub> = 125 °C			0.025	
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 15 A, T <sub>J</sub> = 175 °C			0.031	
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 10 A		0.019	0.024	
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 20 A	10			S
<b>Dynamic<sup>b</sup></b>						
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 25 V, f = 1 MHz		1150		pF
Output Capacitance	C <sub>oss</sub>			215		
Reverse Transfer Capacitance	C <sub>rss</sub>			70		
Total Gate Charge <sup>b</sup>	Q <sub>g</sub>	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 50 A		17	26	nC
Gate-Source Charge <sup>b</sup>	Q <sub>gs</sub>			5		
Gate-Drain Charge <sup>b</sup>	Q <sub>gd</sub>			2.5		
Gate Resistance	R <sub>g</sub>		2.7	5.5	8.25	Ω
Turn-On Delay Time <sup>b</sup>	t <sub>d(on)</sub>	V <sub>DD</sub> = 15 V, R <sub>L</sub> = 0.3 Ω I <sub>D</sub> ≅ 50 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 2.5 Ω		7	15	ns
Rise Time <sup>b</sup>	t <sub>r</sub>			20	30	
Turn-Off Delay Time <sup>b</sup>	t <sub>d(off)</sub>			25	40	
Fall Time <sup>b</sup>	t <sub>f</sub>			12	20	
<b>Source-Drain Diode Ratings and Characteristics (T<sub>C</sub> = 25 °C)<sup>c</sup></b>						
Continuous Current	I <sub>S</sub>				55	A
Pulsed Current	I <sub>SM</sub>				50	
Forward Voltage <sup>a</sup>	V <sub>SD</sub>	I <sub>F</sub> = 20 A, V <sub>GS</sub> = 0 V		1.0	1.5	V
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 40 A, di/dt = 100 A/μs		25	70	ns
Peak Reverse Recovery Current	I <sub>RM</sub>			1.2	2.5	A
Reverse Recovery Charge	Q <sub>rr</sub>			0.15	0.09	μC

Notes

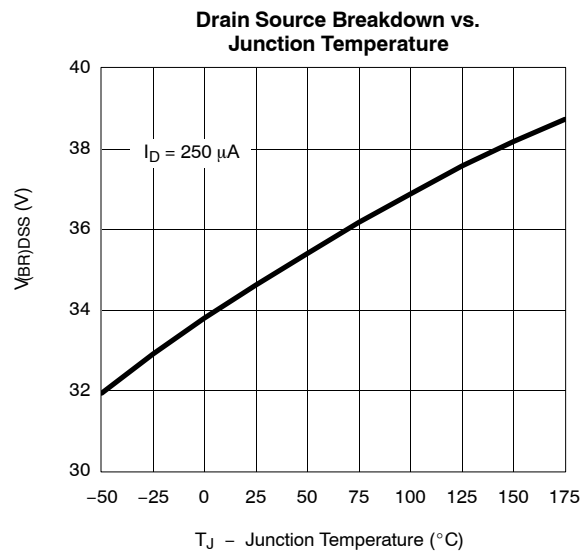
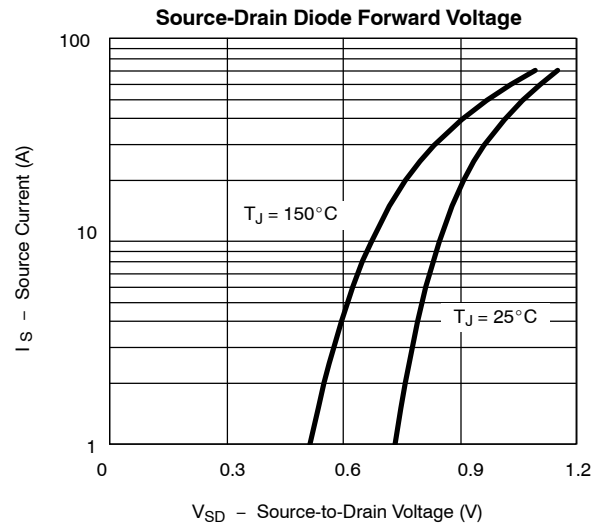
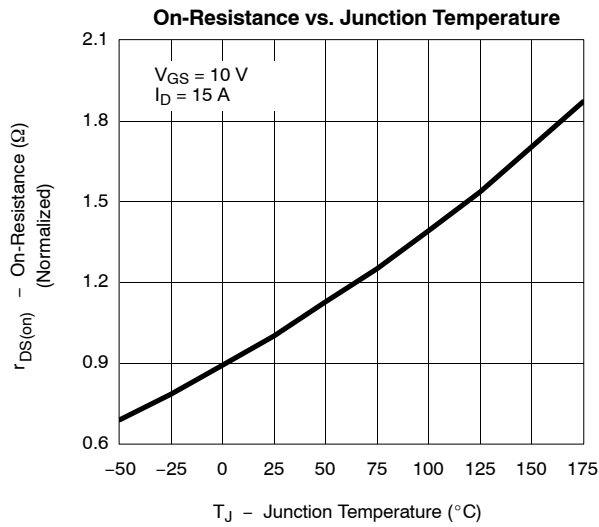
- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- b. Independent of operating temperature.
- c. Guaranteed by design, not subject to production testing.



**TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)**



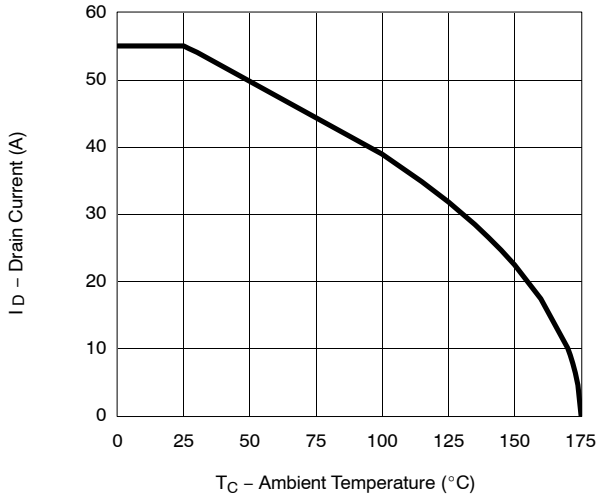
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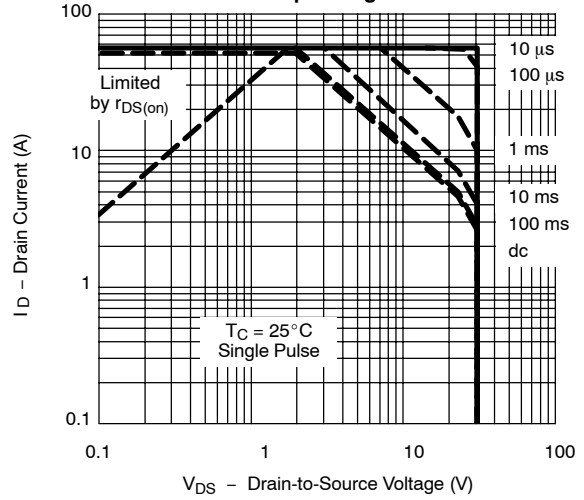


**THERMAL RATINGS**

Maximum Avalanche and Drain Current vs. Case Temperature



Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case

