SAA8122A

Digital Still Camera Processor (ImagIC family)

Rev. 01 — 20 April 2000 **Objective specification**

1. Description

The DSC SAA8122A is a high performance, low power, single-chip Million Instructions Per Second (MIPS) based signal processor, part of the ImagIC family, which is dedicated to image processing, compression, formatting and storage. The DSC SAA8122A is optimized for use with Philips range of CCDs (e.g: FXA1022, 2 Mpixels CCD), V-driver (TDA9991), CDS/PGA/ADC (TDA9952), allowing easy implementation of a complete system solution and fast development of high performance consumer digital still cameras.

The SAA8122A is designed as a single-chip device, able to perform all treatments and connections required for a wide range of Digital Still Cameras. Its embedded RISC CPU, for which the development environment is available, enables shorter development and validation cycles, as well as faster feature upgrade. Since one of the main objectives of the SAA8122A is addressing a wide range of CCD sensors, a DSP (with advanced embedded algorithm) for camera signal processing is integrated with a high level of programmability for pulses generation.

The JPEG core is hardware based in order to allow high-speed image data compression.

2. Features

2.1 General

- Supports a wide range of progressive CCDs (VGA, SVGA, QGA, XGA, EQGA), with RGB Bayer filters up to 2 Mpixels
- Performs an advanced RGB to YUV conversion
- Includes a smart measurement unit to speed up the control loop (focus, auto white balance, etc.)
- Supports a wide range of LCD and TV formats (both NTSC and PAL) with text insertion features
- Includes an embedded JPEG encoder/decoder unit
- Includes a MIPS PR3001 CPU, running at a frequency in a range from 12 to 28 MHz
- PRISC compatible PI-bus architecture, interrupt, power management, clock and reset architectures
- Includes a dedicated video bus supporting SDRAM memory for picture storage

- Interface to ROM, DRAM, SRAM, flash and PC Card [Compact Flash and SSFDC (SmartMedia)]
- Integrated general purpose peripheral units like a UART, timers, an I^2C-bus transceiver, ADC converters, RTC and I/O ports
- Includes USB and RS-232C communication interfaces.

2.2 External interfaces

- Two UART (RS-232) data ports with DMA capabilities (≤187.5 kbit/s) including hardware flow control RxD, TxD, RTS, CTS for modem support
- 32 general purpose, bidirectional I/O interface pins, the first 8 bits may also be used as interrupt inputs
- Two PWM outputs (8-bit resolution).

2.3 CPU related features

- 32-bit PR3001 core
- 1-kbyte data cache and 4-kbyte instruction cache
- Programmable low-power mode, including wake-up on interrupt
- Memory management unit [Translation Lookaside Buffer (TLB)]
- Two built in 24-bit general purpose timers and one 24-bit watchdog timer
- Real-time clock unit (active in sleep mode)
- On-chip 8-kbyte SRAM for storing code which needs fast execution
- Platform software based on real-time pSOS (plug-in Silicon Operating System).

2.4 DSP features

- Advanced colour reconstruction
- Programmable digital filters for noise reduction and contour enhancement
- 16 programmable measurement windows allowing to perform the measurements necessary for exposure, white balance and focus adjustment in a DSC system; available measurement outputs for exposure, white balance and focus control.

2.5 Pulse pattern generator features

- Programmable through dedicated PC-software, allowing to drive all CCDs currently present in the market, as well as CDS/AGC/ADC chips: up to 8×8 kpixels.

2.6 JPEG

- Fully ISO10918 compliant
- Supports Tiff, Exif 2.1, DCF & DPOF
- Quick compression (4 images/s for a 1.3 Mpixels resolution).

2.7 USB interface

- Fully compatible with USB.

2.8 Card interfaces

- Compatible with all SSFDC/CF cards on the market.

2.9 Bus

- Bus structure allows for parallel processing depending on software implementation, allowing easy system optimization.

2.10 SDRAM interface features

- Supports up to 128 Mbyte of SDRAM and 16-bit wide addressses
- Bus speed: 1 or 2 times CCD pixel clock
- 32-bit bus width.

3. Quick reference data

Table 1: Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDD}	digital supply voltage		[1]	3	3.3	3.6	V
V_{DDA}	analog supply current		[2]	3	3.3	3.6	V
I_P	total supply current	f_{clk} = 25 MHz		–	360	560	mA
V_I	input voltage						
	general			0	–	V_{DDD}	V
	5 V tolerant cells only		[3]	0	–	5.5	V
V_O	output voltage	output active		0	–	V_{DDD}	V
T_{amb}	ambient temperature			0	25	70	°C
f_{clk}	clock frequency			–	25	27	MHz

[1] The supplies considered as digital supply (V_{DDD}) are: V_{DDD}, $V_{DDD(RTC)}$.

[2] The supplies considered as analog supply (V_{DDA}) are: $V_{DDA(SPLL)}$, $V_{DDA(PLL)}$, $V_{DDA(BG)}$, $V_{DDA(PPG1)}$, $V_{DDA(ADC)}$, $V_{DDA(OUTPUT1)}$, $V_{DDA(OUTPUT2)}$, $V_{DDA(LCDR)}$, $V_{DDA(LCDG)}$, $V_{DDA(LCDB)}$, $V_{DDA(DLL)}$.

[3] Including voltage on outputs in 3-state mode; only valid when supply voltage is present.

4. Ordering information

Table 2: Ordering information

Type number	Package		
	Name	Description	Version
SAA8122AEL	LFBGA324	plastic low profile fine-pitch ball grid array package; 324 balls; body 16 × 16 × 1.2 mm	SOT571-1

5. Block diagram

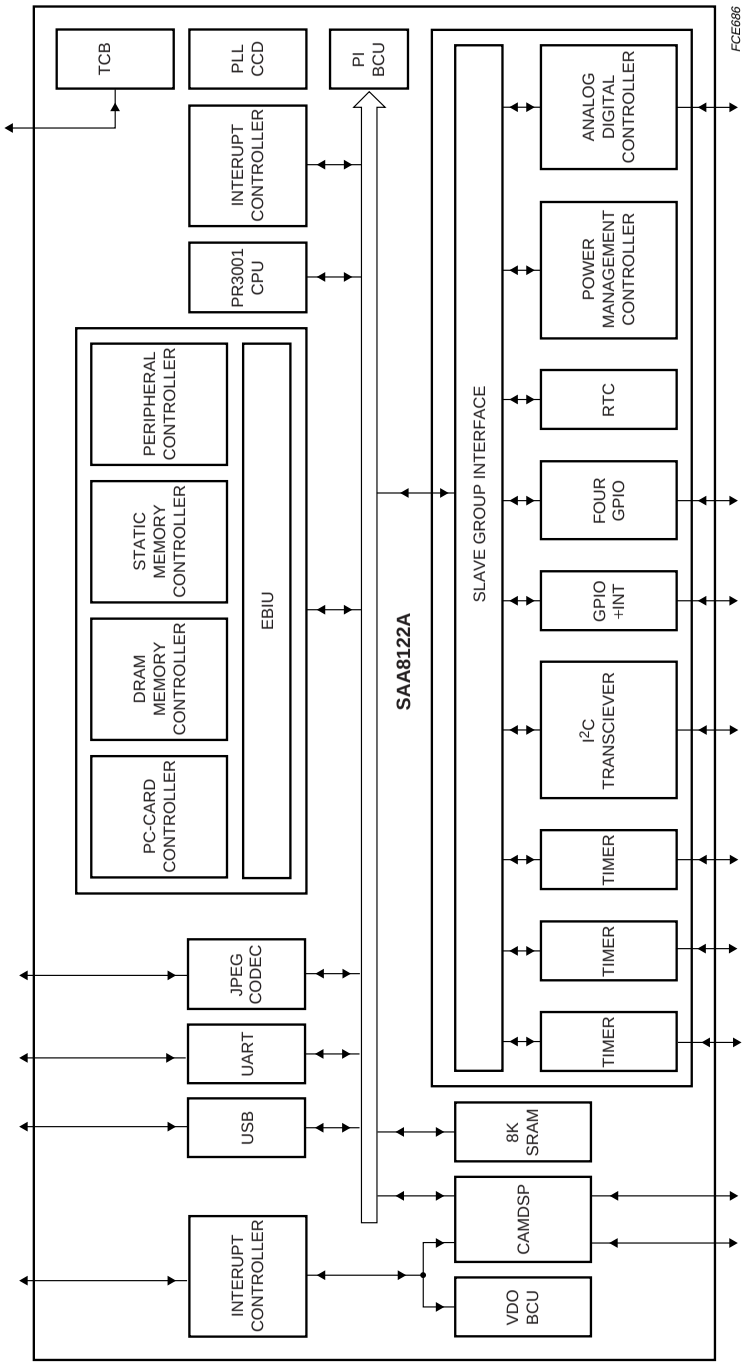


Fig 1. Block diagram.

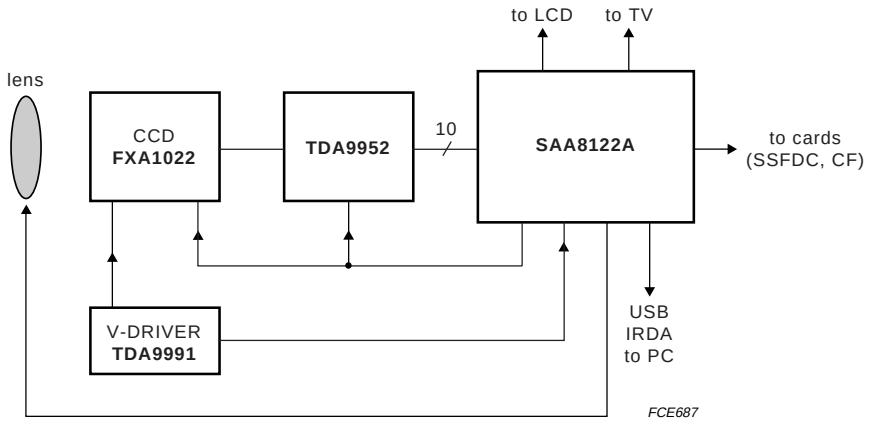


Fig 2. System block diagram.

6. Pinning information

6.1 Pinning

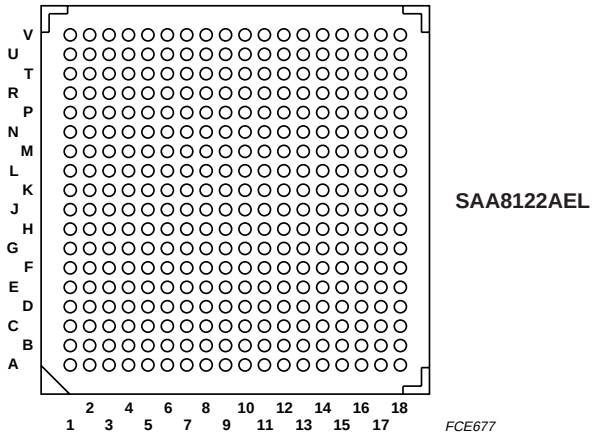


Fig 3. Pin configuration (bottom view).

6.2 Pin description

Table 3: Pin description

Symbol	Pin	Type	Description
V_{DDD}	A1	-	digital supply voltage
$V_{SSA(DLL)}$	A2	-	analog ground for DLL of PPG
$V_{DDA(DLL)}$	A3	-	analog supply voltage for DLL of PPG
DISP_VSYNC	A4	O	digital vertical synchronization signal
IO1/IRQ17	A5	I/O	I/O port 0 bit 1 or interrupt request 17
$V_{DDA(LCDG)}$	A6	P	analog supply voltage for DAC component G
$V_{DDA(OUTPUT2)}$	A7	P	analog supply voltage for DAC video output 2

Table 3: Pin description *...continued*

Symbol	Pin	Type	Description
CREF_BG1	A8	-	band-gap 1
$V_{SS(BG)}$	A9	P	ground for BG of video DAC
$\overline{SYSRSTIN}$	A10	I	system reset input/output; active LOW
$V_{SS(RTC)}$	A11	P	ground for RTC
T0_CAP0	A12	I	timer 0 capture input 0
CNT2	A13	I	timer 2 count pulse input
CNT1	A14	I	timer 1 count pulse input
PWM0	A15	O	timer 0 PWM output
ADC0	A16	I	analog input signal 0 for level measurement
ADC3	A17	I	analog input signal 3 for level measurement
$V_{SS(ADC)}$	A18	P	ground for ADC
ANPPG1	B1	O	PPG analog signal 1
IO6/IRQ22	B4	I/O	I/O port 0 bit 6 or interrupt request 22
IO3/IRQ19	B5	I/O	I/O port 0 bit 3 or interrupt request 19
LCD_G	B6	O	analog green signal
VIDEO_OUT2	B7	O	video output signal 2
$V_{SSA(ref)}$	B8	O	analog reference ground
SC_TCK	B9	I	test clock input for surround scan chains
TCK	B10	I	test clock input
XTALCCDIN	B11	-	oscillator input from a specific CCD crystal
$V_{DDA(SPLL)}$	B12	P	analog supply voltage for SPLL
$V_{SS(PLL)}$	B13	P	ground for PLL
CNT0	B14	I	timer 0 count pulse input
$V_{SSA(ref)(ADC)}$	B15	O	analog reference ground for ADC
ADC2	B16	I	analog input signal 2 for level measurement
$V_{DDA(ADC)}$	B17	P	analog supply voltage for ADC
IO23	B18	I/O	I/O port 2 bit 7
$V_{DDA(PPG1)}$	C1	P	analog supply voltage for PPG
$V_{DDA(PPG0)}$	C2	P	analog supply voltage for PPG
$V_{DDA(DLL)}$	C3	P	analog supply voltage for DLL of PPG
IO7/IRQ23	C4	I/O	I/O port 0 bit 7 or interrupt request 23
IO4/IRQ20	C5	I/O	I/O port 0 bit 4 or interrupt request 20
LCD_R	C6	O	analog red signal
LCD_B	C7	O	analog blue signal
$V_{DDA(OUTPUT1)}$	C8	P	analog supply voltage for DAC video output 1
$V_{DDA(BG)}$	C9	P	analog supply voltage for BG of video DAC
TMS	C10	I	test mode select input
XTAL32KIN	C11	-	oscillator input from a 32 kHz crystal
XTAL10IN	C12	-	oscillator input from a 10 MHz crystal
GATE2	C13	I	timer 2 gate input
$V_{DDA(PLL)}$	C14	P	analog supply voltage for PLL

Table 3: Pin description *...continued*

Symbol	Pin	Type	Description
PWM1	C15	O	timer 1 PWM output
ADC1	C16	I	analog input signal 1 for level measurement
IO22	C17	I/O	I/O port 2 bit 6
IO16	C18	I/O	I/O port 2 bit 0
ANPPG7	D1	O	PPG analog signal 7
$V_{SSA(PPG1)}$	D2	P	analog ground for PPG
DISP_HSYNC	D3	O	digital horizontal synchronization signal
IO5/IRQ21	D4	I/O	I/O port 0 bit 5 or interrupt request 21
IO0/IRQ16	D5	I/O	I/O port 0 bit 0 or interrupt request 16
$V_{SSA(LCD)}$	D6	P	analog ground for display RGB
$V_{SS(OUTPUT)}$	D7	P	ground for DAC video output
CREF_BG2	D8	-	band-gap 2
TDO	D9	O	test data output
TDI	D10	I	test data input
XTAL32KOUT	D11	-	oscillator output from a 32 kHz crystal
XTAL10OUT	D12	-	oscillator output from a 10 MHz crystal
T0_CAP1	D13	I	timer 0 capture input 1
GATE0	D14	I	timer 0 gate input
PWM2	D15	O	timer 2 PWM output
IO17	D16	I/O	I/O port 2 bit 1
IO15	D17	I/O	I/O port 1 bit 7
IO11	D18	I/O	I/O port 1 bit 3
PPG1	E1	O	PPG digital signal 0
PPG2	E2	O	PPG digital signal 1
ANPPG8	E3	O	PPG analog signal 8
$V_{DDA(PPG0)}$	E4	P	analog supply voltage for PPG
IO2/IRQ18	E5	I/O	I/O port 0 bit 2 or interrupt request 18
$V_{DDA(LCDR)}$	E6	P	analog supply voltage for DAC component R
$V_{DDA(LCDB)}$	E7	P	analog supply voltage for DAC component B
VIDEO_OUT1	E8	O	video output signal 1
$\overline{SYSRST}$	E9	O	system reset output; active LOW
TRST	E10	I	test reset input
$V_{DDD(RTC)}$	E11	P	digital supply voltage for RTC
XTALCCDOUT	E12	-	oscillator output from a specific CCD crystal
GATE1	E14	I	timer 1 gate input
IO18	E15	I/O	I/O port 2 bit 2
IO10	E16	I/O	I/O port 1 bit 2
IO9	E17	I/O	I/O port 1 bit 1
UA_CLK	E18	I	UART external clock
PPG5	F1	O	PPG digital signal 4
PPG6	F2	O	PPG digital signal 5

Table 3: Pin description *...continued*

Symbol	Pin	Type	Description
PPG3	F3	O	PPG digital signal 2
ANPPG5	F4	O	PPG analog signal 5
ANPPG3	F5	O	PPG analog signal 3
V_{SS}	F6	-	ground
V_{SS}	F7	-	ground
V_{DD}	F8	-	supply voltage
V_{DD}	F9	-	supply voltage
V_{DD}	F10	-	supply voltage
V_{DD}	F11	-	supply voltage
V_{DD}	F12	-	supply voltage
IO20	F13	I/O	I/O port 2 bit 4
IO19	F14	I/O	I/O port 2 bit 3
IO12	F15	I/O	I/O port 1 bit 4
CTS	F16	I	UART clear to send
RXD	F17	I	UART receive input
TXD	F18	O	UART transmit output
PPG10	G1	O	PPG digital signal 17
PPG12	G2	O	PPG digital control signal 1
PPG8	G3	O	PPG digital signal 8
PPG4	G4	O	PPG digital signal 3
ANPPG6	G5	O	PPG analog signal 6
ANPPG2	G6	O	PPG analog signal 2
V_{DD}	G7	-	supply voltage
V_{SS}	G8	-	ground
V_{SS}	G9	-	ground
V_{SS}	G10	-	ground
V_{SS}	G11	-	ground
V_{DD}	G12	-	supply voltage
IO21	G13	I/O	I/O port 2 bit 5
IO13	G14	I/O	I/O port 1 bit 5
RTS	G15	O	UART request to send
SDA	G16	I/O	I^2C-bus data
SCL	G17	I/O	I^2C-bus clock
n.c.	G18	-	not connected
HDHREF	H1	I/O	PPG horizontal synchronization signal
VDVS	H2	I/O	PPG vertical synchronization signal
PPG13	H3	O	PPG digital control signal 2
PPG7	H4	O	PPG digital control signal 6
PPG14	H5	O	PPG digital control signal 3
ANPPG4	H6	O	PPG analog signal 4
V_{DD}	H7	-	supply voltage

Table 3: Pin description *...continued*

Symbol	Pin	Type	Description
V_{SS}	H8	-	ground
V_{SS}	H9	-	ground
V_{SS}	H10	-	ground
V_{SS}	H11	-	ground
V_{DD}	H12	-	supply voltage
IO14	H13	I/O	I/O port 1 bit 6
RXVPI	H14	I	USB
n.c.	H15	-	not connected
RXVMI	H16	I/O	USB
TXVPO	H17	O	USB
RXDATA	H18	I	USB
CCD_IM2	J1	I	digital image signal 2
CCD_IM3	J2	I	digital image signal 3
CCD_IM4	J3	I	digital image signal 4
PPG11	J4	O	PPG digital signal 18
PPG9	J5	O	PPG digital signal 8
V_{DD}	J6	-	supply voltage
V_{DD}	J7	-	supply voltage
V_{SS}	J8	-	ground
V_{SS}	J9	-	ground
V_{SS}	J10	-	ground
V_{SS}	J11	-	ground
V_{DD}	J12	-	supply voltage
IO8	J13	I/O	I/O port 1 bit 0
SUSPEND	J14	O	USB
TXOE	J15	O	USB
D2	J16	I/O	EBIU D2
D3	J17	I/O	EBIU D3
D0	J18	I/O	EBIU D0
CCD_IM10	K1	I	digital image signal 10
CCD_IM9	K2	I	digital image signal 9
CCD_IM8	K3	I	digital image signal 8
CCD_IM1	K4	I	digital image signal 1
CCD_IM0	K5	I	digital image signal 0
V_{DD}	K6	-	supply voltage
V_{DD}	K7	-	supply voltage
V_{SS}	K8	-	ground
V_{SS}	K9	-	ground
V_{SS}	K10	-	ground
V_{SS}	K11	-	ground
V_{DD}	K12	-	supply voltage

Table 3: Pin description *...continued*

Symbol	Pin	Type	Description
TXVMO	K13	O	USB
D1	K14	I/O	EBIU D1
D4	K15	I/O	EBIU D4
D6	K16	I/O	EBIU D6
D7	K17	I/O	EBIU D7
D8	K18	I/O	EBIU D8
SD_A[0]	L1	O	SDRAM controller address bus bit 0
SD_A[3]	L2	O	SDRAM controller address bus bit 3
SD_A[2]	L3	O	SDRAM controller address bus bit 2
CCD_IM6	L4	I	digital image signal 6
CCD_IM7	L5	I	digital image signal 7
CCD_IM5	L6	I	digital image signal 5
V_{DD}	L7	-	supply voltage
V_{SS}	L8	-	ground
V_{SS}	L9	-	ground
V_{SS}	L10	-	ground
V_{SS}	L11	-	ground
V_{DD}	L12	-	supply voltage
D5	L13	I/O	EBIU D5
D9	L14	I/O	EBIU D9
D11	L15	I/O	EBIU D11
D14	L16	I/O	EBIU D14
D13	L17	I/O	EBIU D13
D12	L18	I/O	EBIU D12
SD_A[7]	M1	O	SDRAM controller address bus bit 7
SD_A[8]	M2	O	SDRAM controller address bus bit 8
SD_A[9]	M3	O	SDRAM controller address bus bit 9
SD_A[4]	M4	O	SDRAM controller address bus bit 4
SD_A[1]	M5	O	SDRAM controller address bus bit 1
CCD_IM11	M6	I	digital image signal 11
V_{DD}	M7	-	supply voltage
V_{SS}	M8	-	ground
V_{SS}	M9	-	ground
V_{SS}	M10	-	ground
V_{SS}	M11	-	ground
V_{DD}	M12	-	supply voltage
D10	M13	I/O	EBIU D10
$\overline{SC\_SE}$	M14	O	EBIU controller $\overline{SE}$ signal for SSFDC card; active LOW
D15	M15	I/O	EBIU D15
$\overline{PC\_WAIT2}$	M16	I	EBIU controller WAIT signal for PC card 2; active LOW
$\overline{SC\_CE}$	M17	O	EBIU controller $\overline{CE}$ signal for SSFDC card; active LOW

Table 3: Pin description *...continued*

Symbol	Pin	Type	Description
SC_CLE	M18	O	EBIU controller CLE signal for SSFDC card
SD_A[12]	N1	O	SDRAM controller address bus bit 12
SD_A[13]	N2	O	SDRAM controller address bus bit 13
SD_A[14]	N3	O	SDRAM controller address bus bit 14
SD_A[10]	N4	O	SDRAM controller address bus bit 10
SD_A[6]	N5	O	SDRAM controller address bus bit 6
SD_A[5]	N6	O	SDRAM controller address bus bit 5
V_{DD}	N7	-	supply voltage
V_{DD}	N8	-	supply voltage
V_{DD}	N9	-	supply voltage
V_{DD}	N10	-	supply voltage
V_{DD}	N11	-	supply voltage
SC_ALE	N12	O	EBIU controller ALE signal for SSFDC card
$\overline{\text{PC2\_CE1}}$	N13	O	EBIU controller CE1 signal for PC card 2; active LOW
$\overline{\text{PC2\_CE2}}$	N14	O	EBIU controller CE2 signal for PC card 2; active LOW
$\overline{\text{PC\_REG}}$	N15	O	EBIU controller REG signal for PC cards; active LOW
$\overline{\text{PC\_WAIT1}}$	N16	O	EBIU controller WAIT signal for PC card 1; active LOW
$\overline{\text{IOWR\_WE}}$	N17	O	EBIU controller IORD signal for PC cards; active LOW
$\overline{\text{IORD\_RE}}$	N18	O	EBIU controller IORD signal for PC cards; active LOW
SD_CLKOUT	P1	O	SDRAM controller clock output
SD_CLKIN	P2	I	SDRAM controller clock input
$\overline{\text{SD\_CS2}}$	P3	O	SDRAM controller chip select for memory 2; active LOW
SD_CLKEN	P4	O	SDRAM controller clock enable
SD_A[11]	P5	O	SDRAM controller address bus bit 11
V_{DD}	P6	-	supply voltage
SD_D[7]	P7	I/O	SDRAM controller data bus bit 7
IO25	P8	I/O	I/O port 3 bit 1
IO38	P9	I/O	I/O port 4 bit 6
A25	P10	I/O	EBIU A25 (Strapin[0] during boot sequence)
A21	P11	I/O	EBIU A21 (Strapin[4] during boot sequence)
V_{DD}	P12	-	supply voltage
A14	P13	I/O	EBIU A14
SCLK	P14	O	EBIU controller clock signal for external peripherals
A9	P15	I/O	EBIU A9
$\overline{\text{CAS0}}$	P16	O	EBIU controller CAS signal for DRAM memory for lower byte; used as data strobe signal for lower byte for general chip select; active LOW
$\overline{\text{PC1\_CE1}}$	P17	O	EBIU controller CE1 signal for PC card 1; active LOW
$\overline{\text{PC1\_CE2}}$	P18	O	EBIU controller CE2 signal for PC card 1; active LOW
$\overline{\text{SD\_CS0}}$	R1	O	SDRAM controller chip select for memory 0; active LOW
$\overline{\text{SD\_CS1}}$	R2	O	SDRAM controller chip select for memory 1; active LOW
$\overline{\text{SD\_CS3}}$	R3	O	SDRAM controller chip select for memory 3; active LOW

Table 3: Pin description *...continued*

Symbol	Pin	Type	Description
SD_D[4]	R4	I/O	SDRAM controller data bus bit 4
$\overline{\text{SD\_RAS}}$	R5	O	SDRAM controller row address strobe; active LOW
SD_D[6]	R6	I/O	SDRAM controller data bus bit 6
SD_D[13]	R7	I/O	SDRAM controller data bus bit 13
IO30	R8	I/O	I/O port 3 bit 6
IO37	R9	I/O	I/O port 4 bit 5
A24	R10	I/O	EBIU A24 (Strapin[1] during boot sequence)
A19	R11	I/O	EBIU A19 (Strapin[6] and Strapin[9] during boot sequence)
A18	R12	I/O	EBIU A18 (Strapin[10] during boot sequence)
A13	R13	I/O	EBIU A13
A5	R14	O	EBIU A5
$\overline{\text{CS6}}$	R15	O	EBIU controller chip select 6; active LOW
$\overline{\text{CAS1}}$	R16	O	EBIU controller CAS signal for DRAM memory for upper byte; used as data strobe signal for upper byte for general chip select; active LOW
$\overline{\text{OE}}$	R17	O	EBIU controller output enable signal; active LOW
$\overline{\text{RAS}}$	R18	O	EBIU controller RAS signal for DRAM memory; active LOW
$\overline{\text{SD\_CAS}}$	T1	O	SDRAM controller column address strobe; active LOW
$\overline{\text{SD\_WE}}$	T2	O	SDRAM controller write enable; active LOW
SD_D[3]	T3	I/O	SDRAM controller data bus bit 3
SD_D[8]	T4	I/O	SDRAM controller data bus bit 8
SD_D[10]	T5	I/O	SDRAM controller data bus bit 10
SD_D[14]	T6	I/O	SDRAM controller data bus bit 14
IO26	T7	I/O	I/O port 3 bit 2
IO29	T8	I/O	I/O port 3 bit 5
IO33	T9	I/O	I/O port 4 bit 1
IO36	T10	I/O	I/O port 4 bit 4
A23	T11	I/O	EBIU A23 (Strapin[2] during boot sequence)
A16	T12	I/O	EBIU A16
A12	T13	I/O	EBIU A12
A3	T14	O	EBIU A3
$\overline{\text{CS7}}$	T15	O	EBIU controller chip select 7; active LOW
$\overline{\text{CS4}}$	T16	O	EBIU controller chip select 4; active LOW
$\overline{\text{WE}}$	T17	O	EBIU controller write enable signal; active LOW
$\overline{\text{CS\_WAIT}}$	T18	O	EBIU controller wait signal for chip selects; active LOW
$\overline{\text{SD\_DQM0}}$	U1	O	SDRAM controller DQ mask enable for byte 0; active LOW
$\overline{\text{SD\_DQM1}}$	U2	O	SDRAM controller DQ mask enable for byte 1; active LOW
SD_D[2]	U3	I/O	SDRAM controller data bus bit 2
SD_D[9]	U4	I/O	SDRAM controller data bus bit 9
SD_D[11]	U5	I/O	SDRAM controller data bus bit 11
SD_D[15]	U6	I/O	SDRAM controller data bus bit 15
IO27	U7	I/O	I/O port 3 bit 3

Table 3: Pin description *…continued*

Symbol	Pin	Type	Description
IO32	U8	I/O	I/O port 4 bit 0
IO34	U9	I/O	I/O port 4 bit 2
A22	U10	I/O	EBIU A22 (Strapin[3] during boot sequence)
A17	U11	I/O	EBIU A17 (Strapin[11] during boot sequence)
A11	U12	I/O	EBIU A11
A8	U13	I/O	EBIU A8
A4	U14	O	EBIU A4
A2	U15	O	EBIU A2
$\overline{CS5}$	U16	O	EBIU controller chip select 5; active LOW
$\overline{CS3}$	U17	O	EBIU controller chip select 3; active LOW
$\overline{CS0}$	U18	O	EBIU controller chip select 0; active LOW
SD_D[0]	V1	I/O	SDRAM controller data bus bit 0
SD_D[1]	V2	I/O	SDRAM controller data bus bit 1
SD_D[5]	V3	I/O	SDRAM controller data bus bit 5
SD_D[12]	V4	I/O	SDRAM controller data bus bit 12
IO24	V5	I/O	I/O port 3 bit 0
IO28	V6	I/O	I/O port 3 bit 4
IO31	V7	I/O	I/O port 3 bit 7
IO35	V8	I/O	I/O port 4 bit 3
IO39	V9	I/O	I/O port 4 bit 7
A20	V10	I/O	EBIU A20 (Strapin[5] and Strapin[8] during boot sequence)
A15	V11	I/O	EBIU A15
A10	V12	I/O	EBIU A10
A7	V13	I/O	EBIU A7
A6	V14	I/O	EBIU A6
A1	V15	O	EBIU A1
A0	V16	O	EBIU A0
$\overline{CS2}$	V17	O	EBIU controller chip select 2; active LOW
$\overline{CS1}$	V18	O	EBIU controller chip select 1; active LOW

7. Limiting values

Table 4: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DDD}	digital supply voltage			–0.5	4	V
V_{DDA}	analog supply voltage			–0.5	4	V
V_I	DC input voltage	general	[1] [2]	–0.5	V_{DD} + 0.5	V
		5 V tolerant cells only	[2] [3]	–0.5	–0.5	V
I_{DD}	DC supply current per supply pin		[4]	–	60	mA
I_{SS}	DC ground current per ground pin		[4]	–	60	mA
T_{stg}	storage temperature		[5]	0	125	°C

[1] Value may not exceed 4 V.

[2] Including voltage on outputs in 3-state mode.

[3] Only valid when supply voltage is present.

[4] The peak current is limited to 10 times the corresponding maximum current.

[5] Dependent of package and not yet determined.

8. Characteristics

Table 5: General supply characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDD}	digital supply voltage		3.0	3.3	3.6	V
$V_{DDA(DLL)}$	analog supply voltage for DLL		3.0	3.3	3.6	V
$V_{DDA(LCDR)}$	analog supply voltage for LCDR output of DAC		3.0	3.3	3.6	V
$V_{DDA(LCDG)}$	analog supply voltage for LCDG output of DAC		3.0	3.3	3.6	V
$V_{DDA(LCDB)}$	analog supply voltage for LCDB		3.0	3.3	3.6	V
$V_{DDA(OUTPUT1)}$	analog supply voltage for video output 1 of DAC		3.0	3.3	3.6	V
$V_{DDA(OUTPUT2)}$	analog supply voltage for video output 2 of DAC		3.0	3.3	3.6	V
$V_{DDA(ADC)}$	analog supply voltage for ADC		3.0	3.3	3.6	V
$V_{DDA(PPG1)}$	analog supply voltage for PPG		3.0	3.3	3.6	V
$V_{DDA(PPG0)}$	analog supply voltage for PPG		3.0	3.3	3.6	V
$V_{DDA(BG)}$	analog supply voltage for bandgap		3.0	3.3	3.6	V
$V_{DDA(PLL)}$	analog supply voltage for PLL		3.0	3.3	3.6	V
$V_{DDA(SPLL)}$	analog supply voltage for SPLL		3.0	3.3	3.6	V
$V_{DDD(RTC)}$	digital supply voltage for RTC	[1]	3.0	3.3	3.6	V

[1] $V_{DDD(RTC)}$ is the single supply which may be on when the others are off. In this case the I/Os of the SAA8122A have to be at 0 V.

Table 6: Operating characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DDA(LCDR)}$	analog supply voltage for LCDR output of DAC		3.0	3.3	3.6	V
$V_{DDA(LCDG)}$	analog supply voltage for LCDG output of DAC		3.0	3.3	3.6	V
$V_{DDA(LCDB)}$	analog supply voltage for LCDB output of DAC		3.0	3.3	3.6	V
$V_{DDA(OUTPUT1)}$	analog supply voltage for video output 1 of DAC		3.0	3.3	3.6	V
$V_{DDA(OUTPUT2)}$	analog supply voltage for video output 2 of DAC		3.0	3.3	3.6	V
$V_{DDA(BG)}$	analog supply voltage for bandgap		3.0	3.3	3.6	V
V_{BG}	bandgap reference voltage	(4σ)	1.18	1.22	1.26	V
V_{OL}	LOW-level output voltage	code 0	-	0.225	-	V
V_{OH}	HIGH-level output voltage	code 511	-	1.625	-	V
LCD channels (1 kΩ buffer)						
R_L	load resistance		-	1	-	kΩ
C_L	load capacitance		-	-	5	pF
RES	resolution		-	8	-	bit
LCD channels (75 Ω mode)						
R_L	load resistance		-	75	-	Ω
C_L	load capacitance		-	5	100	pF
RES	resolution		-	9	-	bit
VIDEO_OUT channels (1 kΩ buffer)						
R_L	load resistance		-	1	-	kΩ
C_L	load capacitance		-	-	5	pF
RES	resolution		-	8	-	bit
VIDEO_OUT channels (1 kΩ mode)						
R_L	load resistance		-	1	-	kΩ
C_L	load capacitance		-	-	5	pF
RES	resolution		-	9	-	bit
ADC						
$V_{DDA(ADC)}$	analog supply voltage for analog ADC		3.0	3.3	3.6	V
ΔV_{DD}	supply voltage difference between V_{DDA} and $V_{DDA(ADC)}$		-	-	0.2	V
RES	resolution		8	-	10	bit
C_i	input capacitance		-	2	-	pF
V_i	input voltage		0	-	3.3	V
f_{sample}	sample frequency	8-bit	0	-	100	kHz
PLL						
$V_{DDA(PLL)}$	analog supply voltage for analog PLL		3.0	3.3	3.6	V

Table 6: Operating characteristics…*continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ΔV_{DD}	supply voltage difference between V_{DDA} and $V_{DDA(PLL)}$		-	-	0.2	V
f_{clk}	clock frequency		-	96	-	MHz
SPLL						
$V_{DDA(SPLL)}$	analog supply voltage for analog SPLL		3.0	3.3	3.6	V
ΔV_{DD}	supply voltage difference between V_{DDA} and $V_{DDA(SPLL)}$		-	-	0.2	V
Power-on reset						
V_{trip}	trip level of power-on reset		1.5	2.07	2.65	V
t_{HIGH}	time that V_{DDA} has to be above 2.65 V before internal reset signal is asserted		-	-	2	µs
t_{LOW}	time that V_{DDA} has to be above 2.65 V before internal reset signal is de-asserted		-	-	8	µs
Analog PPG						
$V_{DDA(DLL)}$	analog supply voltage for analog DLL		3.0	3.3	3.6	V
$\Delta V_{DD-DDA(DLL)}$	supply voltage difference between V_{DDA} and $V_{DDA(DLL)}$		-	-	0.2	V
$V_{DDA(PPG1)}$; $V_{DDA(PPG0)}$	analog supply voltage for analog PPG		3.0	3.3	3.6	V
$\Delta V_{DD-DDA(PPG)}$	supply voltage difference between V_{DDA} and $V_{DDA(PPG1)}$ or $V_{DDA(PPG0)}$		-	-	0.2	V
I/Os (V_{DDD} = V_{DDA}, T_{amb} = 0 to 60 °C)						
Data and control inputs						
SD_CLKIN						
V_{IL}	LOW-level digital input voltage		0	-	$0.3V_{DDD}$	V
V_{IH}	HIGH-level digital input voltage		$0.7V_{DDD}$	-	V_{DDD}	V
C_i	input capacitance		-	1.14	-	pF
I_{IL}	LOW-level input current	V_I = 0 V	-	-	1	µA
I_{IH}	HIGH-level input current	$V_I = V_{DDD}$	-	-	1	µA
$I_{lu(I/O)}$	I/O latch-up current	$-0.5 < V_{DDD} + 0.5$	100	-	-	mA
$\overline{CS\_WAIT}$, $\overline{PC\_WAIT1}$, $\overline{PC\_WAIT2}$, SC_TCK, TCK, TDI, TMS, $\overline{TRST}$, CCD_IM0 to CCD_IM11, CNT0 to CNT2, $\overline{GATE0}$ to $\overline{GATE2}$, T0_CAP0, T0_CAP1, $\overline{CTS}$, RXD, UA_CLK, RXDATA, $\overline{RXVMI}$, $\overline{RXVPI}$						
V_{IL}	LOW-level digital input voltage		0	-	0.8	V
V_{IH}	HIGH-level digital input voltage		2.0	-	5.5	V
C_i	input capacitance		-	1.2	-	pF
I_{IL}	LOW-level input current	V_I = 0 V	-	-	1	µA
I_{IH}	HIGH-level input current	$V_I = V_{DDD}$	-	-	1	µA
$I_{lu(I/O)}$	I/O latch-up current	$-0.5 < V_{DDD} < 5.5$	100	-	-	mA
$\overline{SYSRSTIN}$						
V_{IL}	LOW-level digital input voltage		0	-	0.8	V

Table 6: Operating characteristics…*continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH-level digital input voltage		2.0	-	5.5	V
V_{hys}	hysteresis voltage		0.4	-	-	V
C_i	input capacitance		-	1.2	-	pF
I_{IL}	LOW-level input current	V_I = 0 V	-	-	1	µA
I_{IH}	HIGH-level input current	$V_I = V_{DDD}$	-	-	1	µA
$I_{lu(I/O)}$	I/O latch-up current	$-0.5 < V_{DDD} < 5.5$	100	-	-	mA
Data and control outputs						
ANPPG1 to ANPPG8						
V_{OL}	LOW-level digital output voltage	I_{OL} = 4 mA	0	-	0.4	V
V_{OH}	HIGH-level digital output voltage	I_{OH} = 4 mA	$V_{DDA} - 0.4$	-	V_{DDA}	V
$C_{o(L)(max)}$	maximum output load capacitance	[1]	-	-	100	pF
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; $V_{OH} = V_{DDA} - 0.4$	4	-	-	mA
I_{OH}	HIGH-level output current	$V_{OH} = V_{DDA} - 0.4$	–4	-	-	mA
SCLK, SD_A[0] to SD_A[14], $\overline{SD\_CAS}$, SD_CLKEN, SD_CLKOUT, $\overline{SD\_CS0}$ to $\overline{SD\_CS3}$, $\overline{SD\_DQM0}$ to $\overline{SD\_DQM1}$, SD_RAS, $\overline{SD\_WE}$						
V_{OL}	LOW-level digital output voltage	I_{OL} = 4 mA	0	-	0.4	V
V_{OH}	HIGH-level digital output voltage	I_{OH} = –4 mA	$V_{DDD} - 0.4$		V_{DDD}	V
C_i	input capacitance	-	-	1	-	pF
$C_{o(L)(max)}$	maximum output load capacitance	- [1]	-	-	100	pF
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	-	-	-	µA
I_{OH}	HIGH-level output current	$V_{OH} = V_{DDD} - 0.4$	–4	-	-	mA
I_{OZ}	3-state output leakage current	V_O = 0; $V_O = V_{DDD}$	-	-	1	µA
TDO, $\overline{SYSRST}$, PWM0 to PWM2, RTS, TXD, SUSPEND, TXOE, TXVMO, TXVPO, DISP_HSYNC, DISP_VSYNC						
V_{OL}	LOW-level digital output voltage	I_{OL} = 2 mA	0	-	0.4	V
V_{OH}	HIGH-level digital output voltage	I_{OH} = –2 mA	$V_{DDD} - 0.4$	-	V_{DDD}	V
C_i	input capacitance	-	-	2.2	-	pF
$C_{o(L)(max)}$	maximum output load capacitance	- [1]	-	-	30	pF
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; $V_{OH} = V_{DDD} - 0.4$	2	-	-	mA
I_{OH}	HIGH-level output current	$V_{OH} = V_{DDD} - 0.4$	–2	-	-	mA
I_{OZ}	3-state output leakage current	V_O = 0; $V_O = V_{DD}$	-	-	1	µA
$\overline{CAS0}$, $\overline{CAS1}$, $\overline{CS0}$ to $\overline{CS7}$, $\overline{IORD\_RE}$, $\overline{IOWR\_WE}$, $\overline{OE}$, $\overline{PC\_REG}$, $\overline{PC1\_CE1}$, $\overline{PC1\_CE2}$, $\overline{RAS}$, SC_ALE, $\overline{SC\_SE}$, $\overline{WE}$, PPG1 to PPG14						
V_{OL}	LOW-level digital output voltage	I_{OL} = 4 mA	0	-	0.4	V
V_{OH}	HIGH-level digital output voltage	I_{OH} = –4 mA	$V_{DDD} - 0.4$	-	V_{DDD}	V
C_i	input capacitance	-	-	2.4	-	pF
$C_{o(L)(max)}$	maximum output load capacitance	- [1]	-	-	30	pF
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; $V_{OH} = V_{DDD} - 0.4$	4	-	-	mA
I_{OH}	HIGH-level output current	$V_{OH} = V_{DDD} - 0.4$	–4	-	-	mA

Table 6: Operating characteristics…*continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{OZ}	3-state output leakage current	V_O = 0; $V_O = V_{DDD}$	-	-	1	µA
Data and control I/Os						
SD_D[0] to SD_D[15]						
V_{IL}	LOW-level digital input voltage	-	0	-	$0.3V_{DDD}$	V
V_{IH}	HIGH-level digital input voltage	-	$0.7V_{DDD}$	-	V_{DDD}	V
V_{OL}	LOW-level digital output voltage	I_{OL} = 4 mA	0	-	0.4	V
V_{OH}	HIGH-level digital output voltage	I_{OH} = –4 mA	V_{DDD} – 0.4	-	V_{DDD}	V
C_i	input capacitance	-	-	1.2	-	pF
$C_{o(L)(max)}$	maximum output load capacitance	- [1]	-	-	100	pF
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; $V_{OH} = V_{DDD}$ – 0.4	4	-	-	mA
I_{OH}	HIGH-level output current	$V_{OH} = V_{DDD}$ – 0.4	–4	-	-	mA
I_{OZ}	3-state output leakage current	V_O = 0; $V_O = V_{DDD}$	-	-	1	µA
I_{IL}	LOW-level input current	V_I = 0	-	-	1	µA
I_{IH}	HIGH-level input current	$V_I = V_{DDD}$	-	-	1	µA
A0 to A15, IO8 to IO15, HDHREF, VDVS						
V_{IL}	LOW-level digital input voltage	-	0	-	$0.6V_{DDD}$	V
V_{IH}	HIGH-level digital input voltage	-	$0.7V_{DDD}$	-	V_{DDD}	V
V_{OL}	LOW-level digital output voltage	I_{OL} = 4 mA	0	-	0.4	V
V_{OH}	HIGH-level digital output voltage	I_{OH} = –4 mA	V_{DDD} – 0.4	-	V_{DDD}	V
C_i	input capacitance	-	-	2.5	-	pF
$C_{o(L)(max)}$	maximum output load capacitance	- [1]	-	-	30	pF
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; $V_{OH} = V_{DDD}$ – 0.4	4	-	-	mA
I_{OH}	HIGH-level output current	$V_{OH} = V_{DDD}$ – 0.4	–4	-	-	mA
I_{OZ}	3-state output leakage current	V_O = 0; $V_O = V_{DDD}$	-	-	1	µA
I_{IL}	LOW-level input current	V_I = 0	-	-	1	µA
I_{IH}	HIGH-level input current	$V_I = V_{DDD}$	-	-	1	µA
IO16 to IO23, IO0/IRQ16, IO1/IRQ17, IO2/IRQ18, IO3/IRQ19, IO4/IRQ20, IO5/IRQ21, IO6/IRQ22, IO7/IRQ23						
V_{IL}	LOW-level digital input voltage	-	0	-	$0.3V_{DDD}$	V
V_{IH}	HIGH-level digital input voltage	-	$0.7V_{DDD}$	-	V_{DDD}	V
V_{OL}	LOW-level digital output voltage	I_{OL} = 2 mA	0	-	0.4	V
V_{OH}	HIGH-level digital output voltage	I_{OH} = –2 mA	V_{DDD} – 0.4	-	-	V
C_i	input capacitance	-	-	2.3	-	pF
$C_{o(L)(max)}$	maximum output load capacitance	-	-	-	30	pF
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; $V_{OH} = V_{DDD}$ – 0.4	2	-	-	mA
I_{OH}	HIGH-level output current	$V_{OH} = V_{DDD}$ – 0.4	–2	-	-	mA

Table 6: Operating characteristics…*continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{OZ}	3-state output leakage current	V_O = 0; $V_O = V_{DDD}$	-	-	1	µA
I_{IL}	LOW-level input current	V_I = 0	-	-	1	µA
I_{IH}	HIGH-level input current	$V_I = V_{DDD}$	-	-	1	µA
IO4 to IO31						
V_{IL}	LOW-level digital input voltage	-	0	-	0.8	V
V_{IH}	HIGH-level digital input voltage	-	2.0	-	5.5	V
V_{OL}	LOW-level digital output voltage	I_{OL} = 2 mA	-	-	0.4	V
V_{OH}	HIGH-level digital output voltage	I_{OH} = –2 mA	V_{DDD} – 0.4	-	V_{DDD}	V
C_i	input capacitance	-	-	1.5	-	pF
$C_{o(L)(max)}$	maximum output load capacitance	-	-	-	30	pF
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; $V_{OH} = V_{DDD}$ – 0.4	2	-	-	mA
I_{OH}	HIGH-level output current	$V_{OH} = V_{DDD}$ – 0.4	–2	-	-	mA
I_{OZ}	3-state output leakage current	V_O = 0; $V_O = V_{DDD}$	-	-	1	µA
I_{IL}	LOW-level input current	V_I = 0	-	-	1	µA
I_{IH}	HIGH-level input current	$V_I = V_{DDD}$	-	-	1	µA
IO32 to IO39						
V_{IL}	LOW-level digital input voltage	-	0	-	0.8	V
V_{IH}	HIGH-level digital input voltage	-	2.0	-	5.5	V
V_{OL}	LOW-level digital output voltage	I_{OL} = 1 mA	0	-	0.4	V
V_{OH}	HIGH-level digital output voltage	I_{OH} = –1 mA	V_{DDD} – 0.4	-	V_{DDD}	V
C_i	input capacitance	-	-	1.4	-	pF
$C_{o(L)(max)}$	maximum output load capacitance	-	-	-	30	pF
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; $V_{OH} = V_{DDD}$ – 0.4	1	-	-	mA
I_{OH}	HIGH-level output current	$V_{OH} = V_{DDD}$ – 0.4	–1	-	-	mA
I_{OZ}	3-state output leakage current	V_O = 0; $V_O = V_{DDD}$	-	-	1	µA
I_{IL}	LOW-level input current	V_I = 0	-	-	1	µA
I_{IH}	HIGH-level input current	$V_I = V_{DDD}$	-	-	1	µA
I^2C-bus I/Os						
SCL and SDA						
V_{IL}	LOW-level digital input voltage	-	0	-	$0.3V_{DDD}$	V
V_{IH}	HIGH-level digital input voltage	-	0	-	$0.3V_{DDD}$	V
V_{hys}	hysteresis voltage	-	$0.005V_{DDD}$	-	-	V
V_{OL}	LOW-level digital output voltage	I_{OL} = 3 mA	-	-	0.4	V
C_i	input capacitance	-	-	3.2	-	pF
$C_{o(L)(max)}$	maximum output load capacitance	- [1]	-	-	400	pF

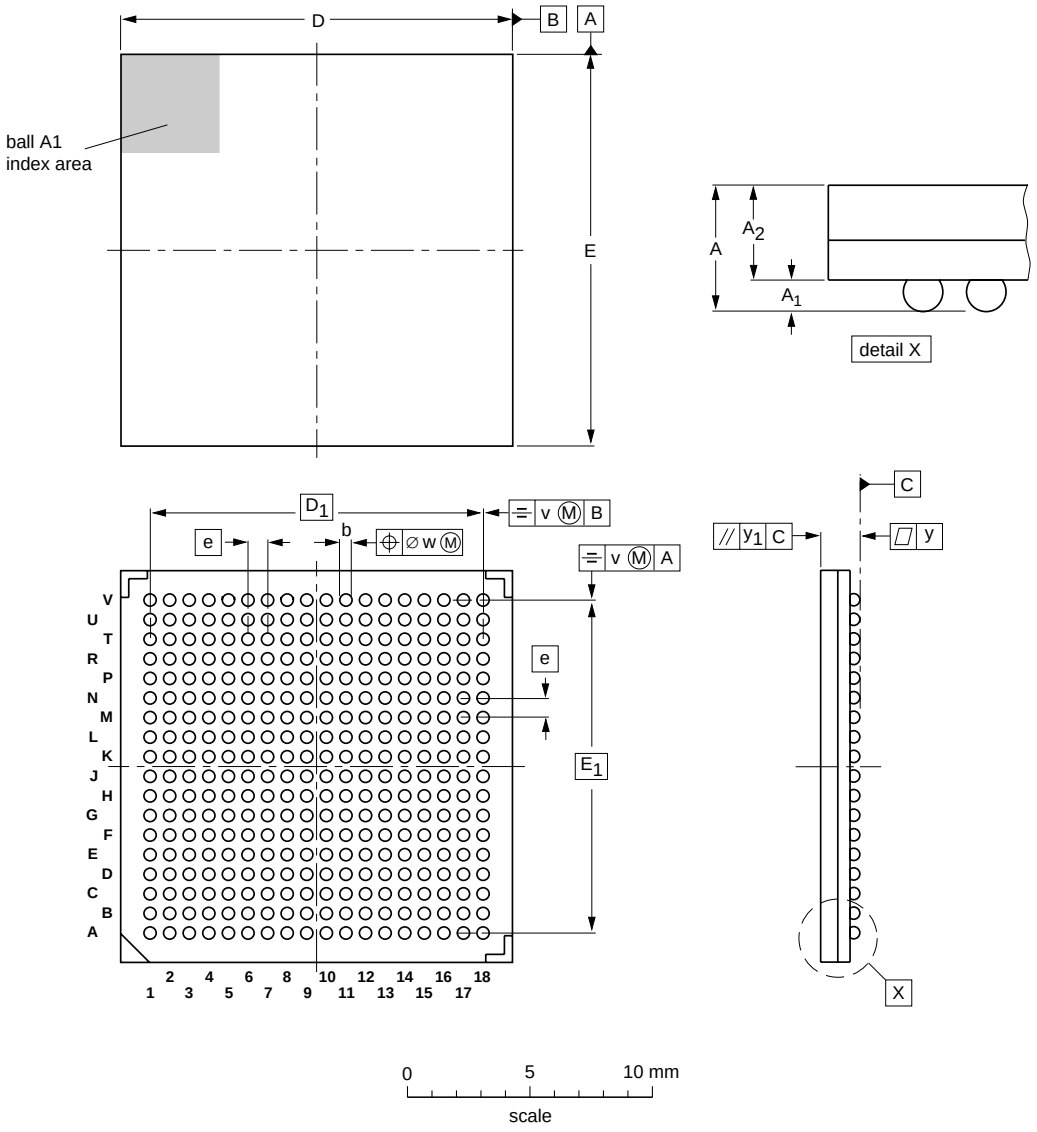
Table 6: Operating characteristics *…continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{OZ}	3-state output leakage	$V_O = 0$; $V_O = V_{DDD}$	-	-	1	µA
I_{IL}	LOW-level input current	$V_I = 0$	-	-	1	µA
I_{IH}	HIGH-level input current	$V_I = V_{DDD}$	-	-	1	µA

[1] The maximum capacitance value given does not take into account the signal frequency. For critical signals the maximum capacitance has to be weighted according to the signal frequency and external devices constraints.

9. Package outline

LFBGA324: plastic low profile fine-pitch ball grid array package; 324 balls; body 16 x 16 x 1.2 mm SOT571-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	b	D	D_1	E	E_1	e	v	w	y	y_1
mm	1.70	0.45 0.35	1.35 1.05	0.55 0.45	16.1 15.9	13.6	16.1 15.9	13.6	0.8	0.15	0.1	0.12	0.10

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT571-1		MO-205				00-01-20

Fig 4. SOT571-1.

10. Soldering

10.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

10.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

10.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C. A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

10.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

10.5 Package related soldering information

Table 7: Suitability of surface mount IC packages for wave and reflow soldering methods

Package	Soldering method	
	Wave	Reflow [1]
BGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable [2]	suitable
PLCC [3], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended [3] [4]	suitable
SSOP, TSSOP, VSO	not recommended [5]	suitable

[1] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[2] These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).

[3] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[4] Wave soldering is only suitable for LQFP, QFP and TQFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[5] Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

11. Revision history

Table 8: Revision history

Rev	Date	CPCN	Description
01	20000420	-	Objective specification; initial version

12. Data sheet status

Datasheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued data sheet before initiating or completing a design.

13. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

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