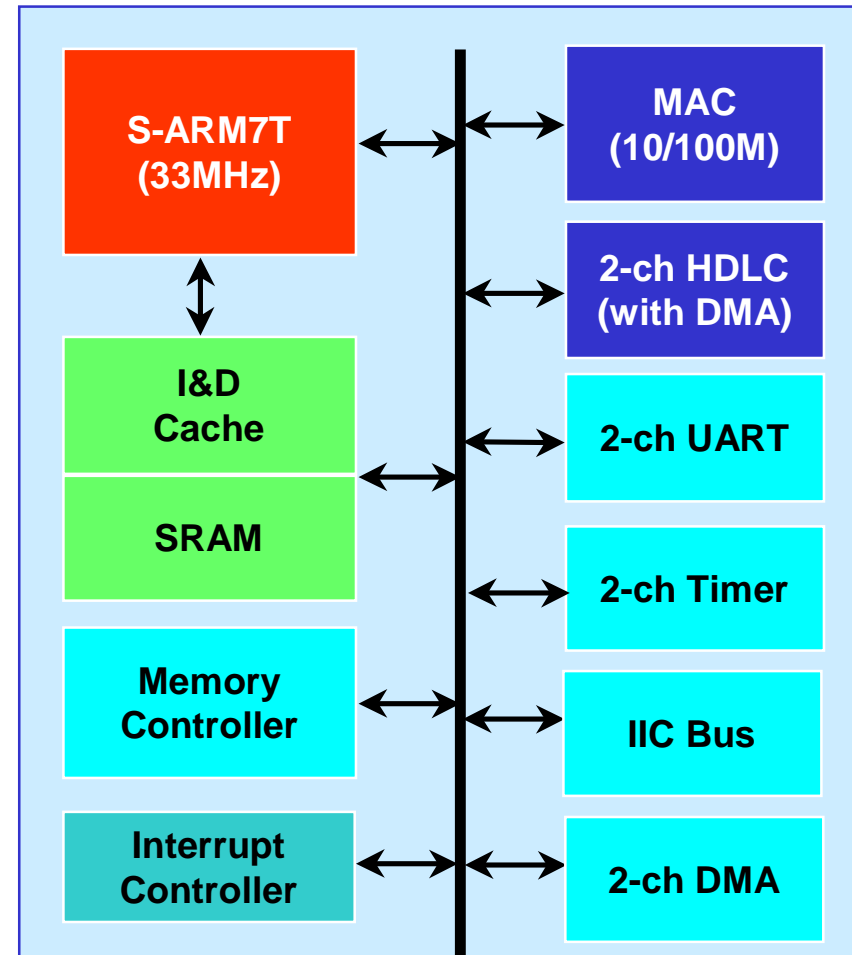
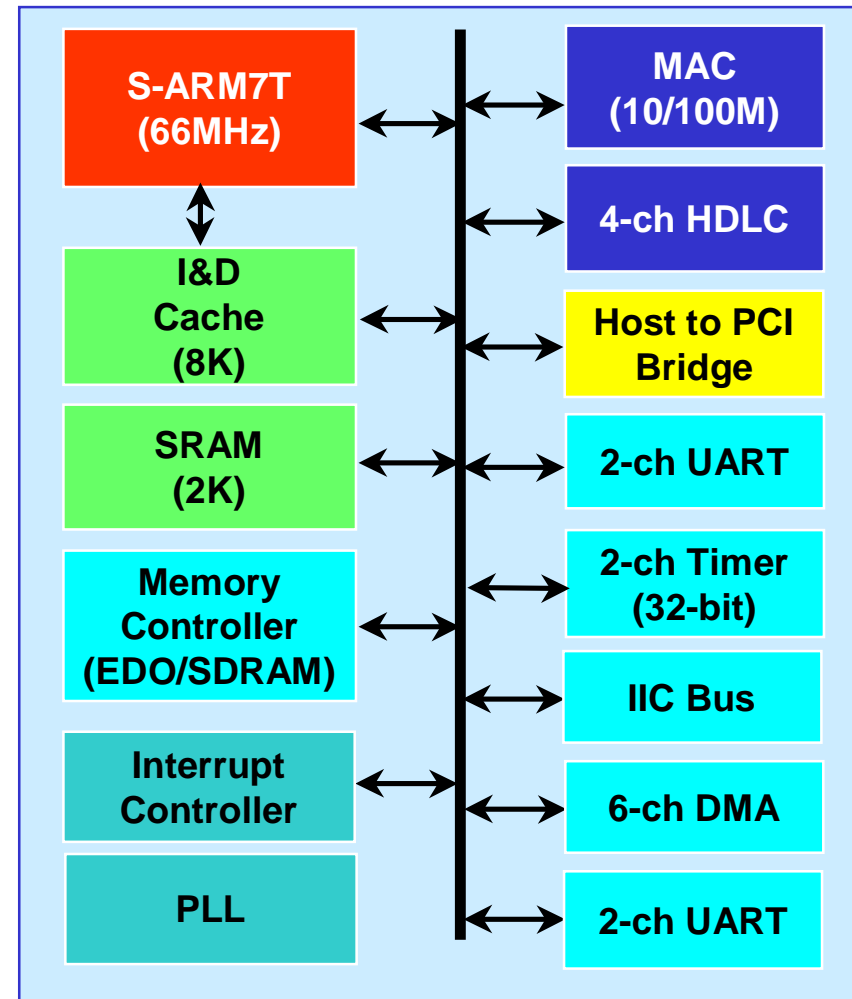
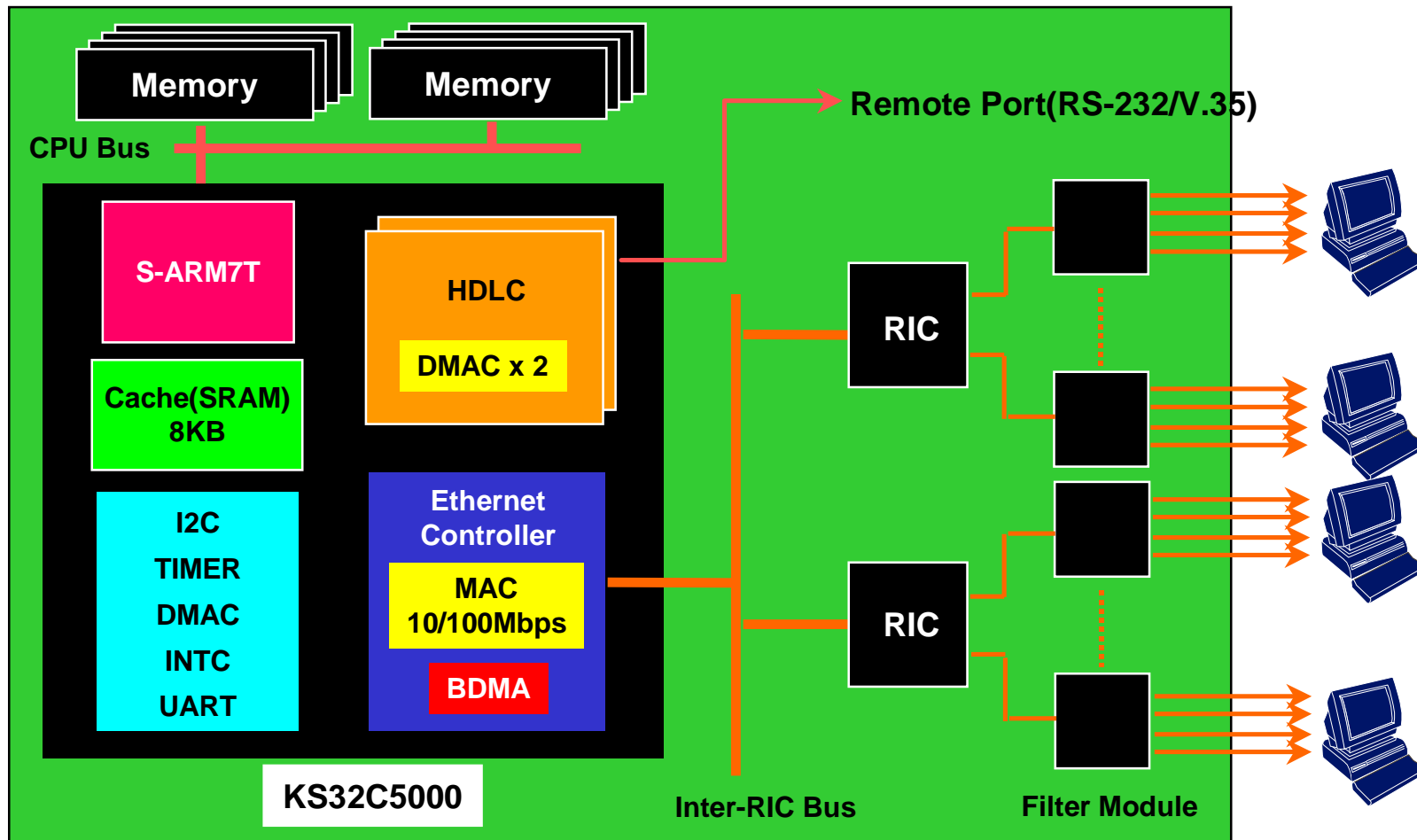


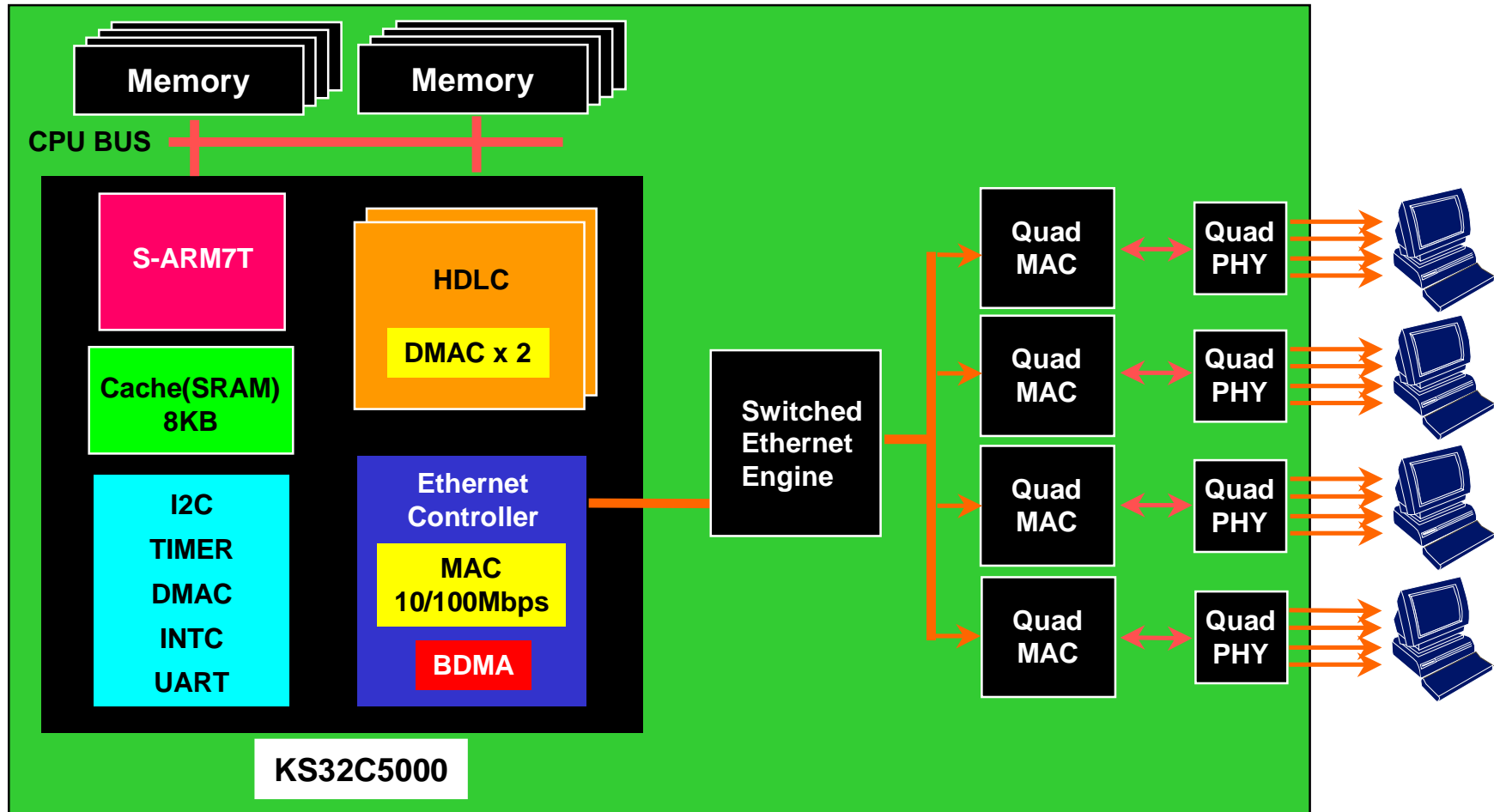
- 32-bit S-ARM7T RISC Core
- 8 Kbytes Unified Cache / SRAM(8K Cache, 4K/4K Cache/SRAM, or 8K SRAM Mode)
- 2-channel UART
- 2-channel HDLC with DMA
- IIC Bus (Simple master)
- 2-channel DMA
- 2-channel 32-bit Timers
- 10/100Mbps Ethernet Controller(MAC)
- Interrupt controller
- Fast Page/EDO Mode DRAM Controller with CBR Refresh and Self Refresh Control
- SRAM/ROM Controller
- Interrupt controller
- 208 QFP
- M/P : '98. 5(E/S : Available)

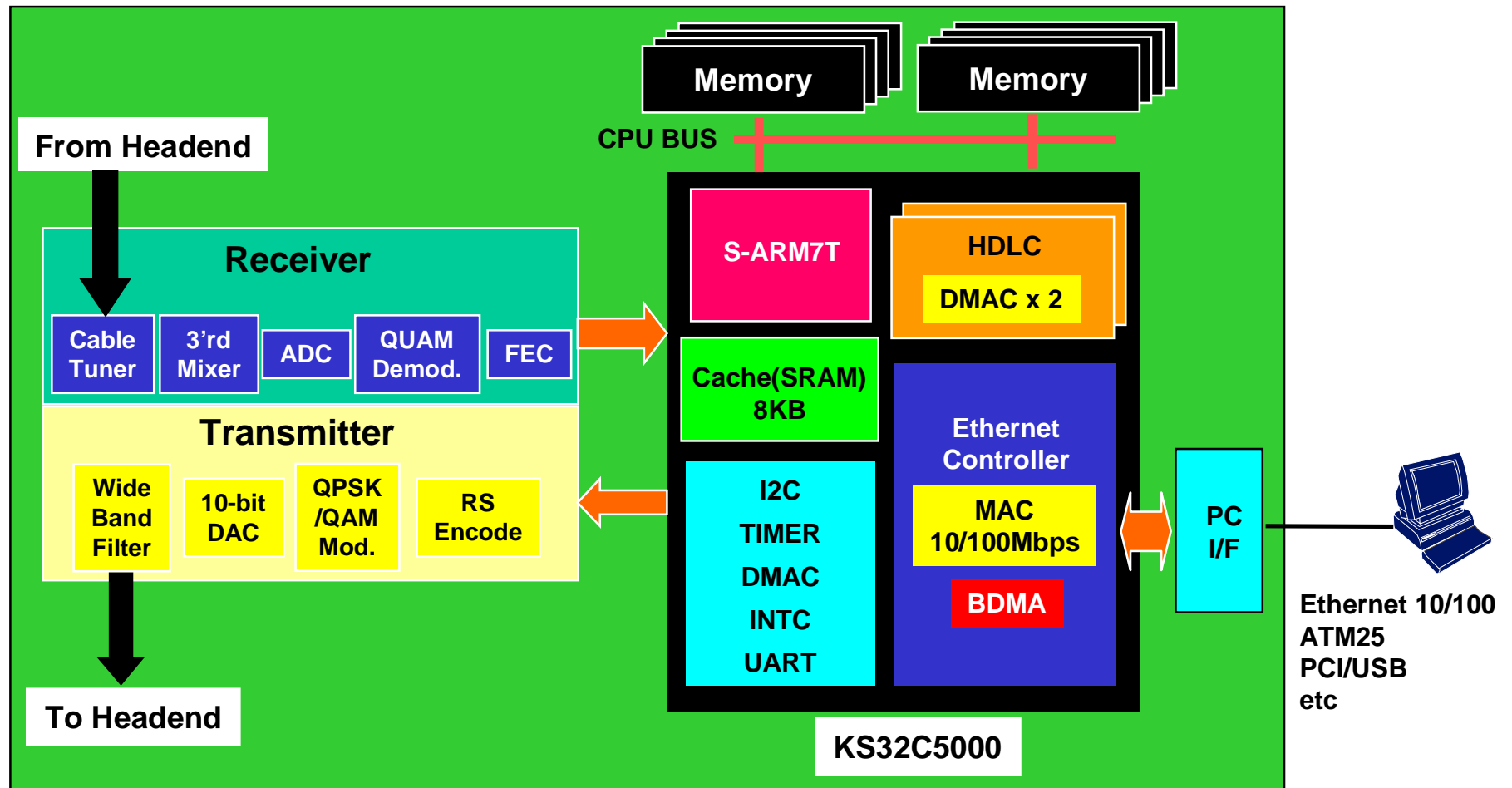


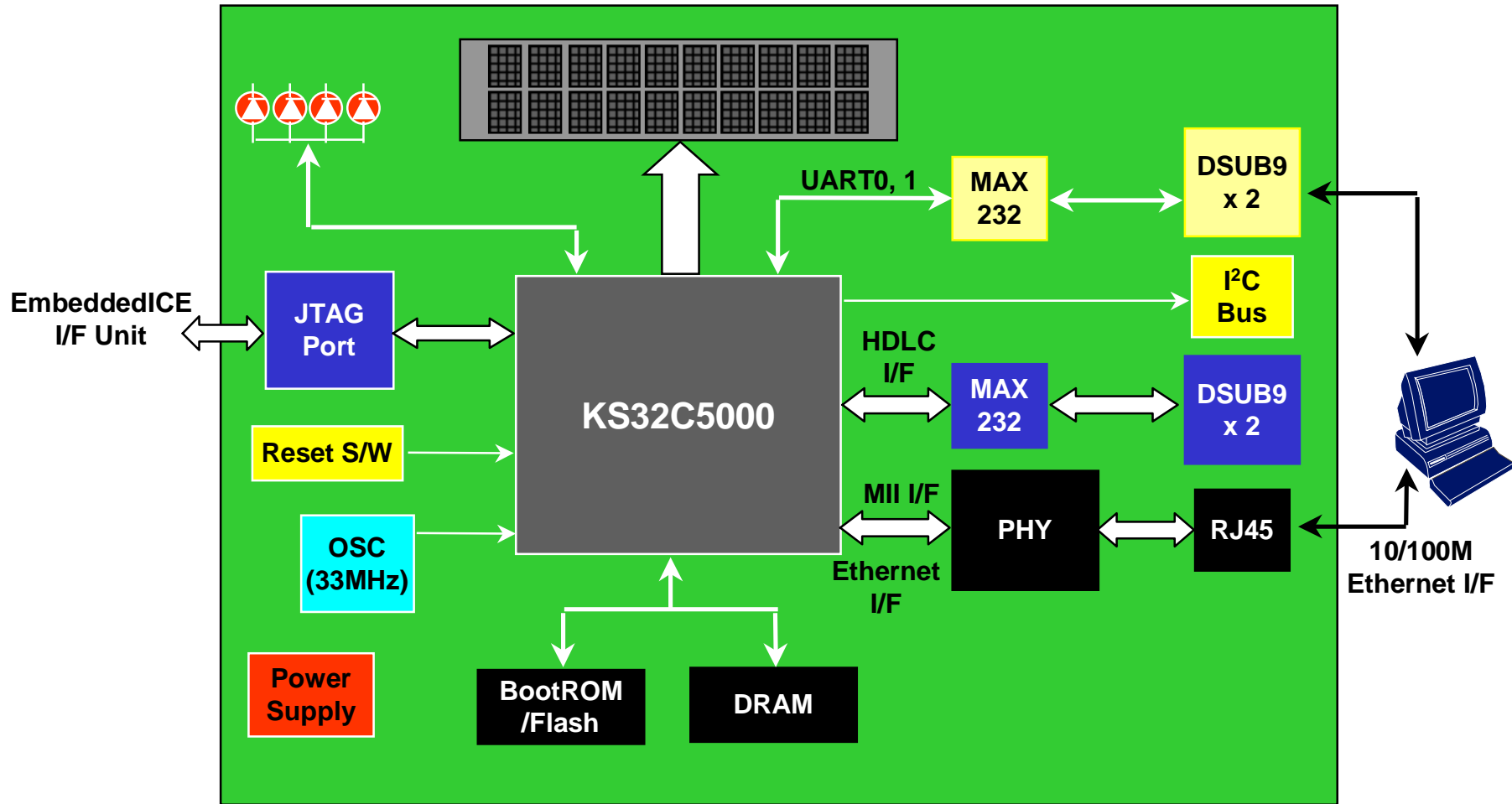
- 32-bit S-ARM7T RISC Core(66MHz@3.3V)
- 8 Kbytes Unified Cache
- **4Kbytes SRAM**
- 2-channel UART
- **4-channel HDLC with dedicated DMA**
- IIC Bus (Simple master)
- **6-channel DMA**
- 2-channel Timers(32-bit)
- **Watchdog Timer(16-bit)**
- 10/100Mbps Ethernet Controller(MAC)
- **Host-to-PCI bridge unit**
- 4 External bus request
- Interrupt controller
- EDO Mode DRAM/**Synchronous DRAM Controller** with CBR Refresh and Self Refresh Control
- SRAM/ROM/Flash Controller
- 22 Programmable I/O ports
- **PLL**
- **256 QFP**
- **M/P : '99. 3(E/S : '98. 12)**











■ RTOS

- pSOS : Available
- VxWorks : June, 1998

■ Drivers

- Ethernet Controller
(10/100M MAC)
- HDLC
- UART
- DMA
- IIC bus interface
- Timer
- Interrupt
- Etc.

■ Protocol supports

- Complete TCP/IP Stack and UDP, DHCP, BOOTP, TFTP, etc.
- SNMP MIB-II
- Web Page Support
 - HTTP Client and Server
 - FTP Client and Server
- Internet Mail Protocol
 - POP3 (VxWorks)
 - SMTP (pSOS, VxWorks)

■ Optional Protocol

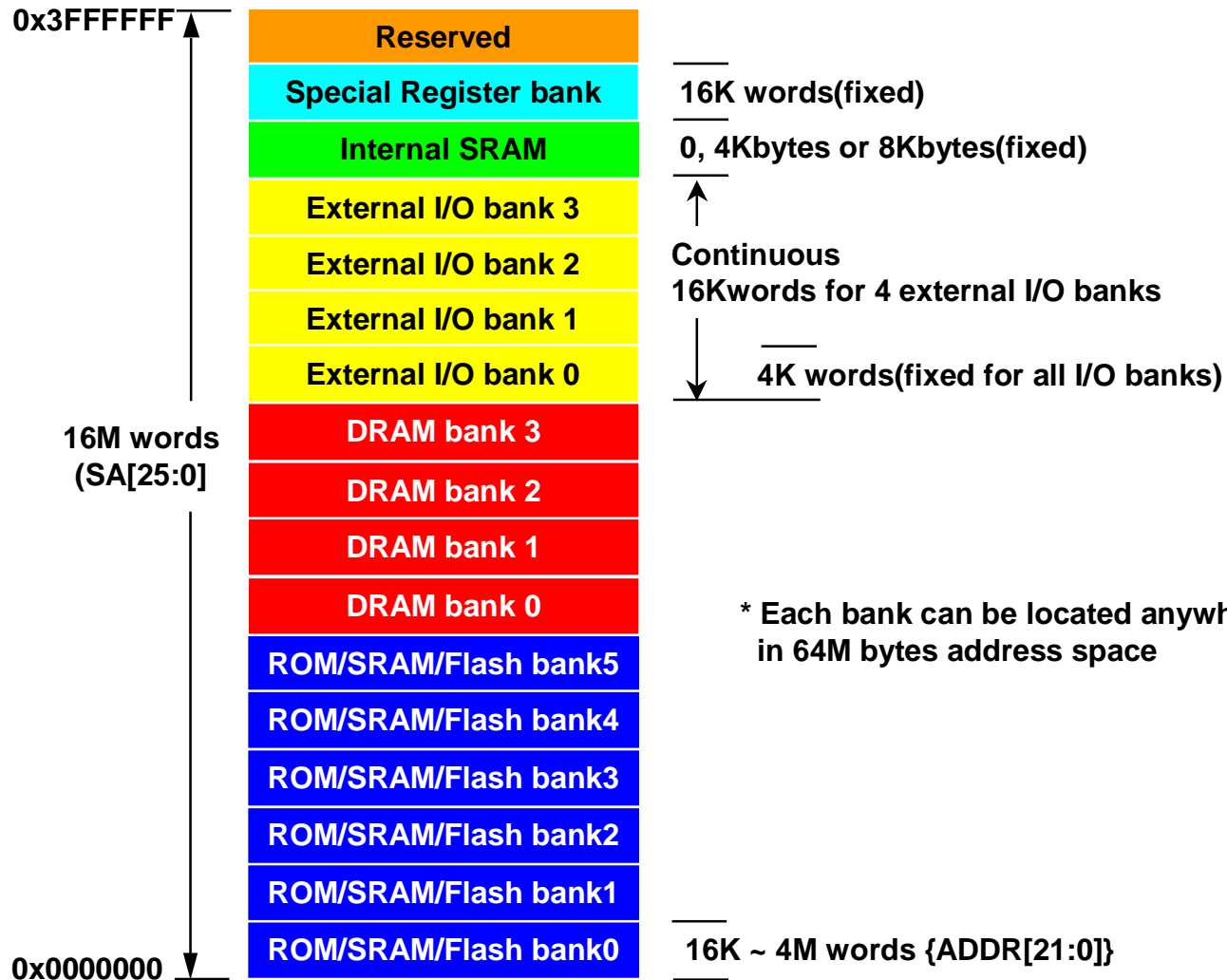
- PPP
- JAVA

- **Most suitable solution for networks**
 - **Cost effective system solution**
 - **Built-in ethernet controller(MAC) and HDLC**
 - **Higher memory efficiency**
 - **Various peripherals such as IIC bus, UART, DMA, etc.**
- **Higher performance and Lower power consumption**
 - **29MIPS @ 33MHz, 37mW / MHz**
- **Establishing full line-up from Low to High-end**
 - **33MHz to 150MHz**
- **Real time engineering supports**
 - **Supports Easy-to-Develop S/W drivers**
 - **User friendly development environment**
 - **Proffer useful document / evaluation board for system development**
 - **Powerful technical support**

Competitor	CPU	Performance	Cache	MAC	DMA	HDLC	PKG
i960Cx	i960	80MIPS(@40Mhz)	4K I-cache 1K D-cache	-	4-ch	-	168PGA/196QFP
i960Hx	i960	150MIPS(@75MHz)	16K I-cache 8K D-cache	-	-	-	168PGA/208QFP
MPC821	PowerPC	66MIPS(@50MHz)		10M	2-ch	1-ch	256BGA
MPC823	PowerPC	66MIPS(@50MHz)		10M	2-ch	1-ch	256BGA
MPC860T	PowerPC	52MIPS(@40MHz)	4K I-cache 4K D-cache	10/100M	16-ch	1-ch	240QFP/255BGA
RV4640	R4000	175MIPS(@133MHz)	8K I-cache 8K D-cache	-	-	-	128QFP
RV4700	R4000	230MIPS(@175MHz)	16K I-cache 16K D-cache	-	-	-	179PGA
NET+ARM	ARM7TDMi	15MIPS		10/100M	10-ch	-	208QFP
KS32C5000	ARM7TDMi	29MIPS(@33MHz)	8K I/D-cache	10/100M	6-ch	2-ch	208QFP
KS32C5100*	ARM7TDMi	58MIPS(@66MHz)	8K I/D-cache	10/100M	4-ch	4-ch	256QFP

- System Manager
- System Memory Map
- Cache(SRAM)
- Ethernet Controller (100/10M MAC)
- HDLC
- UART
- Timers
- DMA
- Input / Output
- Interrupts

- 16M words addressing range supports
- External 8/16/32-bit bus width supports
- Glueless interface for external memory supports
 - 4 banks of DRAM supports
 - 6 banks of ROM/SRAM/Flash supports
 - 4 banks of external I/O
 - 1 bank of special register
- CBR(CAS before RAS) refresh, Fast page mode, and EDO (Extended Data Out) mode for DRAM access
- Programmable bank start/end definition to provide consecutive memory map
- Programmable bank size (64K to 4M words for DRAM/ROM/SRAM, 4K to 16K words for external I/O)
- Programmable access cycles for memory bank(2 to 7 cycles)
- One external bus master with bus request/grant pins



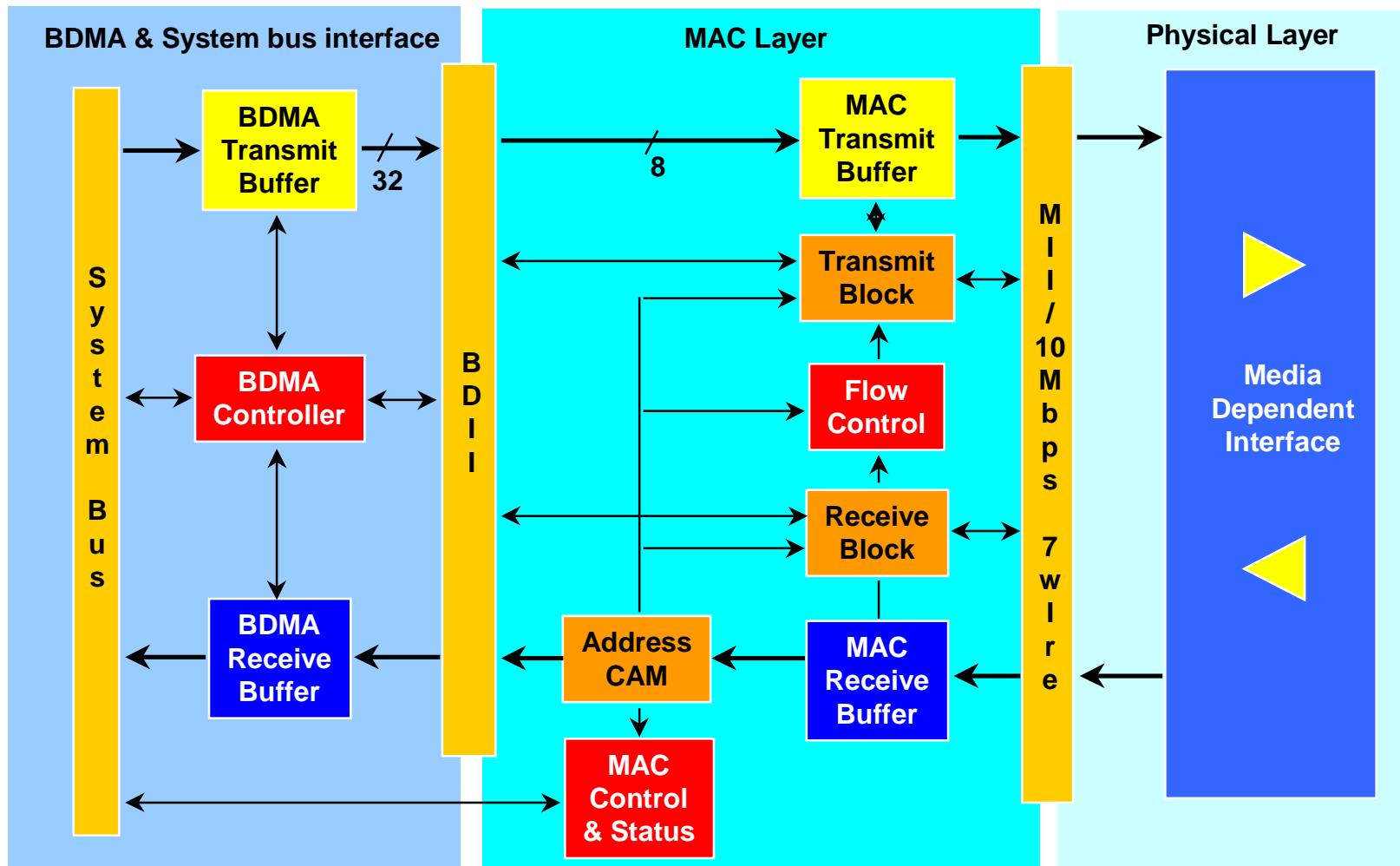
- Cost-effective connection with external RIC/Ethernet backbone
- Buffered DMA engine using burst mode
- BDMA Tx/Rx buffer(256bytes/256bytes)
- MAC Tx/Rx FIFO(80bytes/16bytes)
Retransmit after collision without DMA request.
Handle DMA latency
- Data alignment logic
- Endian translation
- Supports old/new media
Compatible with existing 10Mbps networks
- 100/10Mbps operations
- Full **IEEE802.3/u** compatible
- Modified MII / modified 7-wire interface
- Station management signaling
external physical layer configuration
and link negotiation
- On chip CAM(21 addresses)
- Full duplex mode / PAUSE operation
Double bandwidth/ H/W support for full
duplex flow control
- Long/Short packet mode
- Pad generation

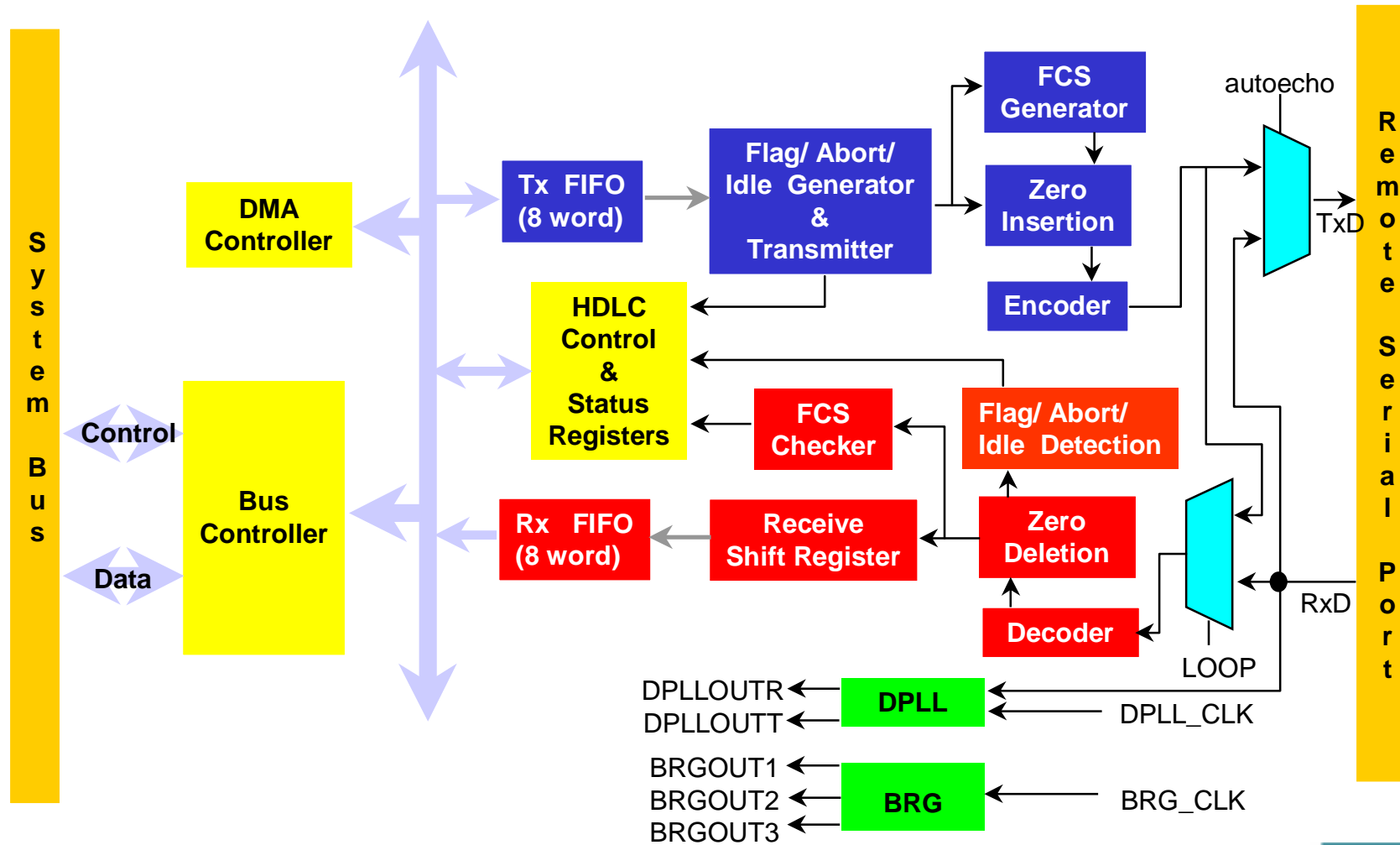
MAC : Media Access Control

RIC : Repeater IC

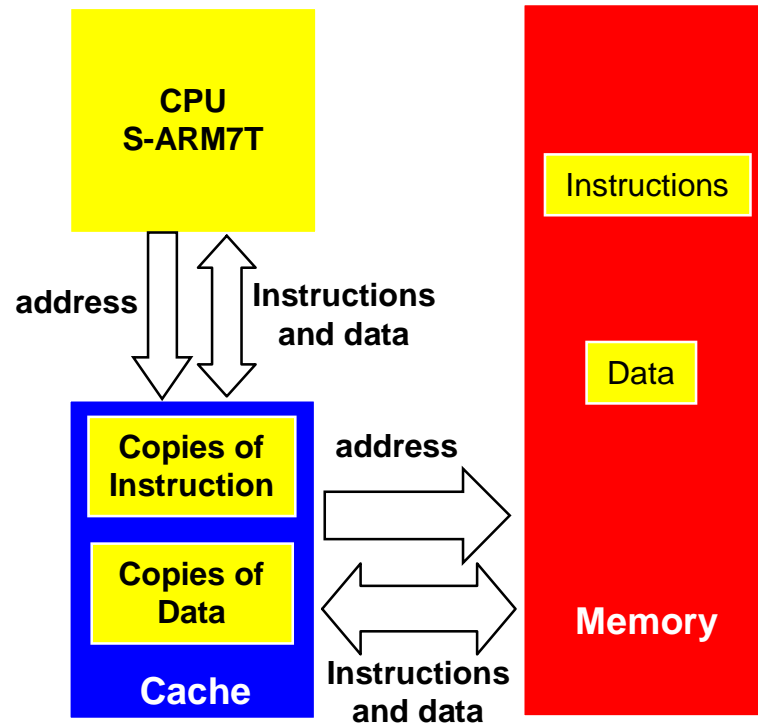
II : Media Independent Interface

CAM : Content Addressable Memory



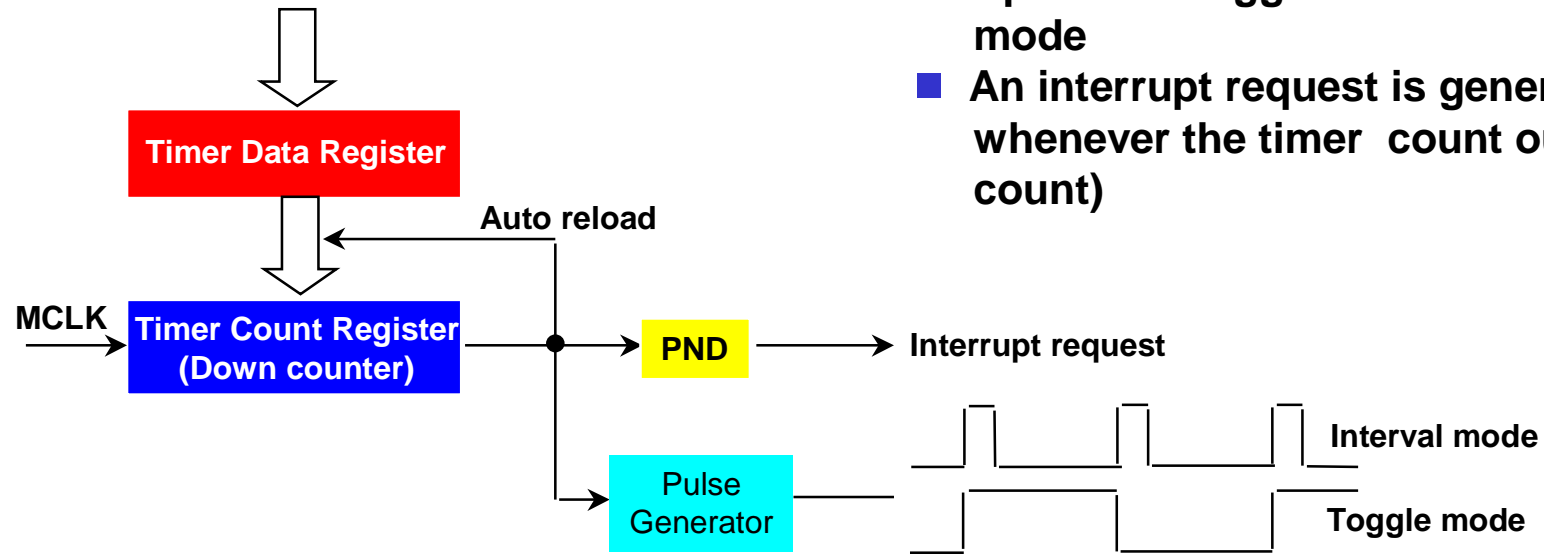


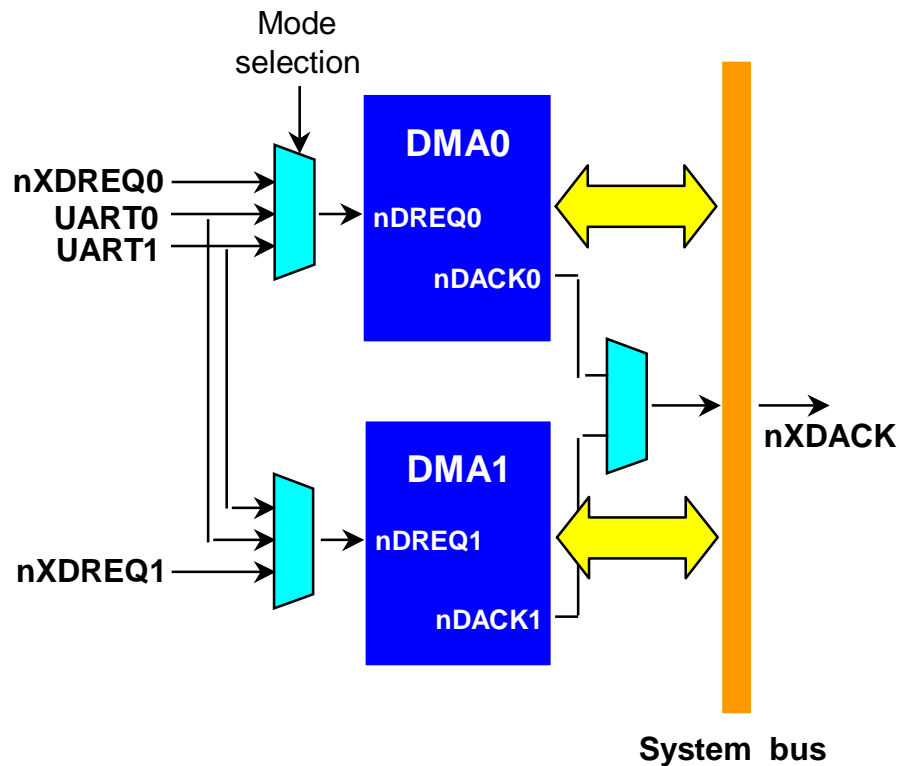
- Protocol features
 - Flag detection and synchronization
 - Zero insertion and deletion
 - Idle detection and transmission
 - FCS encoding and detection(16-bit)
 - Abort detection and transmission
- Address search mode
- No-CRC mode
- Automatic CRC generator preset
- Digital PLL block for clock recovery
- Baud rate generator
- NRZ/NRZI/FM/Manchester data formats for Tx/Rx
- Loop-back and auto echo mode
- Selectable 1-word or 4-word data transfer mode
- Tx and Rx FIFOs 8-word depth
- Data alignment logic
- Endian translation
- Programmable interrupts
- Modem interface
- Up to 4Mbps using external receive clock
- Up to 2Mbps with 32MHz MCLK for FM encoding using DPLL
- Up to 1Mbps with 32MHz MCLK for NRZI encoding using DPLL
- 2-ch DMA controller
 - 2-ch for HTxFIFO and HRxFIFO
 - 4-word burst transfer mode
 - Count for counting transferred bytes from HRxFIFO to memory
- HDLC frame length based on octets



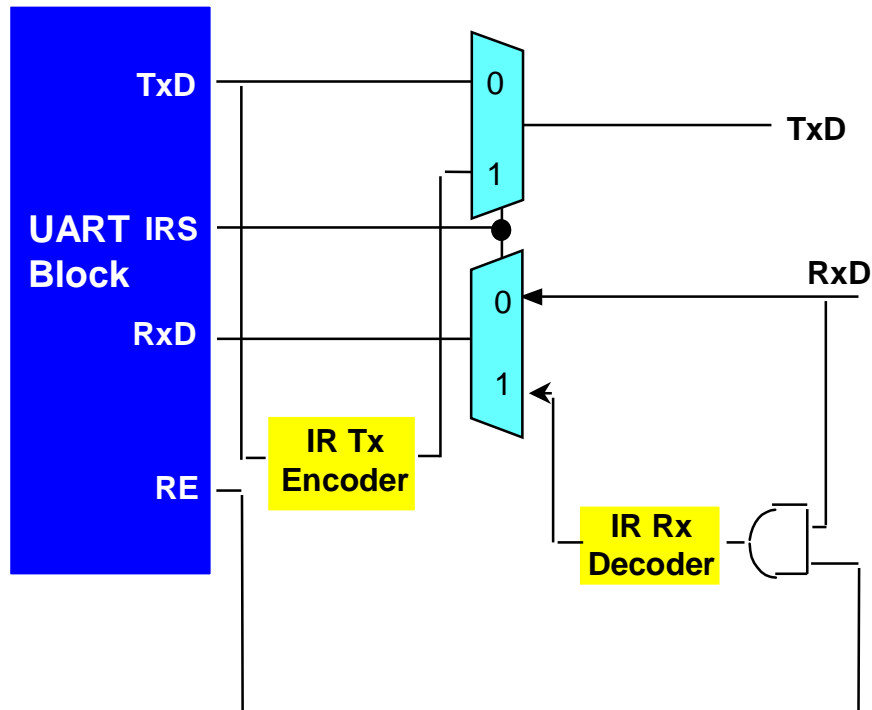
- 8K Byte (2048 instructions or data /32, 4096 instruction or data /16)
- 2 Way set associative
- Single cycle access
- Can define two non-cacheable regions for data only
- Main memory updated by “Write through four write buffers”
- Software/Hardware selectable for cache disable

- Two 32-bit programmable timers
- Operate in toggle mode and interval mode
- An interrupt request is generated whenever the timer count out(down count)





- Two general DMA channels
 - Memory-from/to-memory
 - Serial port(UART)-from/to-memory
- DMA operation can be triggered by S/W and/or by external DMA requests
- Operation can also be stopped and then restarted by S/W
- S/W polling and/or internal DMA interrupt can be used to recognize the completed DMA operation
- 8,16,and 32bit data transfers
- Address can be generated to Big endian format



- Two independent channels
- DMA or interrupt based operation
- 5-, 6-, 7-, or 8-bit data to be transmitted or received per frame
- Parity mode: none, odd, even, parity forced/checked 1, 0
- Programmable baud rate
 - $\text{Baud rate} = \text{Baud Clock} / (\text{Divisor} \times 16)$
- Support IR (Infra-red) Tx/Rx : IrDA(Infra-Red Data Acquisition)
 - In IR mode, the Tx period is pulsed at a rate of $3/16$ that of the normal Tx rate(when THR = 0)
- Loop back mode for testing the UART

- **I/O (Input / Output)**
 - 18 programmable I/O ports
 - Each pin can be configured individually as input/output or I/O for a dedicated signal

- **Interrupt**
 - 20 source
 - 4 external
 - 16 internal
 - Normal or fast interrupt modes
 - IRQ (Interrupt request)
 - FIQ (Fast interrupt request)
 - Prioritized interrupt handling