SONY

CXP80P624A

CMOS 8-bit Single Chip Microcomputer

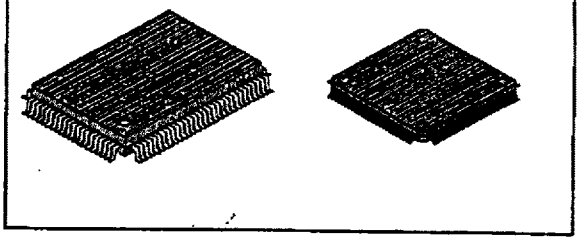
Description

The CXP80P624A is a CMOS 8-bit microcomputer which consists of A/D converter, serial interface (2-ch independently), timer/counter, time base timer, vector interruption, high precision timing pattern generation circuit, PWM generator, general purpose prescaler, PWM for tuner, VCR vertical sync separation circuit and the measuring circuit which measure signals of capstan FG and drum FG/PG and other servo systems, as well as basic configurations like 8-bit CPU, PROM, RAM and I/O port. They are integrated into a single chip.

Also this IC provides power on reset function, sleep/stop function which enables to lower power consumption.

CXP80P624A is the PROM-incorporated version of the CXP80624A with built-in mask ROM. This provides the additional feature of being able to write directly into the program. Thus, it is most suitable for evaluation use during system development and for small-quantity production.

100 pin QFP (Plastic) 100 pin VQFP (Plastic)



Structure

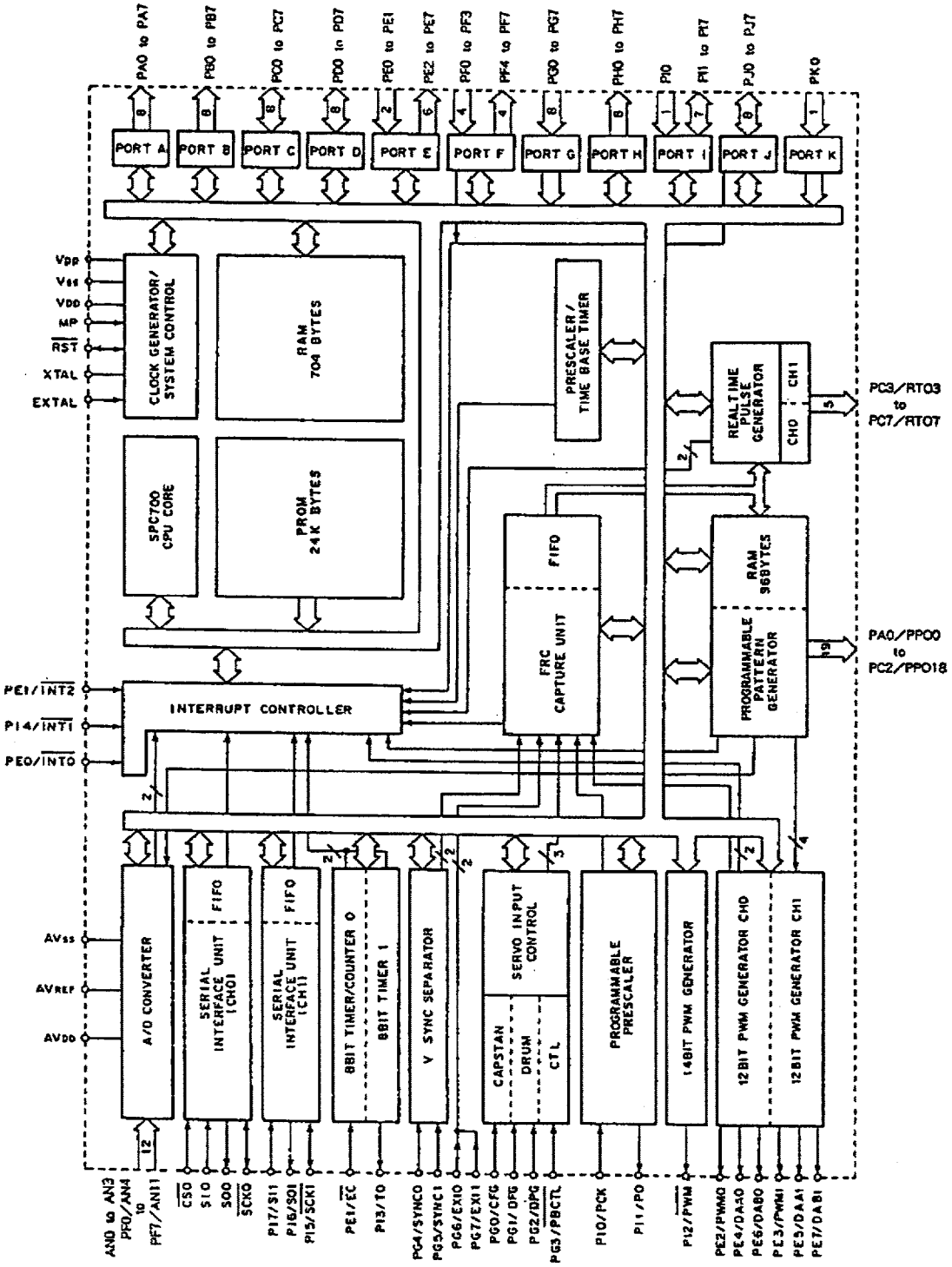
Silicon gate CMOS IC

Features

- A wide instruction set (213 instructions) which cover various types of data.
  - — 16-bit arithmetic instruction/multiplication and division instructions/boolean bit operation instruction
- Minimum instruction cycle — During operation 333ns/12MHz
- Incorporated PROM capacity — 24Kbytes
- Incorporated RAM capacity — 800bytes
- Peripheral functions
  - — A/D converter — 8-bit, 12-channel, successive approximation system (Conversion time: 26.7 µs/12MHz)
  - — Serial I/O with auto transfer mode — Incorporated 8-bit and 8-stage FIFO for data (1 to 8 bytes auto transfer) 2-channel independently
  - — Timer — 8-bit timer, 8-bit timer/counter, 19-bit time base timer
  - — High precision timing pattern generator
    - PPG 19 pins 32-stage programmable
    - RTG 5 pins 2-channel
  - — PWM/DA gate output — 12-bit, 2-channel (Repetitive frequency 46kHz/12MHz)
  - — Servo input control — Capstan FG, Drum FG/PG, CTL input
  - — VSYNC separator
  - — FRC capture unit — Incorporated 26-bit and 8-stage FIFO
  - — PWM output for tuner — 14-bit
  - — General purpose prescaler — 10-bit (System clock asynchronous)
- Interruption — 17 factors, 14 vectors, multi-interruption possible
- Standby mode — SLEEP/STOP
- Package — 100-pin plastic QFP/VQFP

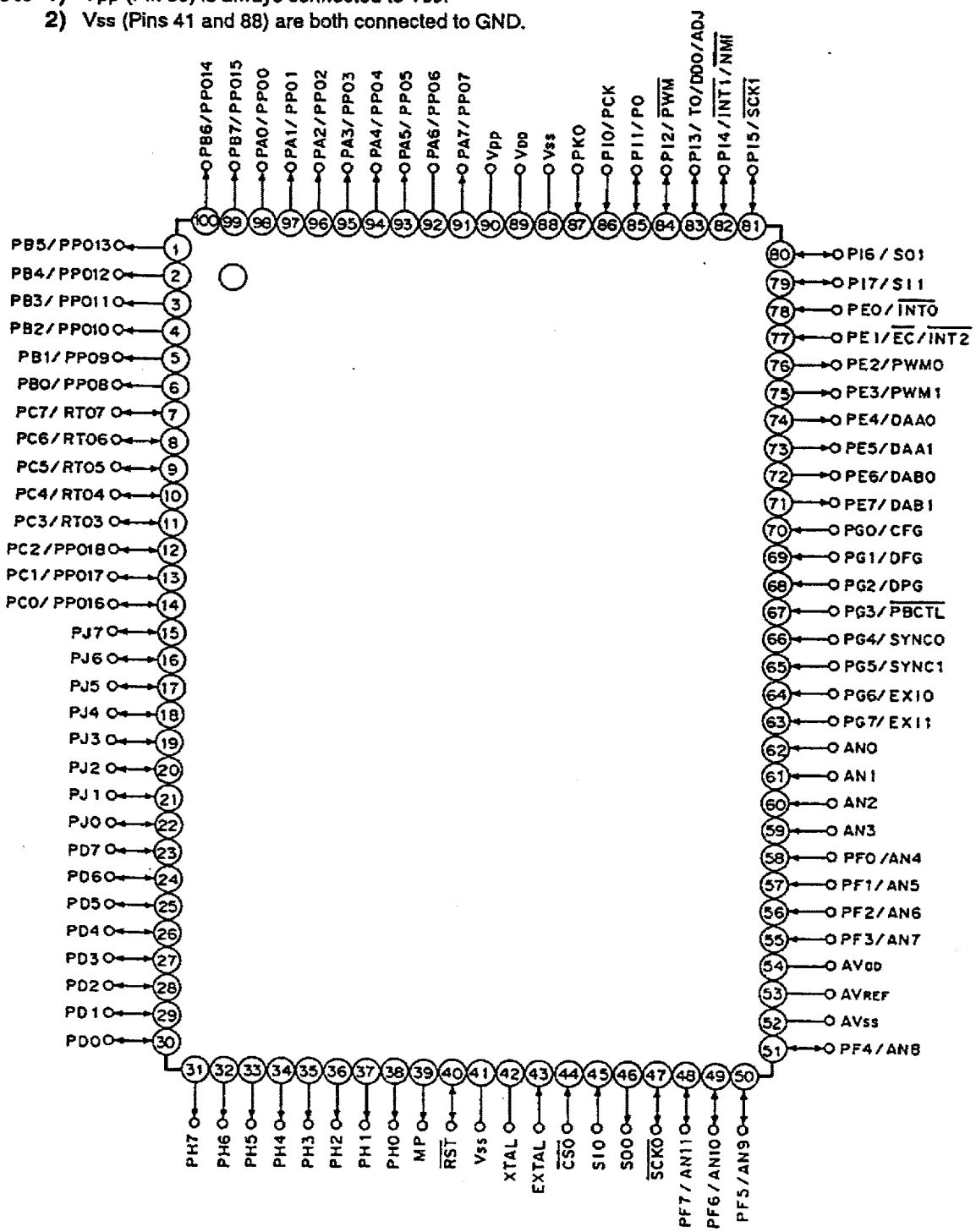
E92Z19 - ST

Block Diagram



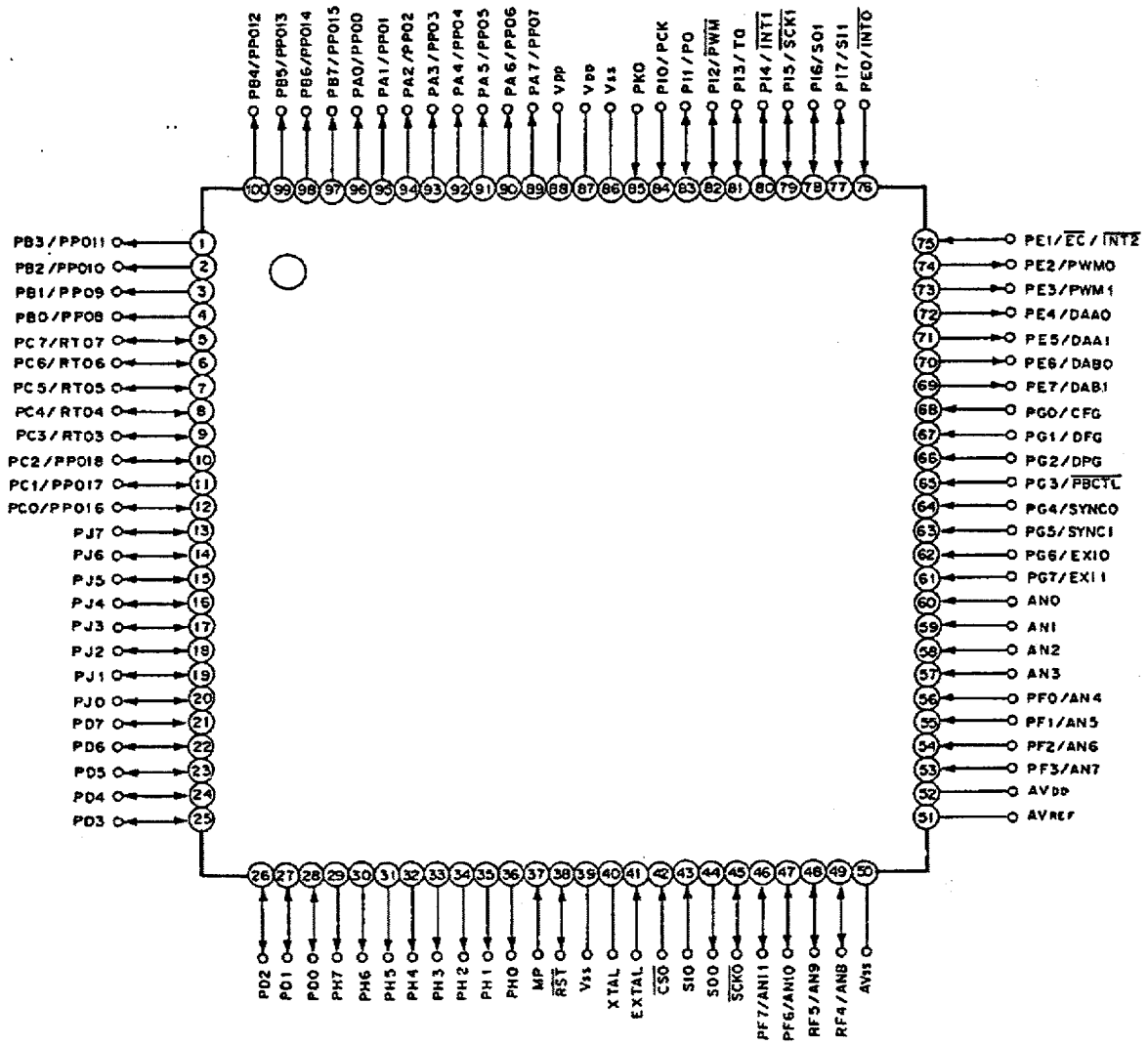
Pin Configuration 1 (Top View) 100 pin QFP package

Note 1) Vpp (Pin 90) is always connected to V_{DD}.
2) Vss (Pins 41 and 88) are both connected to GND.



Pin Configuration 2 (Top View) 100 pin VQFP package

Note 1) Vpp (Pin 88) is always connected to VDD.
2) Vss (Pins 39 and 86) are both connected to GND.

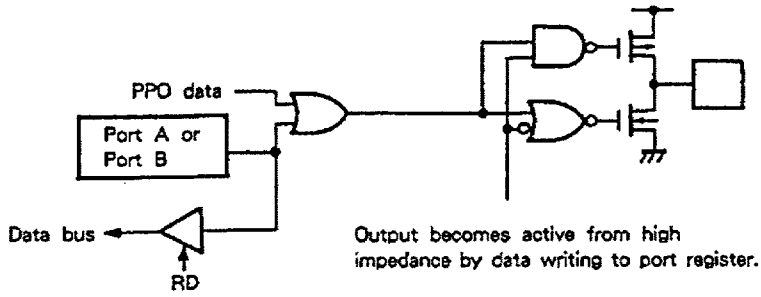
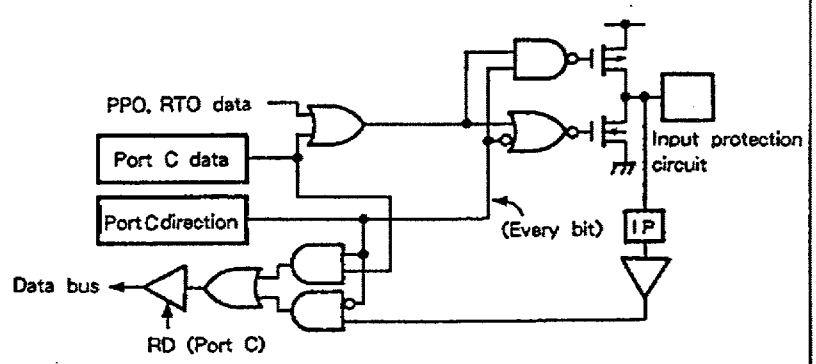
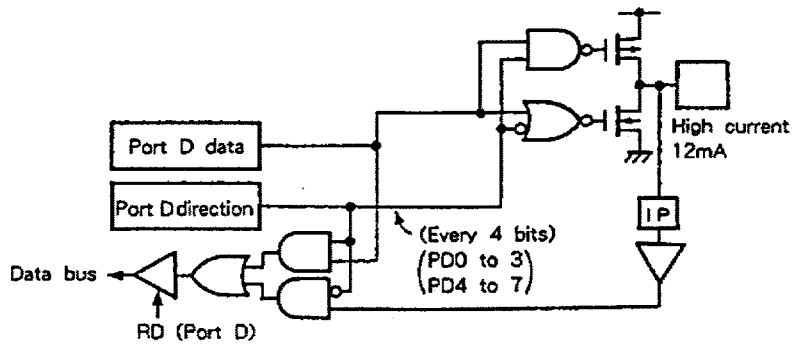


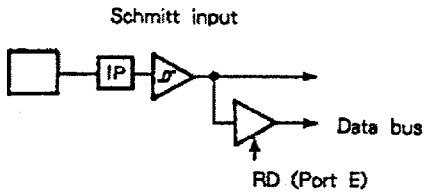
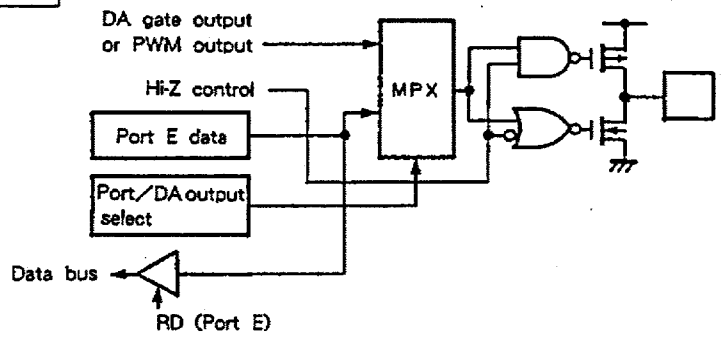
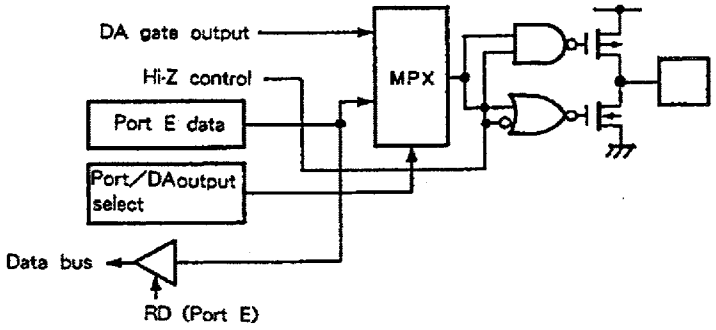
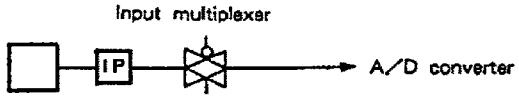
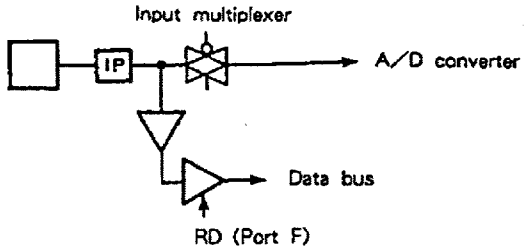
Pin Description

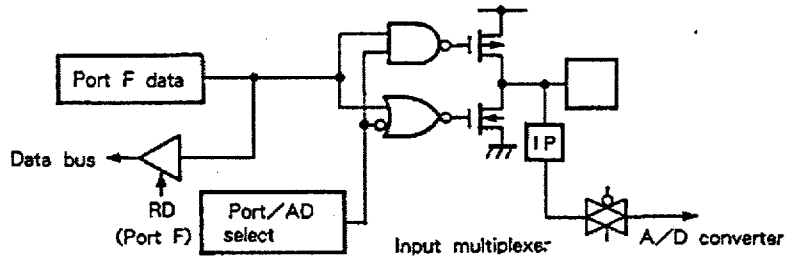
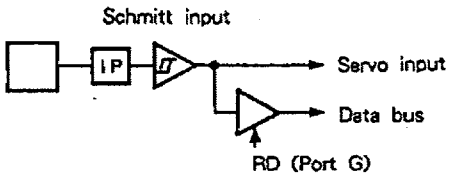
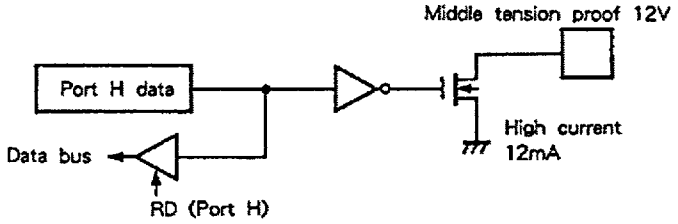
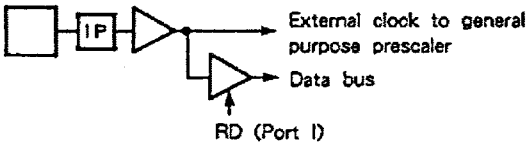
<table>
<tr><th>Symbol</th><th>I/O</th><th colspan="3">Description</th></tr>
<tr><td>PA0/PPO0
to
PA7/PPO7</td><td>Output/
Real time
Output</td><td>(Port A)
8-bit output port. Data is gated with PPO contents by OR-gate and they are output.
(8 pins)</td><td colspan="2" rowspan="3">Programmable pattern generator (PPG) output.
Functions as high precision real time pulse output port.
(19 pins)</td></tr>
<tr><td>PB0/PPO8
to
PB7/PPO15</td><td>Output/
Real time
Output</td><td>(Port B)
8-bit output port. Data is gated with PPO contents by OR-gate and they are output.
(8 pins)</td></tr>
<tr><td>PC0/PPO16
to
PC2/PPO18</td><td>I/O/
Real time
Output</td><td rowspan="2">(Port C)
8-bit input/output port, enables to specify input/output by bit unit. Data is gated with PPO or RTO contents by OR-gate and they are output.
(8 pins)</td></tr>
<tr><td>PC3/RTO3
to
PC7/RTO7</td><td>I/O/
Real time
Output</td><td colspan="2">Real time pulse generator (RTG) output. Functions as high precision real time pulse output port.
(5 pins)</td></tr>
<tr><td>PD0 to PD7</td><td>I/O</td><td colspan="3">(Port D)
8-bit input/output port. Enable to specify input/output by 4-bit unit.
Enables to drive 12mA sinc current.
(8 pins)</td></tr>
<tr><td>PE0/$\overline{\text{INT0}}$</td><td>Input</td><td rowspan="8">(Port E)
8-bit port. Lower 2 bits are input pins and upper 6 bits are output pins.
(8 pins)</td><td colspan="2">Input pin to request external interruption.
Active when falling edge.</td></tr>
<tr><td>PE1/$\overline{\text{EC}}$/$\overline{\text{INT2}}$</td><td>Input</td><td>External event input pin for timer/counter.</td><td>Input pin to request external interruption.
Active when falling edge.</td></tr>
<tr><td>PE2/PWM0</td><td>Output</td><td colspan="2" rowspan="2">PWM output pins.
(2 pins)</td></tr>
<tr><td>PE3/PWM1</td><td>Output</td></tr>
<tr><td>PE4/DAA0</td><td>Output</td><td colspan="2" rowspan="4">DA gate pulse output pins.
(4 pins)</td></tr>
<tr><td>PE5/DAA1</td><td>Output</td></tr>
<tr><td>PE6/DAB0</td><td>Output</td></tr>
<tr><td>PE7/DAB1</td><td>Output</td></tr>
<tr><td>AN0 to AN3</td><td>Input</td><td colspan="3">Analog input pins to A/D converter. (12 pins)</td></tr>
<tr><td>PF0/AN4
to
PF3/AN7</td><td>Input</td><td colspan="3" rowspan="2">(Port F)
Lower 4 bits are input port and upper 4 bits are output port.
Lower 4 bits also serve as standby release input pin.
(8 pins)</td></tr>
<tr><td>PF4/AN8
to
PF7/AN11</td><td>Output/Input</td></tr>
<tr><td>$\overline{\text{SCK0}}$</td><td>I/O</td><td colspan="3">Serial clock (CH0) input/output pin.</td></tr>
<tr><td>SO0</td><td>Output</td><td colspan="3">Serial data (CH0) output pin.</td></tr>
</table>

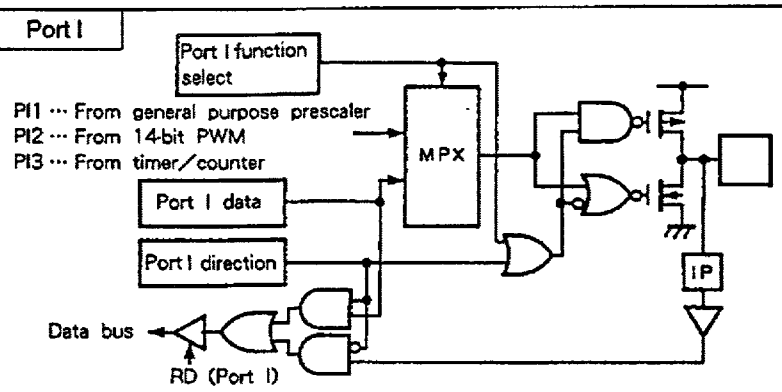
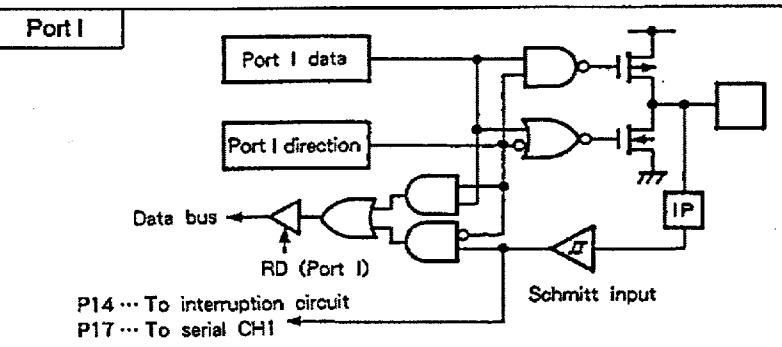
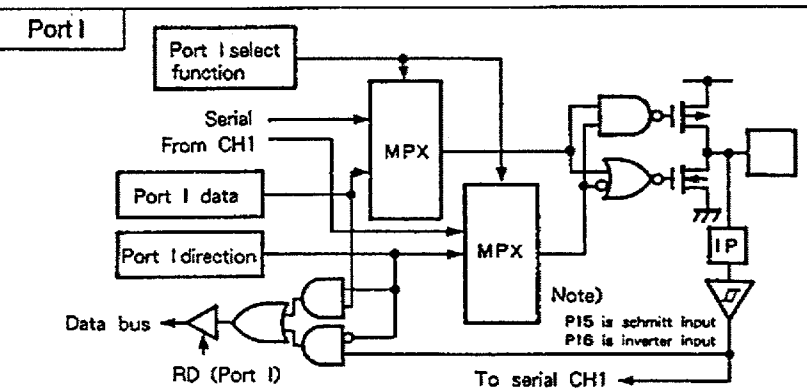
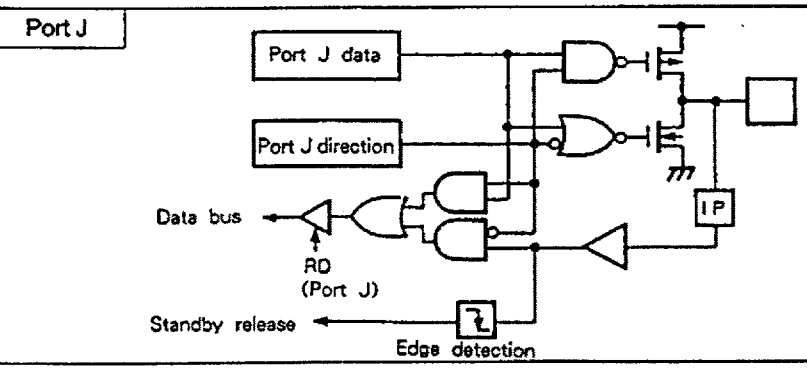
Symbol	I/O	Description	
SI0	Input	Serial data (CH0) input pin.	
$\overline{CS0}$	Input	Serial chip select (CH0) input pin.	
PG0/CFG	Input	(Port G) 8-bit input port. (8 pins)	Capstan FG input pin.
PG1/DFG	Input		Drum FG input pin.
PG2/DPG	Input		Drum PG input pin.
PG3/$\overline{PBCTL}$	Input		Playback CTL pulse input pin.
PG4/SYNC0	Input		Composite sync signal input pin.
PG5/SYNC1	Input		
PG6/EXI0	Input		External input pin to FRC capture unit.
PG7/EXI1	Input		
PH0 to PH7	Output	(Port H) 8-bit output port ; N-ch open drain output of middle tension proof (12V) and high current (12mA). (8 pins)	
PI0/PCK	Input	(Port I) Lower 1 bit is input port and upper 7 bits are input/output port. Input/output port can be specified by bit unit (8 pins).	External clock input pin of general purpose prescaler.
PI1/PO	I/O / Output		General purpose prescaler output pin.
PI2/$\overline{PWM}$	I/O / Output		14-bit PWM output pin
PI3/TO	I/O / Output		Timer/counter output pin. (duty=50%)
PI4/$\overline{INT1}$	I/O / Input		Input pin to request external interruption. Active when falling edge.
PI5/$\overline{SCK1}$	I/O / I/O		Serial clock (CH1) input/output pin.
PI6/SO1	I/O / Output		Serial data (CH1) output pin.
PI7/SI1	I/O / Input		Serial data (CH1) input pin.
PJ0 to PJ7	I/O	(Port J) 8-bit input /output port. Function as standby release input can be specified by bit unit. Input/output can be specified by bit unit.	
PK0	Input	Input port	
EXTAL	Input	Connecting pin of crystal oscillator for system clock. When supplying the external clock, input the external clock to EXTAL pin and input opposite phase clock to XTAL pin.	
XTAL	Output		
$\overline{RST}$	I/O	System reset pin of active "L" level. $\overline{RST}$ pin is input/output pin, which output "L" level by incorporated power on reset function when power on. (Mask option)	
MP	Input	Microprocessor mode input pin. Always connect to GND.	
AV_{DD}		Positive power supply pin of A/D converter.	
AV_{REF}	Input	Reference voltage input pin of A/D converter.	
AV_{SS}		GND pin of A/D converter.	
V_{DD}		Positive power supply pin.	
Vpp		Positive power supply pin for built-in PROM writing. Please connect to V_{DD} for normal operation.	
Vss		GND pin. Connect both Vss pins to GND.	

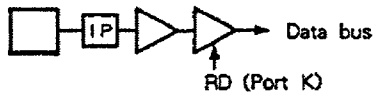
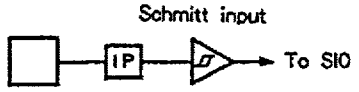
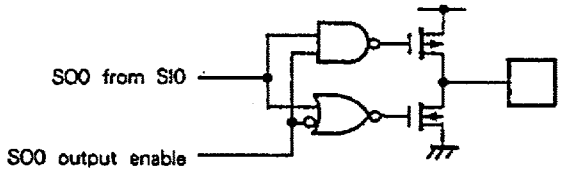
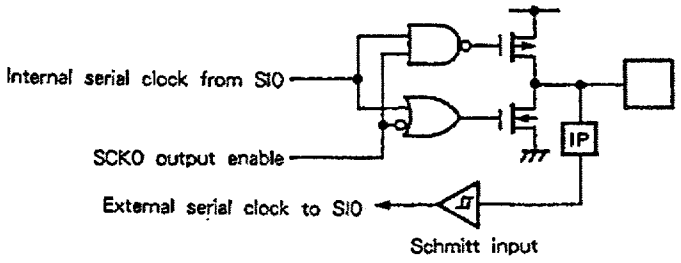
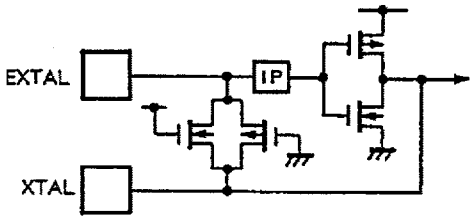
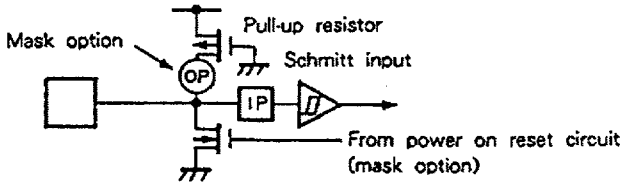
Input/Output Circuit Formats for Pins

Pin	Circuit format	When reset
PA0/PPO0 to PA7/PPO7 PB0/PPO8 to PB7/PPO15 16 pins	Port A Port B 	Hi-Z
PC0/PPO16 to PC2/PPO18 PC3/RTO3 to PC7/RTO7 8 pins	Port C 	Hi-Z
PD0 to PD7 8 pins	Port D 	Hi-Z

Pin	Circuit format	When reset
PE0/$\overline{INT0}$ PE1/EC/$\overline{INT2}$ 2 pins	Port E 	Hi-Z
PE2/PWM0 PE3/PWM1 PE4/DAA0 PE5/DAA1 4 pins	Port E 	Hi-Z
PE6/DAB0 PE7/DAB1 2 pins	Port E 	H level
AN0 to AN3 4 pins		Hi-Z
PF0/AN4 to PF3/AN7 4 pins	Port F 	Hi-Z

Pin	Circuit format	When reset
PF4/AN8 to PF7/AN11 4 pins	Port F 	Hi-Z
PG0/CFG PG1/DFG PG2/DPG PG3/PBCTL PG4/SYNC0 PG5/SYNC1 PG6/EXI0 PG7/EXI1 8 pins	Port G  Note) For PG4/SYNC0, PG5/SYNC1, CMOS schmitt input and TTL schmitt input can be selected with the mask option.	Hi-Z
PH0 to PH7 8 pins	Port H 	Hi-Z
PI0/PCK 1 pin	Port I 	Hi-Z

Pin	Circuit format	When reset
PI1/PO PI2/$\overline{PWM}$ PI3/TO 3 pins	Port I 	Hi-Z
PI4/$\overline{INT1}$ PI7/SI1 2 pins	Port I 	Hi-Z
PI5/$\overline{SCK1}$ PI6/SO1 2 pins	Port I 	Hi-Z
PJ0 to PJ7 8 pins	Port J 	Hi-Z

Pin	Circuit format	When reset
PK0 1 pin	Port K 	Hi-Z
$\overline{CS0}$ SI0 2 pins		Hi-Z
SO0 1 pin		Hi-Z
$\overline{SCK0}$ 1 pin		Hi-Z
EXTAL XTAL 2 pins	 • Shows the circuit composition during oscillation. • Feedback resistor is removed during stop.	Oscillation
$\overline{RST}$ 1 pin		L level
MP 1 pin		Hi-Z

Absolute Maximum Ratings (Vss=0V)

Item	Symbol	Ratings	Unit	Remarks
Power supply voltage	V_{DD}	−0.3 to +7.0	V	
	Vpp	−0.3 to +13.0	V	Incorporated PROM
	AV_{DD}	AVss to +7.0 *1	V	
	AVss	−0.3 to +0.3	V	
Input voltage	V_{IN}	−0.3 to +7.0 *2	V	
Output voltage	V_{OUT}	−0.3 to +7.0 *2	V	
Middle tension proof output voltage	V_{OUTP}	−0.3 to +15.0	V	PH pin
High level output current	I_{OH}	−5	mA	
High level total output current	ΣI_{OH}	−50	mA	Total of output pins
Low level output current	I_{OL}	15	mA	Other than high current output pins:per pin
	I_{OLC}	20	mA	High current port pin *3 : per pin
Low level total output current	ΣI_{OL}	130	mA	Total of output pins
Operating temperature	Topr	−10 to +75	°C	
Storage temperature	Tstg	−55 to +150	°C	
Allowable power dissipation	P_D	600	mW	QFP package
		380		VQFP package

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should better take place under the recommended operating conditions. Exceeding those conditions may adversely affect the reliability of the LSI.

*1) AV_{DD} and V_{DD} should be set to a same voltage.

*2) V_{IN} and V_{OUT} should not exceed V_{DD}+0.3V.

*3) The high current operation transistors are the N-ch transistors of the PD and PH ports.

Recommended Operating Conditions

(Vss=0V)

Item	Symbol	Min.	Max.	Unit	Remarks
Power supply voltage	V_{DD}	4.5	5.5	V	Guaranteed range during high speed mode (1/2 dividing clock) operation
		3.5	5.5	V	Guaranteed range during low speed mode (1/16 dividing clock) operation
		2.5	5.5	V	Guaranteed data hold operation range during STOP
	Vpp	Vpp=V_{DD}		V	*6
Analog power supply	AV_{DD}	4.5	5.5	V	*1
High level input voltage	V_{IH}	0.7V_{DD}	V_{DD}	V	*2
	V_{IHS}	0.8V_{DD}	V_{DD}	V	C-MOS schmitt input *3
	V_{IHTS}	2.2	V_{DD}	V	TTL schmitt input *4
	V_{IHEX}	V_{DD}–0.4	V_{DD}+0.3	V	EXTAL pin *5
Low level input voltage	V_{IL}	0	0.3V_{DD}	V	*2
	V_{ILS}	0	0.2V_{DD}	V	C-MOS schmitt input *3
	V_{ILTS}	0	0.8	V	TTL schmitt input *4
	V_{ILEX}	–0.3	0.4	V	EXTAL pin *5
Operating temperature	Topr	–10	+75	°C	

*1) AV_{DD} and V_{DD} should be set to a same voltage.
*2) Normal input port (each pin of PC, PD, PE0 to PE1, PF0 to PF3, PG, PI, PJ and PK), MP pin
*3) Each pin of $\overline{CS0}$, SI0, $\overline{SCK0}$, $\overline{RST}$, PE0/$\overline{INT0}$, PE1/$\overline{EC}$/$\overline{INT2}$, PG (For PG4 and PG5, PI4/$\overline{INT1}$, PI5/$\overline{SCK1}$ and PI7/SI1.
*4) Each pin of PG4 and PG5.
*5) It specifies only when the external clock is input.
*6) Vpp and V_{DD} should be set to a same voltage.

Electrical Characteristics

DC Characteristics

(Ta=−10 to +75°C, Vss=0V)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
High level output voltage	V_{OH}	PA to PD, PE2 to PE7, PF4, to PF7, PH (V_{OL} only), PI1 to PI7, PJ, SO, $\overline{SCK}$, $\overline{RST}$ (V_{OL} only)	V_{DD}=4.5V, I_{OH}=−0.5mA	4.0			V
			V_{DD}=4.5V, I_{OH}=−1.2mA	3.5			V
Low level output voltage	V_{OL}		V_{DD}=4.5V, I_{OL}=1.8mA			0.4	V
			V_{DD}=4.5V, I_{OL}=3.6mA			0.6	V
		PD, PH	V_{DD}=4.5V, I_{OL}=12.0mA			1.5	V
Input current	I_{IHE}	EXTAL	V_{DD}=5.5V, V_{IH}=5.5V	0.5		40	µA
	I_{ILE}		V_{DD}=5.5V, V_{IL}=0.4V	−0.5		−40	µA
	I_{ILR}	$\overline{RST}$	V_{DD}=5.5V, V_{IL}=0.4V	−1.5		−400	µA
I/O leakage current	I_{IZ}	PA to PG, PI to PK, MP, AN0 to $\overline{AN3}$, $\overline{CS0}$, SI0, SO0, $\overline{SCK0}$	V_{DD}=5.5V V_I=0, 5.5V			±10	µA
Open drain output leakage current (N-ch Tr OFF in state)	I_{LOH}	PH	V_{DD}=5.5V V_{OH}=12V			50	µA
Supply current *1	I_{DD}	V_{DD}	Crystal oscillation (C1=C2=15pF) of 12MHz		21	45	mA
	I_{DDS1}		V_{DD}=5V ± 10% *2 SLEEP mode V_{DD}=5V ± 10%		1.1	8	mA
	I_{DDS2}		STOP mode V_{DD}=5V ± 10%			30	µA
Input capacity	C_{IN}	Other than V_{DD}, Vss, AV_{DD}, AVss pins	Clock 1MHz 0V other than the measured pins		10	20	pF

*1) When entire output pins are open.

*2) When setting upper 2 bits (CPU clock selection) of clock control register CLC (address: 00FEH) to "00" and operating in high speed mode (1/2 dividing clock).

AC Characteristics

(1) Clock timing

(Ta=−10 to +75°C, V_{DD}=4.5 to 5.5V, Vss=0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
System clock frequency	fc	XTAL EXTAL	Fig. 1, Fig. 2	1	12	MHz
System clock input pulse width	t_{XL} t_{XH}	EXTAL	Fig. 1, Fig. 2 (External clock drive)	37.5		ns
System clock input rising and falling times	t_{CR} t_{CF}				200	ns
Event count clock input pulse width	t_{EL} t_{EH}	$\overline{EC}$	Fig. 3	tsys * +50		ns
Event count clock input rising and falling times	t_{ER} t_{EF}	$\overline{EC}$	Fig. 3		20	ms

* tsys indicates three values according to the contents of the clock control register (address; 00FEH) upper 2 bits (CPU clock selection).
tsys [ns] =2000/fc (Upper 2-bit="00"), 4000/fc (Upper 2-bit="01"), 16000/fc (Upper 2-bit="11")

Fig. 1. Clock timing

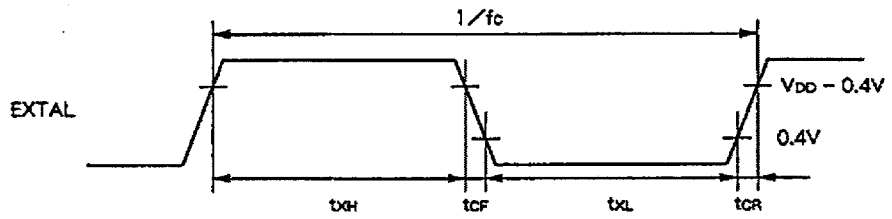


Fig. 2. Clock applying condition

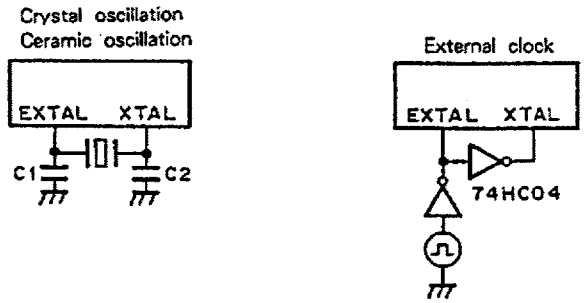
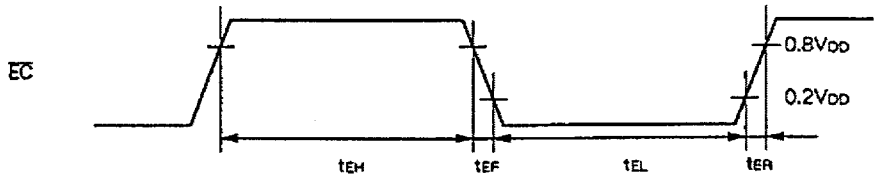


Fig. 3. Event count clock timing



(2) Serial transfer (CH0)

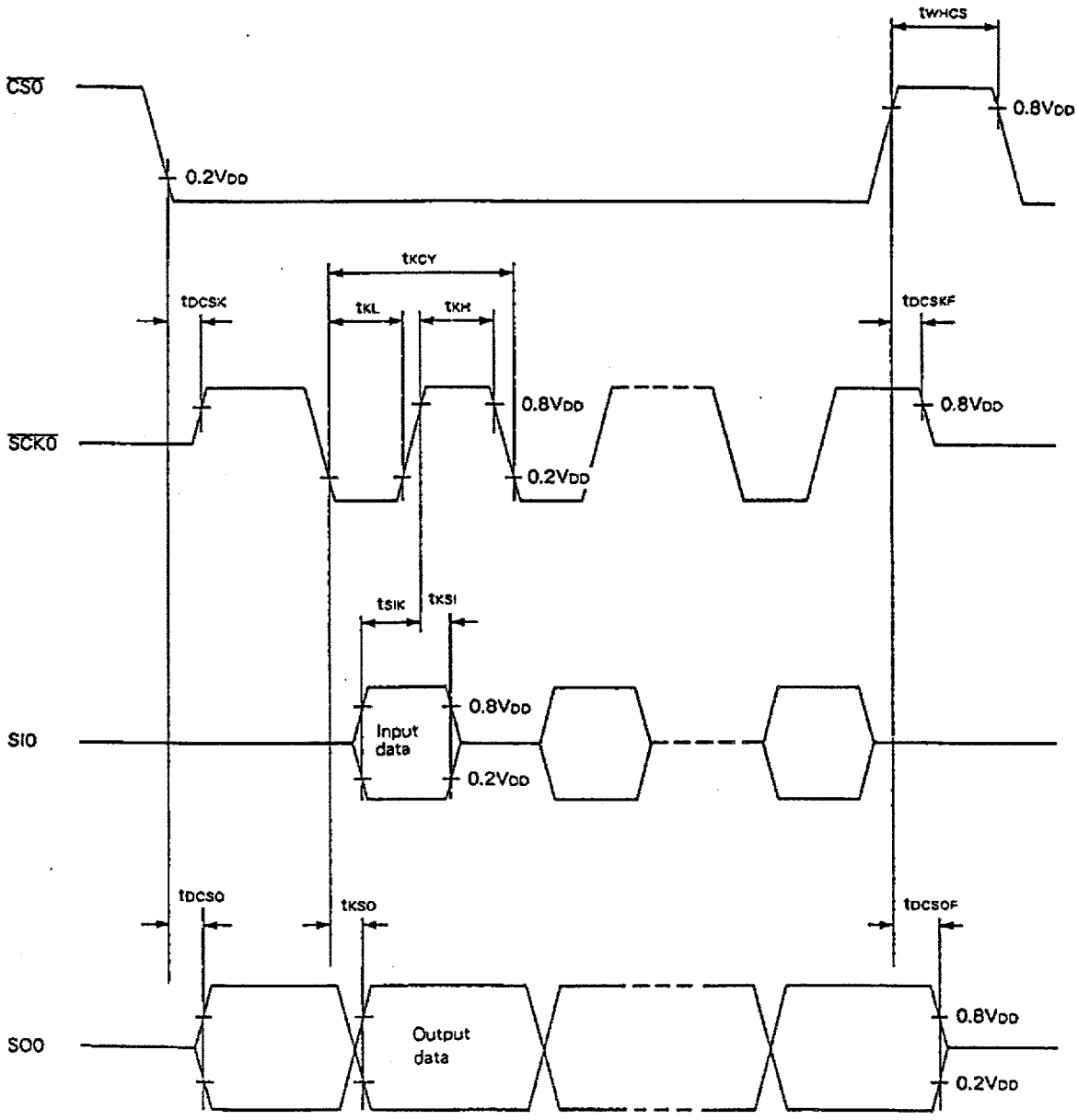
(Ta=−10 to +75°C, V_{DD}=4.5 to 5.5V, V_{SS}=0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{CS0}$ ↓ → $\overline{SCK0}$ delay time	t_{DCSK}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK0}$=output mode)		tsys+200	ns
$\overline{CS0}$ ↑ → $\overline{SCK0}$ floating delay time	t_{DCSKF}	$\overline{SCK0}$			tsys+200	ns
$\overline{CS0}$ ↓ → SO0 delay time	t_{DCSO}	SO0	Chip select transfer mode		tsys+200	ns
$\overline{CS0}$ ↑ → SO0 floating delay time	t_{DCSOF}	SO0			tsys+200	ns
$\overline{CS0}$ high level width	t_{WHCS}	$\overline{CS0}$		tsys+200		ns
$\overline{SCK0}$ cycle time	t_{KCY}	$\overline{SCK0}$	Input mode	2tsys+200		ns
			Output mode	16000/fc		ns
$\overline{SCK0}$ high and low level widths	t_{KH} t_{KL}	$\overline{SCK0}$	Input mode	tsys+100		ns
			Output mode	8000/fc−50		ns
SI0 input setup time (against $\overline{SCK0}$ ↑)	t_{SIK}	SI0	$\overline{SCK0}$ input mode	100		ns
			$\overline{SCK0}$ output mode	200		ns
SI0 input hold time (against $\overline{SCK0}$ ↑)	t_{KSI}	SI0	$\overline{SCK0}$ input mode	tsys+200		ns
			$\overline{SCK0}$ output mode	100		ns
$\overline{SCK0}$ ↓ → SO0 delay time	t_{KSO}	SO0	$\overline{SCK0}$ input mode		tsys+200	ns
			$\overline{SCK0}$ output mode		100	ns

Note 1) tsys indicates three values according to the contents of the clock control register (address; 00FE$_H$) upper 2 bits (CPU clock selection).
tsys [ns] =2000/fc (Upper 2-bit="00"), 4000/fc (Upper 2-bit="01"), 16000/fc (Upper 2-bit="11")

2) The Load of $\overline{SCK0}$ output mode and SO0 output delay time is 50pF+1TTL.

Fig. 4. Serial transfer CH0 timing

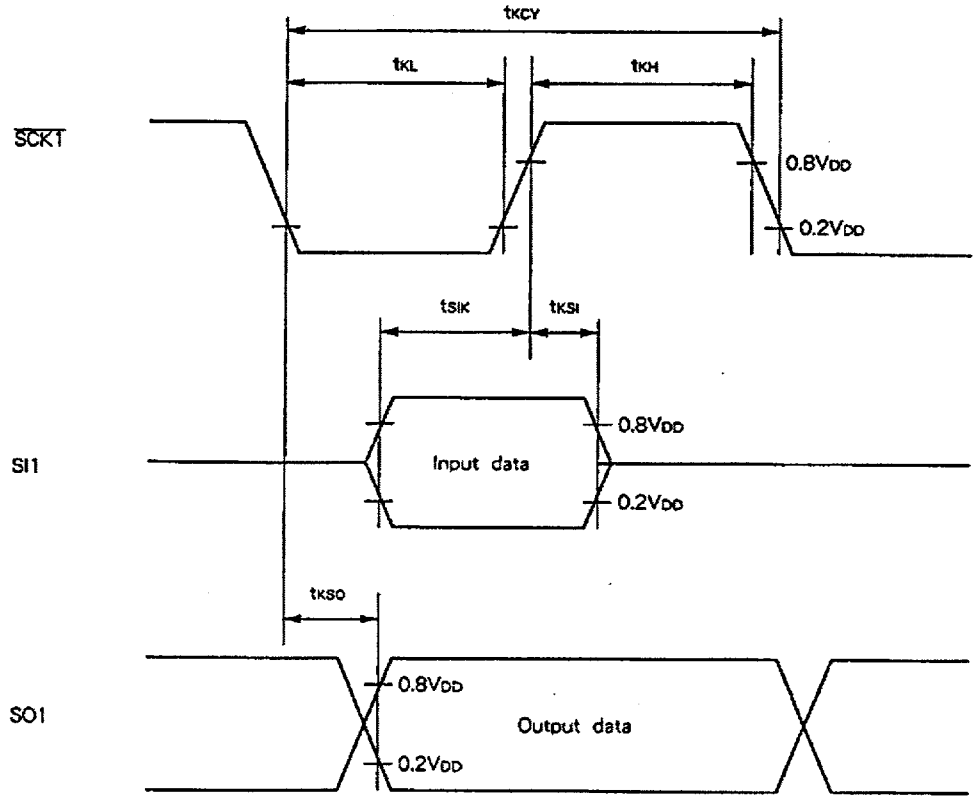


Serial transfer (CH1) (SIO mode) (Ta=−10 to +75°C, V_{DD}=4.5 to 5.5V, Vss=0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{SCK1}$ cycle time	t_{KCY}	$\overline{SCK1}$	Input mode	2tsys+200		ns
			Output mode	16000/fc		ns
$\overline{SCK1}$ high and low level widths	t_{KH} t_{KL}	$\overline{SCK1}$	Input mode	tsys+100		ns
			Output mode	8000/fc−50		ns
SI1 input setup time (against $\overline{SCK1}$ ↑)	t_{SIK}	SI1	$\overline{SCK1}$ input mode	100		ns
			$\overline{SCK1}$ output mode	200		ns
SI1 input hold time (against $\overline{SCK1}$ ↑)	t_{KSI}	SI1	$\overline{SCK1}$ input mode	tsys+200		ns
			$\overline{SCK1}$ output mode	100		ns
$\overline{SCK1}$ ↓ → SO1 delay time	t_{KSO}	SO1	$\overline{SCK1}$ input mode		tsys+200	ns
			$\overline{SCK1}$ output mode		100	ns

Note 1) tsys indicates three values according to the contents of the clock control register (address; 00FE$_H$) upper 2 bits (CPU clock selection).
tsys [ns] =2000 /fc (Upper 2-bit="00"), 4000/fc (Upper 2-bit="01"), 16000/fc (Upper 2-bit="11").
2) The Load of $\overline{SCK1}$ output mode and SO1 output delay time is 50pF +1TTL.

Fig. 5. Serial transfer CH1 timing (SIO mode)



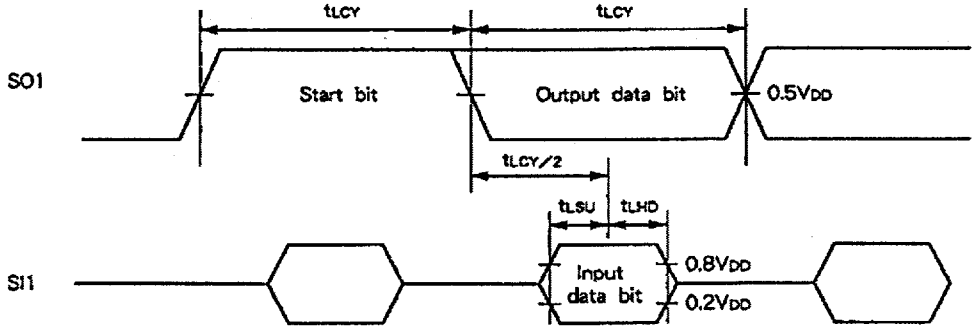
Serial transfer (CH1) (Special mode) (Ta=−10 to +75°C, V_{DD}=4.5 to 5.5V, Vss=0V)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
SO1 cycle time	t_{LCY}	SO1 SI1	Note 1)		104		µs
SI1 data setup time	t_{LSU}	SI1		2			µs
SI1 data hold time	t_{LHD}	SI1		2			µs

Note 1) t_{LCY} specifies only serial mode register (CH1) (SIOM1: Address 01FA$_H$) lower 2 bits (SO1 clock selection) has been set at 104 µs.

2) The load of SO1 pin is 50pF +1TTL.

Fig. 6. Serial transfer CH1 timing (Special mode)

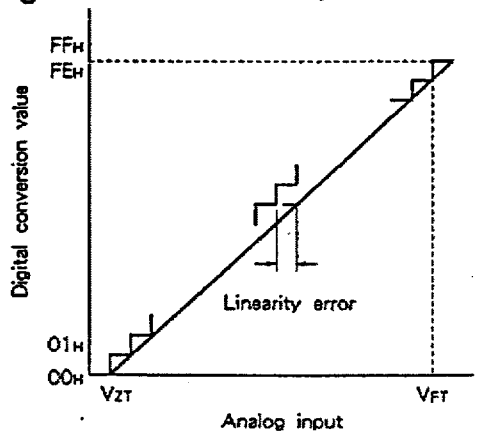


(3) A/D converter characteristics

(Ta=−10 to +75°C, V_{DD}=AV_{DD}=4.5 to 5.5V, AV_{REF}=4.0V to AV_{DD}, V_{SS}=AV_{SS}=0V)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			Ta=25°C V_{DD}=AV_{DD}=5.0V V_{SS}=AV_{SS}=0V			±1	LSB
Zero transition voltage	V_{ZT} *1			−10	30	70	mV
Full scale transition voltage	V_{FT} *2			4930	4970	5010	mV
Conversion time	t_{CONV}			160/f_{ADC} *3			µs
Sampling time	t_{SAMP}			12/f_{ADC} *3			µs
Reference input voltage	V_{REF}	AV_{REF}		AV_{DD}−0.5		AV_{DD}	V
Analog input voltage	V_{IAN}	AN0 to AN11		0		AV_{REF}	V
AV_{REF} current	I_{REF}	AV_{REF}	Operating mode		0.6	1.0	mA
	I_{REFS}		SLEEP mode STOP mode			10	µA

Fig. 7. Definitions of A/D converter terms



*1) V_{ZT}: Indicates the value that digital conversion value changes from 00H to 01H and vice versa.

*2) V_{FT}: Indicates the value that digital conversion value changes from FEH to FFH and vice versa.

*3) The value of f_{ADC} is as follows by selecting ADC operation clock (MSC: Address 01FFH bit 0).

When PS2 is selected, f_{ADC}=fc/2

When PS1 is selected, f_{ADC}=fc

(4) Interruption, reset input

(Ta=−10 to +75°C, V_{DD}=4.5 to 5.5V, Vss=0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
External interruption high and low level widths	t_{IH}, t_{IL}	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$ PJ0 to PJ7		1		µs
Reset input low level width	t_{RSL}	$\overline{RST}$		8/fc		µs

Fig. 8. Interruption input timing

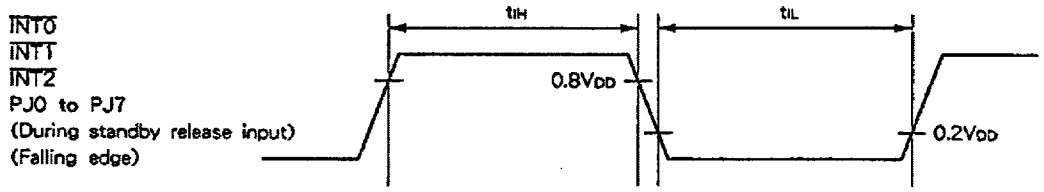
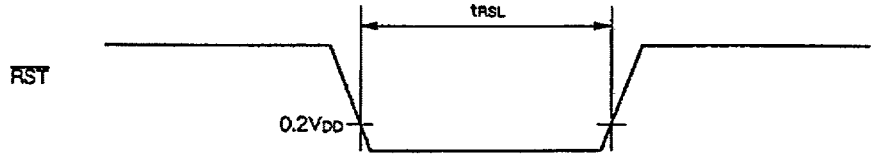


Fig. 9. Reset input timing



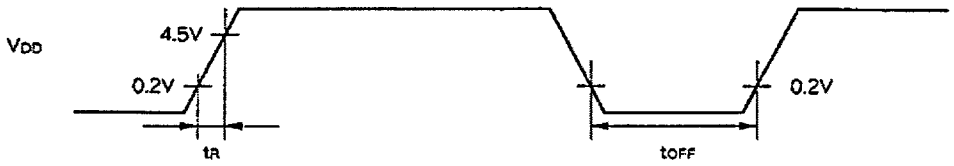
(5) Power on reset

Power on reset

(Ta=−10 to +75°C, V_{DD}=4.5 to 5.5V, Vss=0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
Power supply rising time	t_R	V_{DD}	Power on reset	0.05	50	ms
Power supply cut-off time	t_{OFF}		Repetitive power on reset	1		ms

Fig. 10. Power on reset



The power supply should rise smoothly.

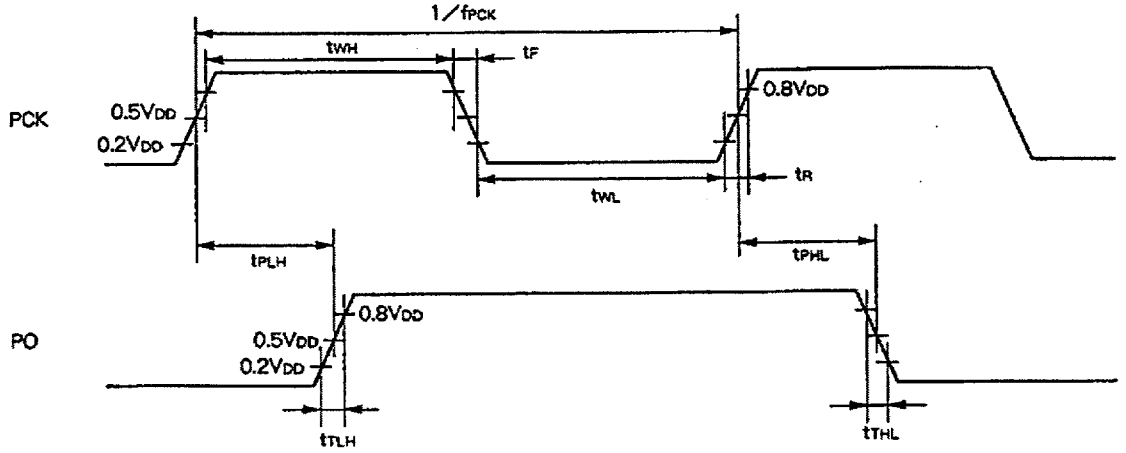
(6) General purpose prescaler

(Ta=–10 to +75°C, V_{DD}=4.5 to 5.5V, Vss=0V)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
External clock input frequency	f_{PCK}	PCK				12	MHz
External clock input pulse width	t_{WH}, t_{WL}	PCK		33			ns
External clock input rising and falling times	t_R, t_F	PCK				200	ns
Prescaler output delay time (against PCK ↑)	t_{PLH}	PO	External clock input PCK t_R=t_F=6ns		80	130	ns
	t_{PHL}				60	100	ns
Prescaler output rising and falling times	t_{TLH}	PO	External clock input PCK t_R=t_F=6ns		50	100	ns
	t_{THL}				20	40	ns

Note) The load of PO pin is 50pF.

Fig. 11. General purpose prescaler timing



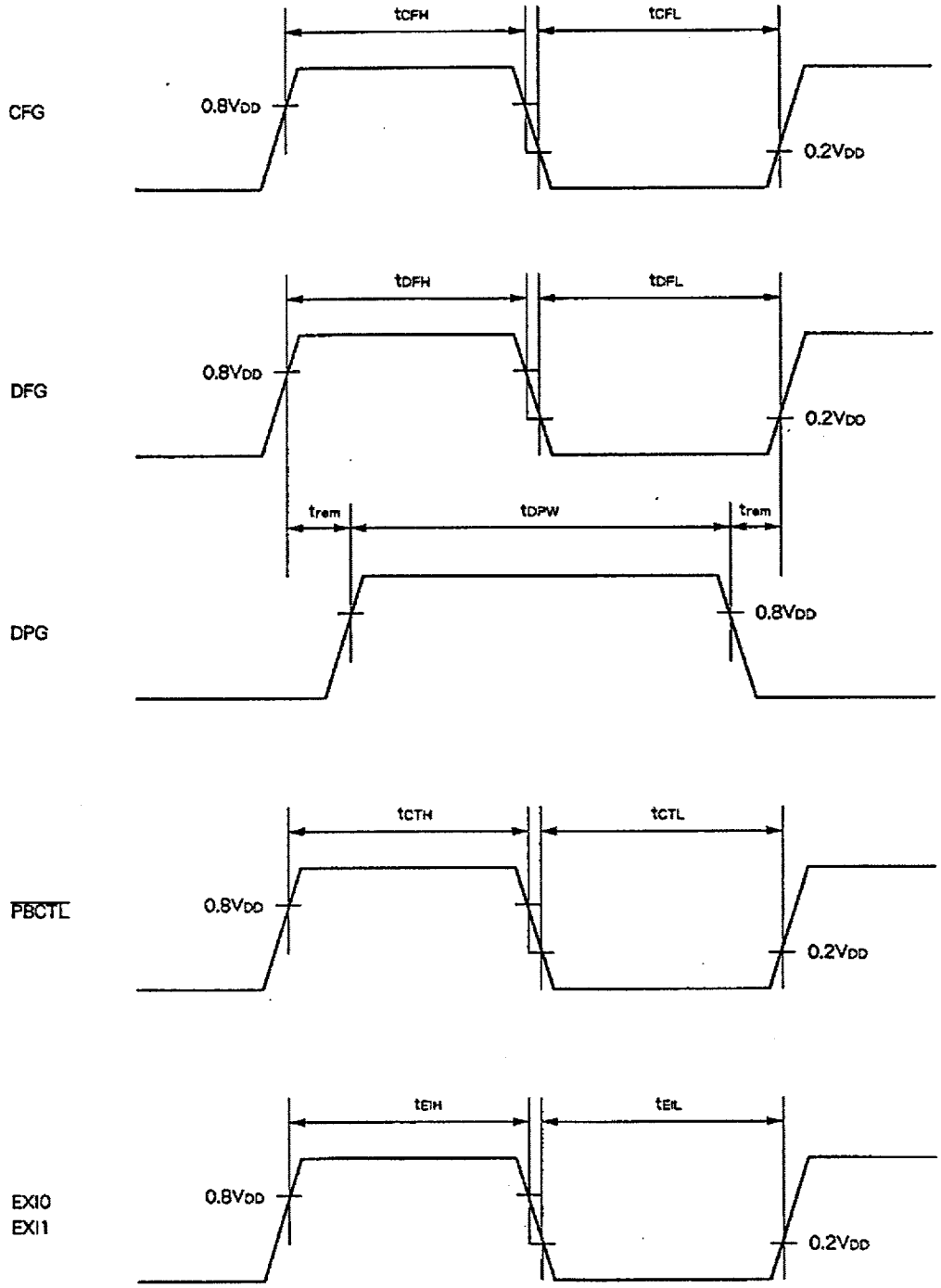
(7) Others

(Ta=–10 to +75°C, V_{DD}=4.5 to 5.5V, Vss=0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
CFG input high and low level widths	t_{CFH}, t_{CFL}	CFG		tsys+200		ns
DFG input high and low level widths	t_{DFH}, t_{DFL}	DFG		1000/fc+200		ns
DPG minimum pulse width	t_{DPW}	DPG		50		ns
DPG minimum removal time	trem	DPG		50		ns
$\overline{\text{PBCTL}}$ input high and low level widths	t_{CTH}, t_{CTL}	$\overline{\text{PBCTL}}$	tsys=2000/fc	tsys+200		ns
EXI input high and low level widths	t_{EIH}, t_{EIL}	EXI0 EXI1	tsys=2000/fc	tsys+200		ns

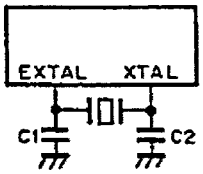
Note) tsys indicates three values according to the contents of the clock control register (address; 00FE$_H$) upper 2 bits (CPU clock selection).
tsys [ns] =2000/fc (Upper 2-bit="00"), 4000/fc (Upper 2-bit="01"), 16000/fc (Upper 2-bit="11")

Fig. 12. Other timings



Supplement

Fig. 13. Recommended oscillation circuit



Manufacturer	Model	Frequency f (MHz)	C_1, C_2 (pF)
MURATA MFG CO., LTD.	CSA12.0MTZ0C3	12	30

Manufacturer	Model	Frequency f (MHz)	C_1, C_2 (pF)
RIVER ELETEC CO., LTD.	HC-49/U03	12	12
KINSEKI LTD.	HC-49/U	12	15
CITIZEN WATCH CO., LTD.	CSA-309	12	10

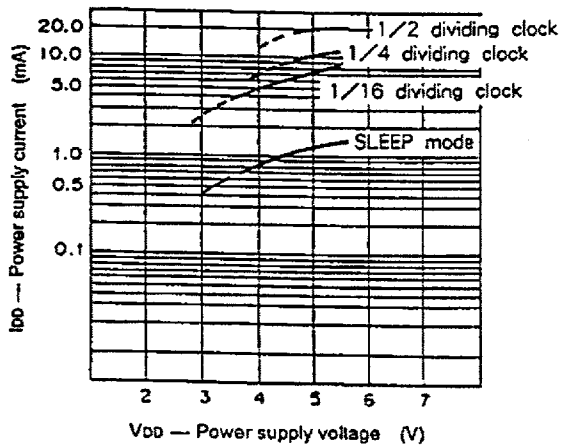
Selection Guide

Option item	Mask product	CXP80P624AQ-1-□□□	CXP80P624AR-1-□□□
Package	100-pin plastic QFP/VQFP	100-pin plastic QFP	100-pin plastic VQFP
ROM capacitance	20K bytes/24K bytes	PROM 24K bytes	PROM 24K bytes
Reset pin pull-up resistor	Existent/non-existent	Existent	Existent
Power on reset circuit	Existent/non-existent	Existent	Existent
Input circuit format *	CMOS Schmitt/TTL Schmitt	TTL Schmitt	TTL Schmitt

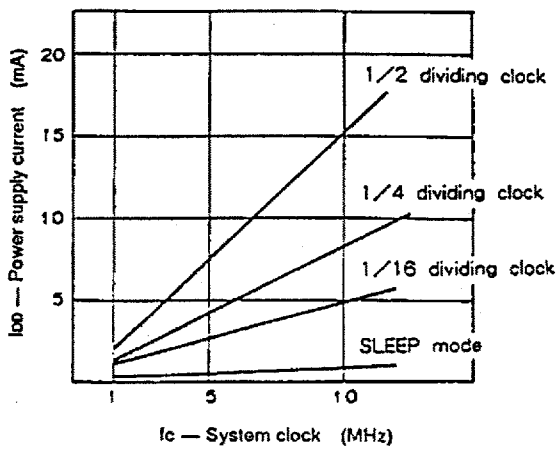
* Pins PG4/SYNC0, PG5/SYNC1 only.

Characteristics Curve

I_{DD} vs. V_{DD}
(fc=12MHz, Ta=25°C, Typical)



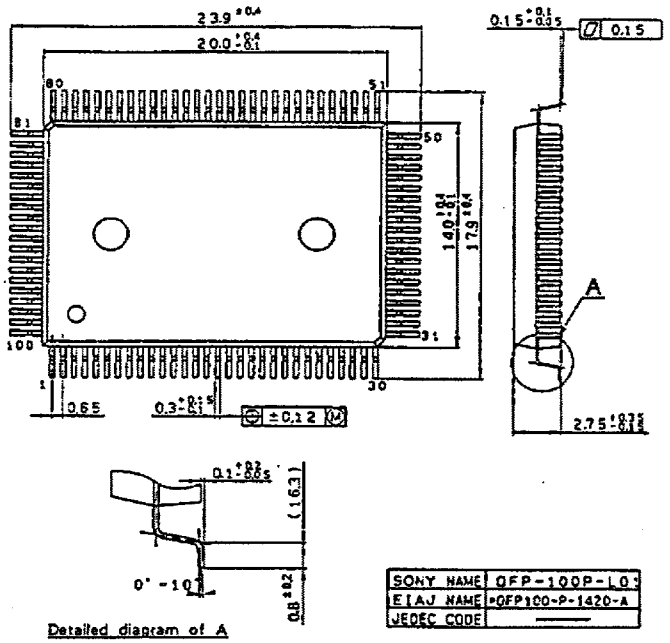
I_{DD} vs. fc
(V_{DD}=5V, Ta=25°C, Typical)



Package Outline

Unit : mm

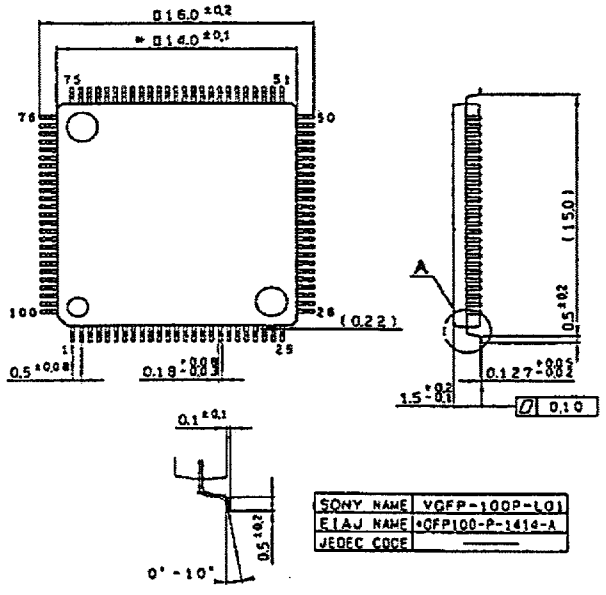
100pin QFP (Plastic) 1.7g



Detailed diagram of A

SONY NAME	QFP-100P-L01
EIAJ NAME	*QFP100-P-1420-A
JEDEC CODE	

100pin VQFP (Plastic)



SONY NAME	VQFP-100P-L01
EIAJ NAME	*QFP100-P-1414-A
JEDEC CODE	

Detailed diagram of A

Note) Dimensions marked with * does not include resin residue.