



E COMPUTER
E CONVERSIONS
E CORPORATION

6 Dunton Court, East Northport, NY 11731 • (516) 261-3300

LVT SERIES

DIGITAL TO LVDT CONVERTERS

DESCRIPTION

The LVT Series are low profile, continuously updating, single and dual channel digital to LVDT converters used to simulate the output of LVDT and RVDT related devices.

Industrial and Military applications include; vehicular training equipment, ship and flight simulators, ATE (automatic test equipment), and varied instrumentation comparison and diagnostic uses.

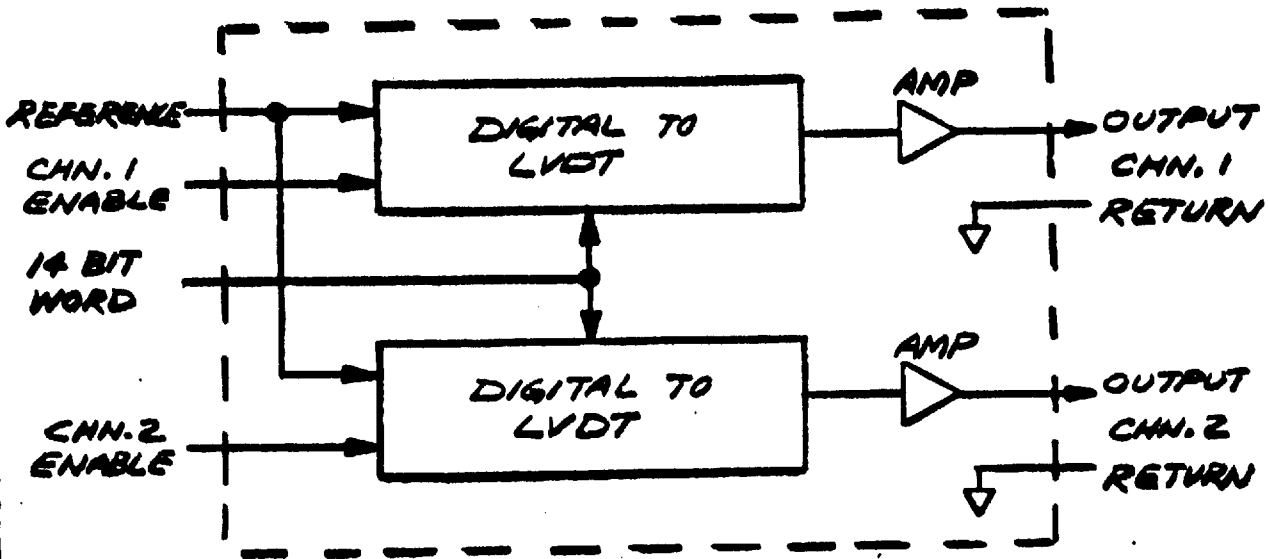
These 2.6 x 3.1 x .4"H modules will accept 14 bits of binary data offered with offset binary or two's complement type formats and convert it into polarized AC data corresponding to the output typical of an LVDT.

Two channel versions feature a common 14 bit binary data input buss with discreet data enable inputs and LVDT outputs for each channel. Data enables are active low (200 nsec. min.) to latch the command input data, and both channels may latched simultaneously with the same input data if and when desired.

REFERENCE INPUT.....7 VOLTS, 3KHZ
 OUTPUT.....0-7V RMS, 3KHZ
 OUTPUT LOAD.....2K MIN.
 D.C. SUPPLY REQ'D.....+5V
 (REGULATED) +15V
 -15V
 GND
 RESOLUTION.....14 BITS
 ACCURACY.....+.1% @ F.S. STD.
 HIGHER ACCURACY OPT.

DIGITAL INPUT CODES

SCALE	DLVDT314-7-1 OFFSET BINARY	DLVDT314A-7-1 TWO'S COMPLEMENT
+FS - 1 LSB	1111 1111 1111	0111 1111 1111
+3/4 FS	1110 0000 0000	0110 0000 0000
+1/2 FS	1100 0000 0000	0100 0000 0000
+1/4 FS	1010 0000 0000	0010 0000 0000
0	1000 0000 0000	0000 0000 0000
-1/4 FS	0110 0000 0000	1110 0000 0000
-1/2 FS	0100 0000 0000	1100 0000 0000
-3/4 FS	0010 0000 0000	1010 0000 0000
-FS +1 LSB	0000 0000 0001	1000 0000 0001
-FS	0000 0000 0000	1000 0000 0000



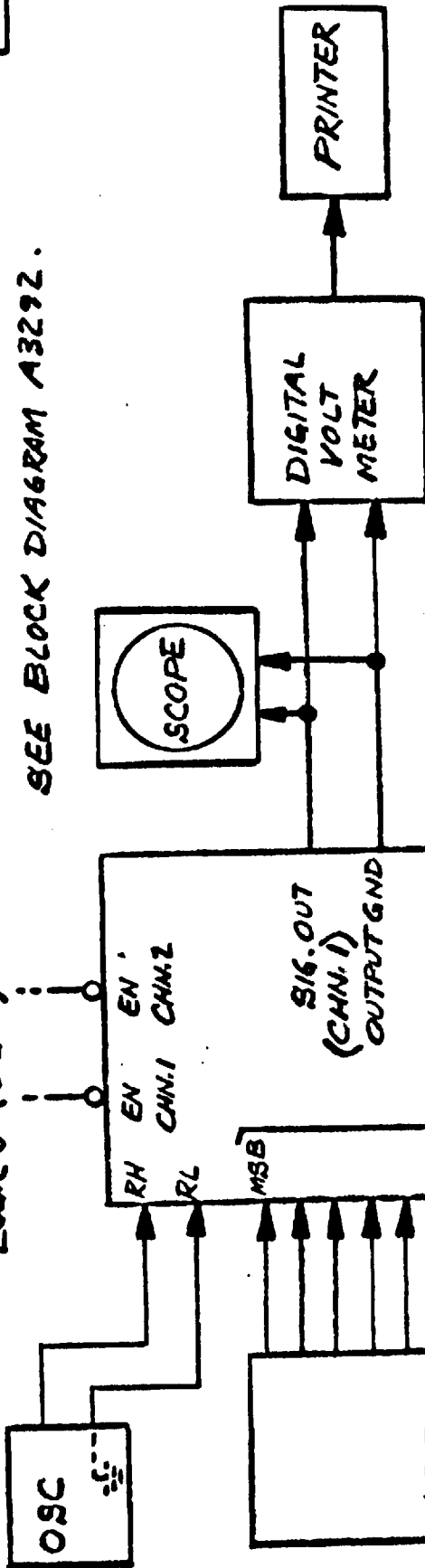
NOTE:

ENABLE INPUTS ARE ACTIVE LOW.

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SCALE: <i>H</i>	APPROVED BY:	DRAWN BY: <i>D. K. ...</i>
DATE: <i>12-18-84</i>		REVISED:
2 CHANNEL LVDT SIMULATOR MODULE		
BLOCK DIAGRAM		DRAWING NUMBER A3292

REV-

LOGIC 0" (D GND) = DAC REGISTER LOAD
SEE BLOCK DIAGRAM A3292.



(SAME AS CHN. 1)

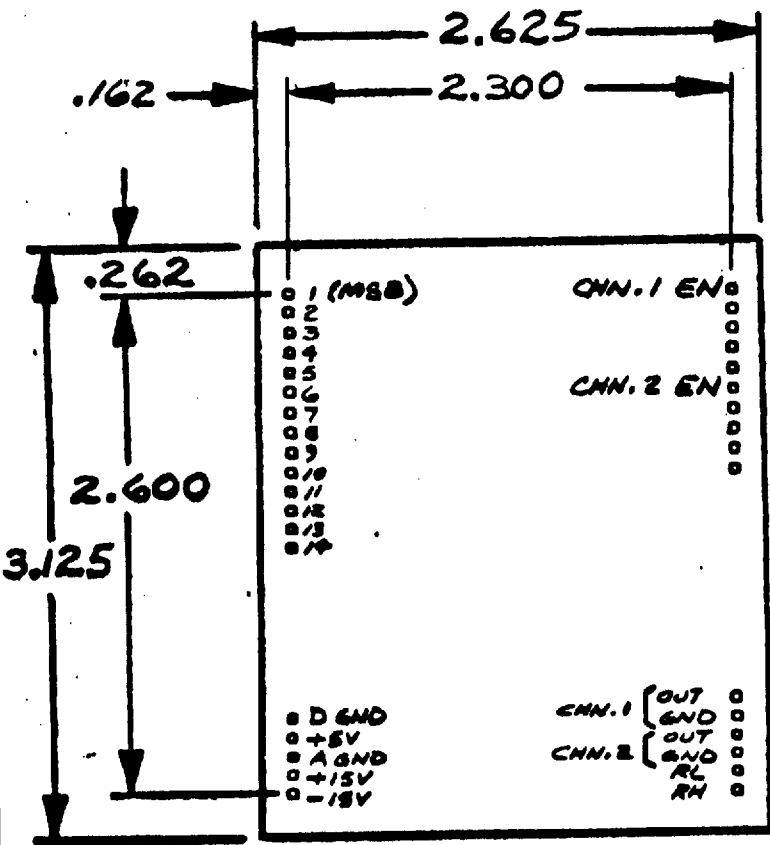
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 8 DUNTON COURT - EAST NORTHPORT, N.Y. 11731 - 616 261-3300

SCALE: *AK* APPROVED BY: *D. K. ...*
 DATE: 3-4-85 REVISION:

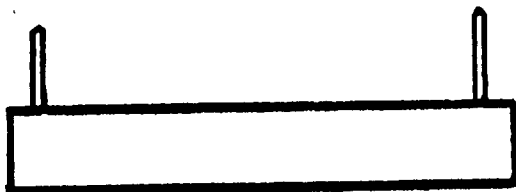
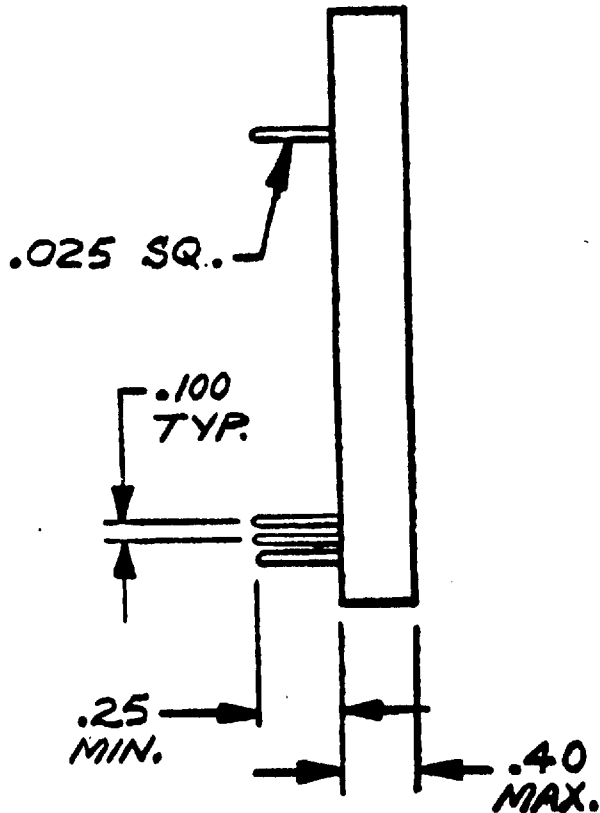
2 CHANNEL LVDT SIMULATOR MODULE

TEST CIRCUIT **A3292-1**

REV-



NOTE: UN-MARKED PINS HAVE NO INTERNAL CONNECTIONS & ARE USED FOR SOLDER SUPPORT.



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SCALE: FULL	APPROVED BY:	DRAWN BY: D. VARRONE
DATE: 12-17-84		REVISED:

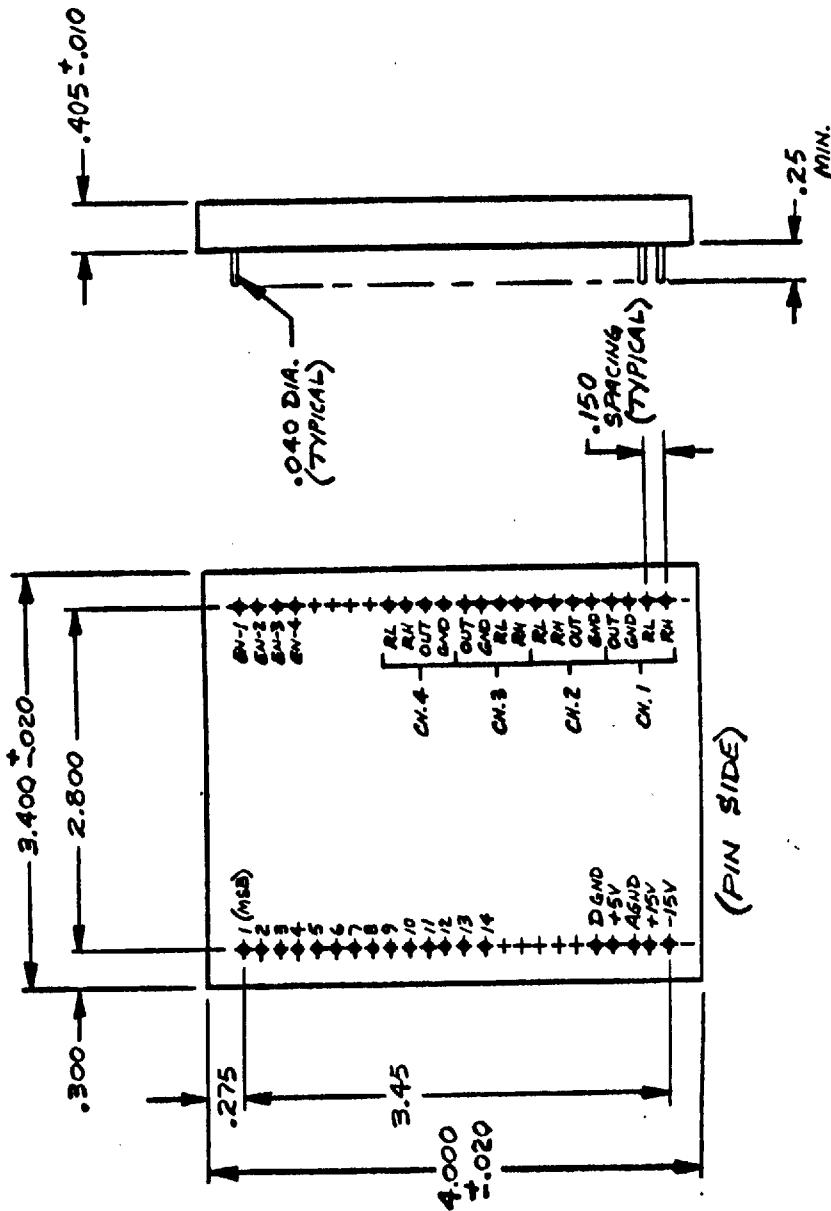
2 CHANNEL LVDT SIMULATOR MODULE

MODULE OUTLINE	DRAWING NUMBER A3290-1
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REVISIONS

DATE	DESCRIPTION	REV
7-13-89	ORIGINAL RELEASE	-
8-9-89	REVERSED CHN. 4 RH WITH RL	A



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SCALE: FULL	APPROVED BY: <i>[Signature]</i>
DATE: 7-12-89	REVISED
4 CHN. 4 BIT DIGITAL TO LVDT CONVERTER	
GLVDT-3/4-7-1L" 6" GLVDT-3/4A-7-1L"	
DRAWING NUMBER	
MECHANICAL OUTLINE	
B4718	

REFERENCE INPUT.....7 VOLTS, 3KHZ

OUTPUT.....0-7V RMS, 3KHZ

OUTPUT LOAD.....2K MIN.

D.C. SUPPLY REQ'D.....+5V @ 12 ma MAX (8 ma TYP)
(REGULATED) +15V @ 50 ma MAX (32ma TYP)
-15V @ 50 ma MAX (32ma TYP)
GND

RESOLUTION.....14 BITS

ACCURACY.....+.1% @ F.S. STD.
HIGHER ACCURACY OPT.

DIGITAL INPUT CODES

SCALE	QLVDT314-7-1L OFFSET BINARY		QLVDT314A-7-1L TWO'S COMPLEMENT	
	MSB	LSB	MSB	LSB
+FS - 1 LSB	11111111111111		01111111111111	
+3/4 FS	11100000000000		01100000000000	
+1/2 FS	11000000000000		01000000000000	
+1/4 FS	10100000000000		00100000000000	
0	10000000000000		00000000000000	
-1/4 FS	01100000000000		11100000000000	
-1/2 FS	01000000000000		11000000000000	
-3/4 FS	00100000000000		10100000000000	
-FS +1 LSB	00000000000001		10000000000001	
-FS	00000000000000		10000000000000	

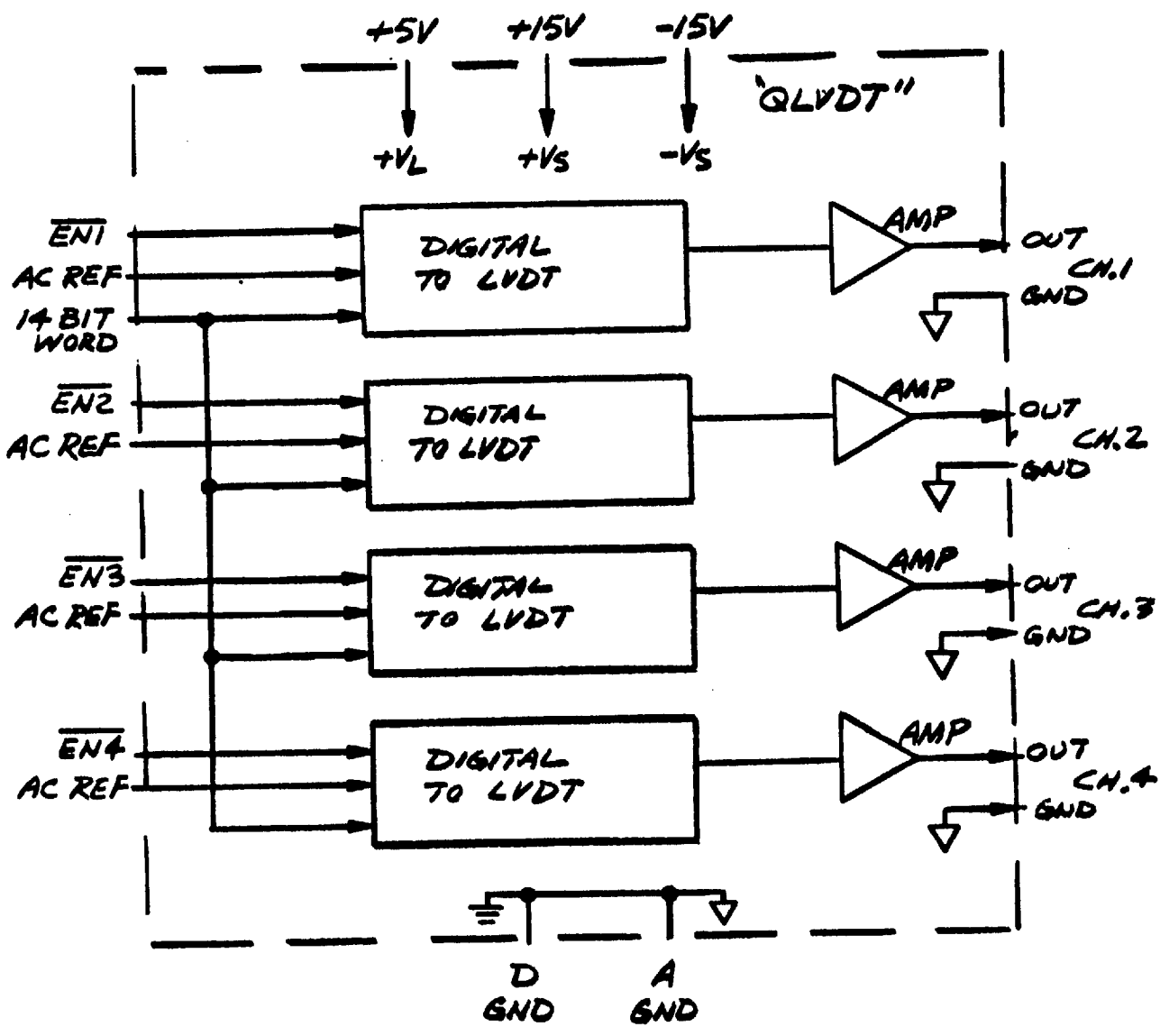
CHANNEL ENABLE..... LOGIC "0" = INPUT DATA LOAD
(TTL COMPATIBLE LOGIC)

MECHANICAL..... 3.40" x 4.00" x .40"
SEE DG B4718

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SCALE: <i>1X</i>	APPROVED BY:	DRAWN BY: <i>D. Williams</i>
DATE: 4-21-89		REVISED
4 CHANNEL LVDT SIMULAOR MODULE QLVDT314-7-1L & QLVDT314A-7-1L		
SPECIFICATIONS		DRAWING NUMBER A4719

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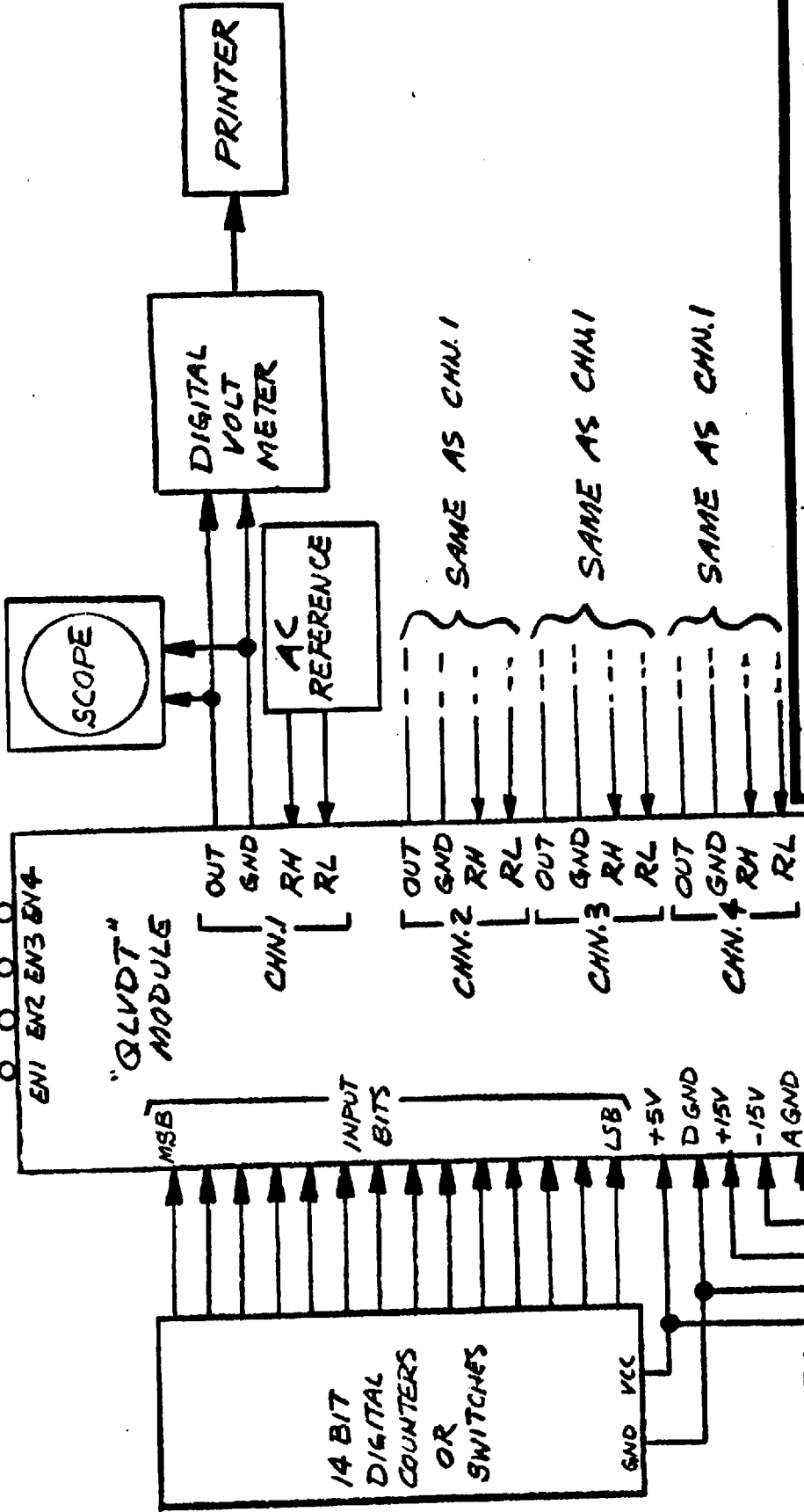
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SCALE <i>CA</i>	APPROVED BY:	DRAWN BY <i>WARRING</i>
DATE 4-21-89		REVISED
4 CHANNEL LVDT SIMULATOR MODULE "QLVDT 314-7-1L" & "QLVDT 314A-7-1L"		
BLOCK DIAGRAM		DRAWING NUMBER A4720

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REV-

LOGIC 0" (DGND) = DAC REGISTER LOAD
SEE BLOCK DIAGRAM A4434.



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SCALE: *XL* APPROVED BY: *[Signature]* DRAWN BY: *[Signature]* REVISED

DATE: 4-21-89

4 CHANNEL LVDLT SIMULATOR MODULE
"QLVDT314-7-1L" & "QLVDT344-7-1L"

DRAWING NUMBER: A4721

TEST CIRCUIT