

# BUK9Y40-55B

N-channel TrenchMOS™ logic level FET

Rev. 01 — 28 May 2004

Product data

## 1. Product profile

### 1.1 Description

N-channel enhancement mode field-effect power transistor in a plastic package using Philips High-Performance Automotive (HPA) TrenchMOS™ technology.

### 1.2 Features

- Very low on-state resistance
- 175 °C rated
- Q101 compliant
- Logic level compatible.

### 1.3 Applications

- Automotive systems
- Motors, lamps and solenoids
- 12 V and 24 V loads
- General purpose power switching.

### 1.4 Quick reference data

- $E_{DS(AL)S} \leq 48$  mJ
- $I_D \leq 20$  A
- $R_{DSon} = 34$  mΩ (typ)
- $P_{tot} \leq 50$  W.

## 2. Pinning information

Table 1: Pinning - SOT669 (LFPAK) simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1,2,3	source (s)	<p>Top view MBL286</p> <p><b>SOT669 (LFPAK)</b></p>	
4	gate (g)		
mb	mounting base, connected to drain (d)		



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### 3. Ordering information

**Table 2: Ordering information**

Type number	Package		Version
	Name	Description	
BUK9Y40-55B	LFPAK	Plastic single-ended surface mounted package (Philips version LFPAK); 4 leads	SOT669

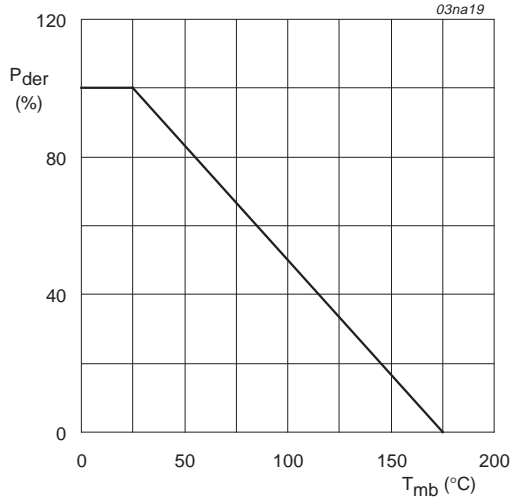
### 4. Limiting values

**Table 3: Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

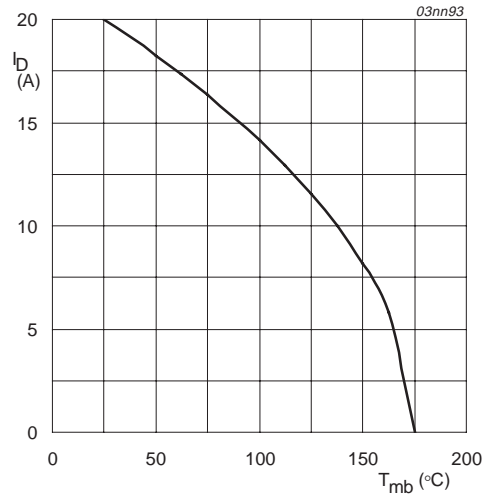
Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage (DC)		-	55	V
$V_{DGR}$	drain-gate voltage (DC)	$R_{GS} = 20 \text{ k}\Omega$	-	55	V
$V_{GS}$	gate-source voltage (DC)		-	$\pm 15$	V
$I_D$	drain current (DC)	$T_{mb} = 25 \text{ }^\circ\text{C}$ ; $V_{GS} = 5 \text{ V}$ ; Figure 2 and 3	-	20	A
		$T_{mb} = 100 \text{ }^\circ\text{C}$ ; $V_{GS} = 5 \text{ V}$ ; Figure 2	-	14	A
$I_{DM}$	peak drain current	$T_{mb} = 25 \text{ }^\circ\text{C}$ ; pulsed; $t_p \leq 10 \text{ }\mu\text{s}$ ; Figure 3	-	80	A
$P_{tot}$	total power dissipation	$T_{mb} = 25 \text{ }^\circ\text{C}$ ; Figure 1	-	50	W
$T_{stg}$	storage temperature		-55	+175	$^\circ\text{C}$
$T_j$	junction temperature		-55	+175	$^\circ\text{C}$
<b>Source-drain diode</b>					
$I_{DR}$	reverse drain current (DC)	$T_{mb} = 25 \text{ }^\circ\text{C}$	-	20	A
$I_{DRM}$	peak reverse drain current	$T_{mb} = 25 \text{ }^\circ\text{C}$ ; pulsed; $t_p \leq 10 \text{ }\mu\text{s}$	-	80	A
<b>Avalanche ruggedness</b>					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; $I_D = 20 \text{ A}$ ; $V_{DS} \leq 55 \text{ V}$ ; $V_{GS} = 5 \text{ V}$ ; $R_{GS} = 50 \text{ }\Omega$ ; starting $T_{mb} = 25 \text{ }^\circ\text{C}$	-	48	mJ
$E_{DS(AL)R}$	repetitive drain-source avalanche energy		-	[1]	-

- [1] Maximum value not quoted. Repetitive rating defined in Figure 16.  
 Single-shot avalanche rating limited by  $T_{j(max)}$  of 175  $^\circ\text{C}$ .  
 Repetitive avalanche rating limited by  $T_{j(avg)}$  of 170  $^\circ\text{C}$ .  
 Refer to [http://www.semiconductors.philips.com/acrobat/applicationnotes/AN10273\\_1.pdf](http://www.semiconductors.philips.com/acrobat/applicationnotes/AN10273_1.pdf) for further information.



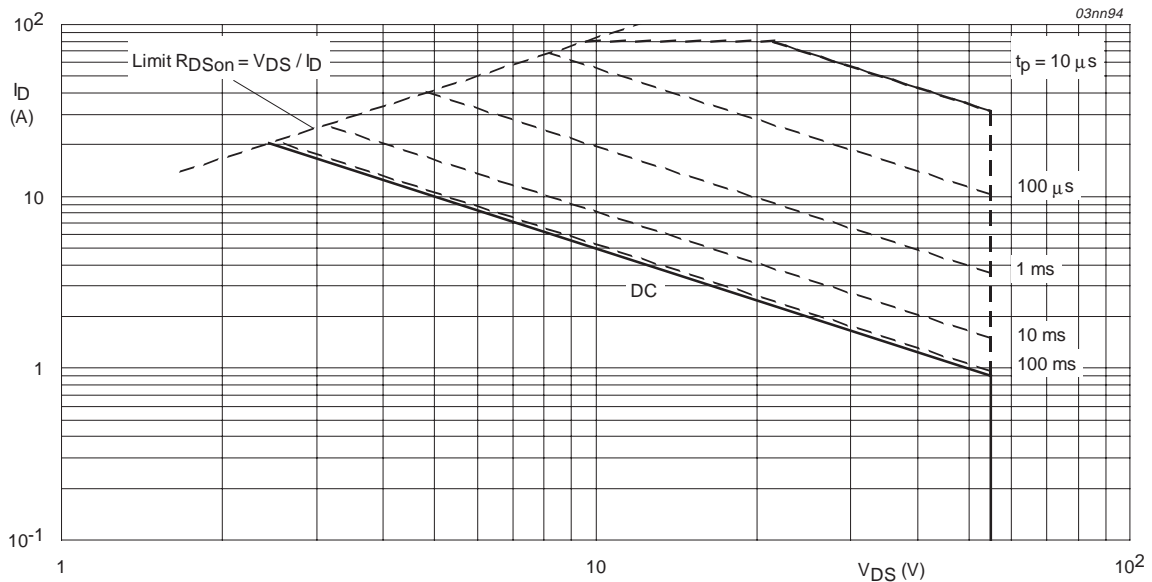
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

**Fig 1. Normalized total power dissipation as a function of mounting base temperature.**



$V_{GS} \geq 5\text{ V}$

**Fig 2. Continuous drain current as a function of mounting base temperature.**



$T_{mb} = 25^{\circ}C$ ;  $I_{DM}$  single pulse.

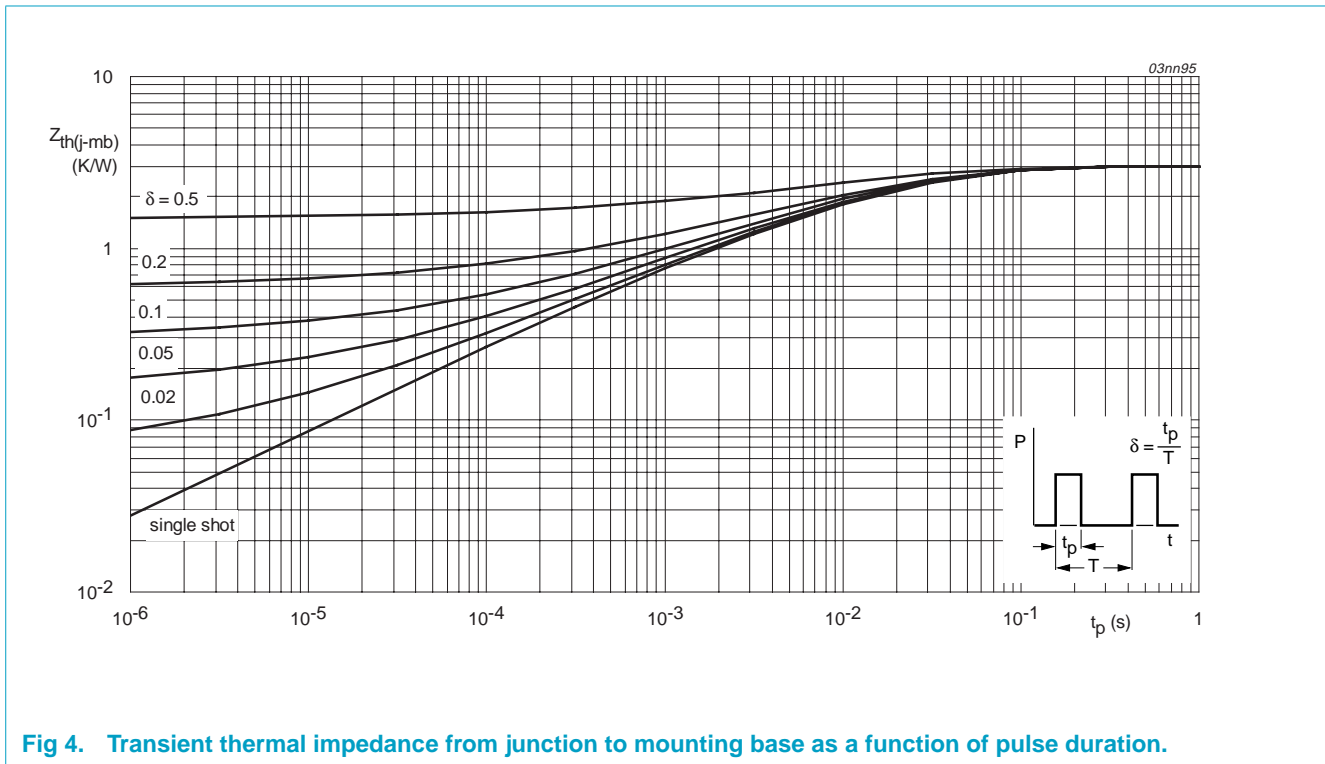
**Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.**

**5. Thermal characteristics**

**Table 4: Thermal characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Figure 4	-	-	3	K/W

**5.1 Transient thermal impedance**

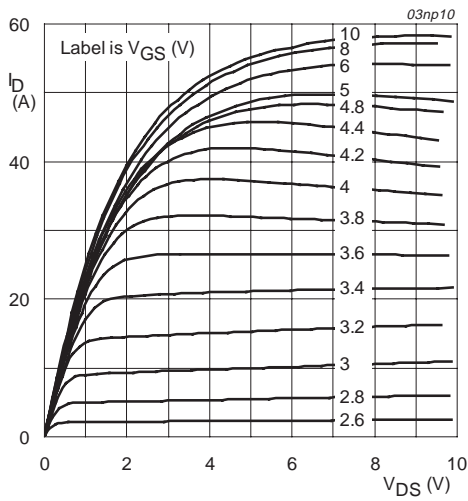


**Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration.**

## 6. Characteristics

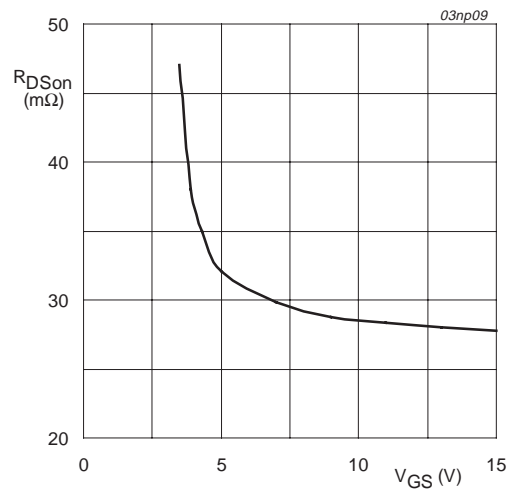
**Table 5: Characteristics**
*T<sub>j</sub> = 25 °C unless otherwise specified*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
V <sub>(BR)DSS</sub>	drain-source breakdown voltage	I <sub>D</sub> = 0.25 mA; V <sub>GS</sub> = 0 V T <sub>j</sub> = 25 °C	55	-	-	V
		T <sub>j</sub> = -55 °C	50	-	-	V
V <sub>GS(th)</sub>	gate-source threshold voltage	I <sub>D</sub> = 1 mA; V <sub>DS</sub> = V <sub>GS</sub> ; Figure 9				
		T <sub>j</sub> = 25 °C	1.1	1.5	2	V
		T <sub>j</sub> = 175 °C	0.5	-	-	V
		T <sub>j</sub> = -55 °C	-	-	2.3	V
I <sub>DSS</sub>	drain-source leakage current	V <sub>DS</sub> = 55 V; V <sub>GS</sub> = 0 V T <sub>j</sub> = 25 °C	-	0.02	1	μA
		T <sub>j</sub> = 175 °C	-	-	500	μA
I <sub>GSS</sub>	gate-source leakage current	V <sub>GS</sub> = ±15 V; V <sub>DS</sub> = 0 V	-	2	100	nA
R <sub>DS(on)</sub>	drain-source on-state resistance	V <sub>GS</sub> = 5 V; I <sub>D</sub> = 15 A; Figure 7 and 8				
		T <sub>j</sub> = 25 °C	-	34	40	mΩ
		T <sub>j</sub> = 175 °C	-	-	84	mΩ
		V <sub>GS</sub> = 4.5 V; I <sub>D</sub> = 15 A	-	-	45	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 15 A	-	32	36	mΩ
<b>Dynamic characteristics</b>						
Q <sub>g(tot)</sub>	total gate charge	V <sub>GS</sub> = 5 V; V <sub>DD</sub> = 44 V; I <sub>D</sub> = 15 A; Figure 14	-	11	-	nC
Q <sub>gs</sub>	gate-to-source charge		-	2	-	nC
Q <sub>gd</sub>	gate-to-drain (Miller) charge		-	5	-	nC
C <sub>iss</sub>	input capacitance	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 25 V; f = 1 MHz; Figure 12	-	765	1020	pF
C <sub>oss</sub>	output capacitance		-	123	148	pF
C <sub>rss</sub>	reverse transfer capacitance		-	71	97	pF
t <sub>d(on)</sub>	turn-on delay time	V <sub>DD</sub> = 30 V; R <sub>L</sub> = 2.2 Ω; V <sub>GS</sub> = 5 V; R <sub>G</sub> = 10 Ω	-	17	-	ns
t <sub>r</sub>	rise time		-	93	-	ns
t <sub>d(off)</sub>	turn-off delay time		-	35	-	ns
t <sub>f</sub>	fall time		-	72	-	ns
<b>Source-drain diode</b>						
V <sub>SD</sub>	source-drain (diode forward) voltage	I <sub>S</sub> = 20 A; V <sub>GS</sub> = 0 V; Figure 15	-	0.85	1.2	V
t <sub>rr</sub>	reverse recovery time	I <sub>S</sub> = 20 A; dI <sub>S</sub> /dt = -100 A/μs	-	45	-	ns
Q <sub>r</sub>	recovered charge	V <sub>GS</sub> = -10 V; V <sub>DS</sub> = 30 V	-	25	-	nC



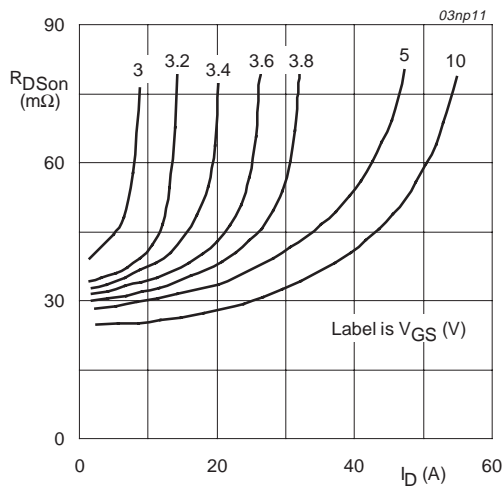
$T_j = 25\text{ }^\circ\text{C}; t_p = 300\text{ }\mu\text{s}$

**Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.**



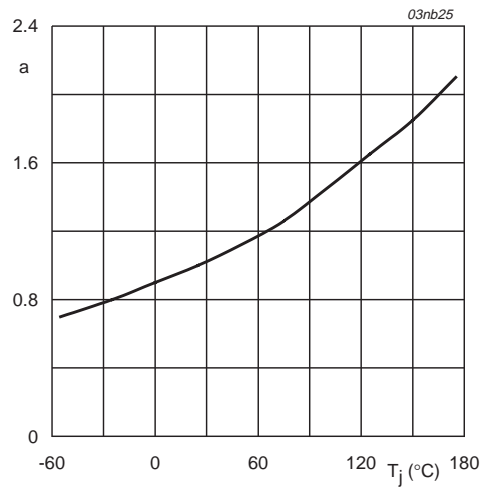
$T_j = 25\text{ }^\circ\text{C}; I_D = 15\text{ A}$

**Fig 6. Drain-source on-state resistance as a function of gate-source voltage; typical values.**



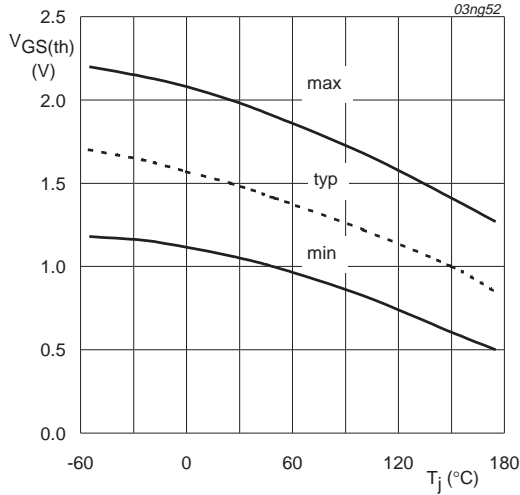
$T_j = 25\text{ }^\circ\text{C}$

**Fig 7. Drain-source on-state resistance as a function of drain current; typical values.**



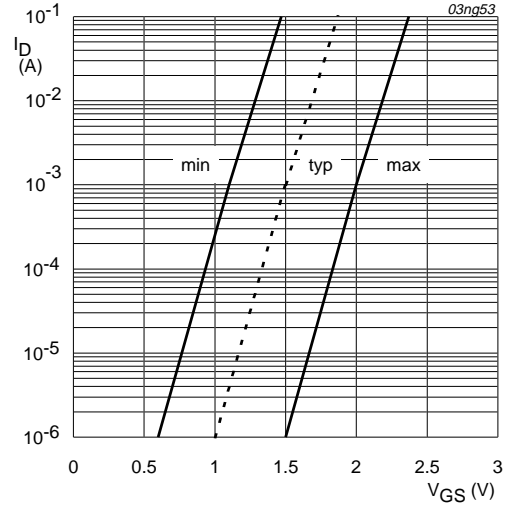
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

**Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.**



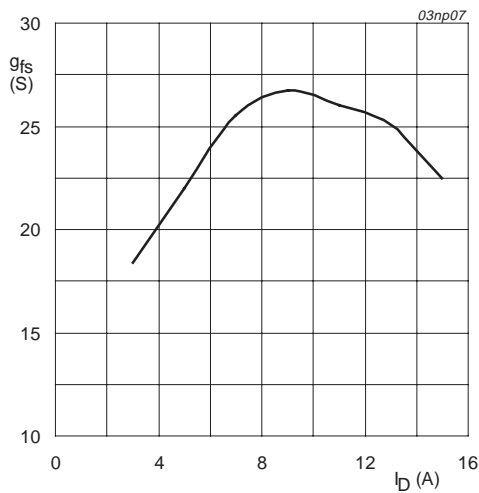
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

**Fig 9. Gate-source threshold voltage as a function of junction temperature.**



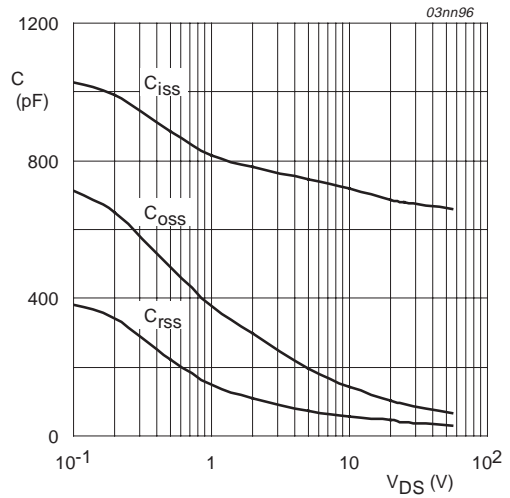
$T_j = 25 \text{ }^{\circ}C; V_{DS} = V_{GS}$

**Fig 10. Sub-threshold drain current as a function of gate-source voltage.**



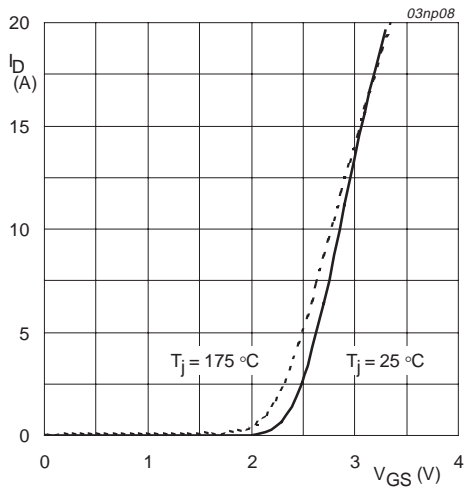
$T_j = 25 \text{ }^{\circ}C; V_{DS} = 25 \text{ V}$

**Fig 11. Forward transconductance as a function of drain current; typical values.**



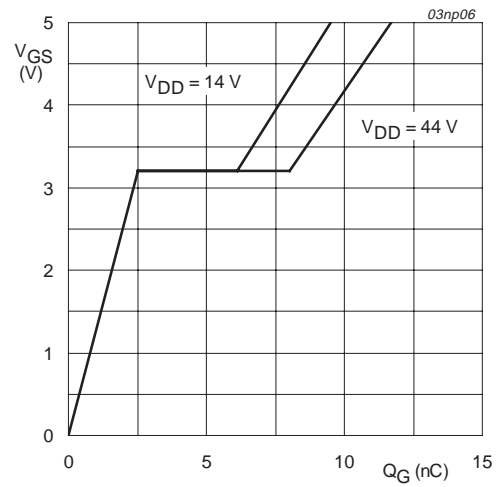
$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

**Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.**



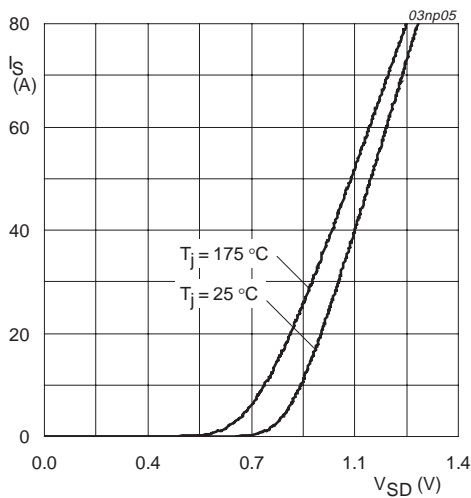
$V_{DS} = 25\text{ V}$

**Fig 13. Transfer characteristics: drain current as a function of gate-source voltage; typical values.**



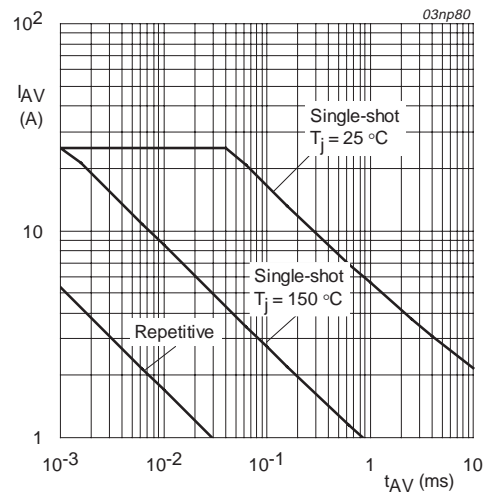
$T_j = 25^\circ\text{C}$ ;  $I_D = 15\text{ A}$

**Fig 14. Gate-source voltage as a function of gate charge; typical values.**



$V_{GS} = 0\text{ V}$

**Fig 15. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.**



See [Table note \[1\]](#) to [Table 3 "Limiting values"](#)

**Fig 16. Single-shot and repetitive avalanche rating; avalanche current as a function of avalanche period.**



**7. Package outline**

Plastic single-ended surface mounted package (Philips version LFPAK); 4 leads

SOT669

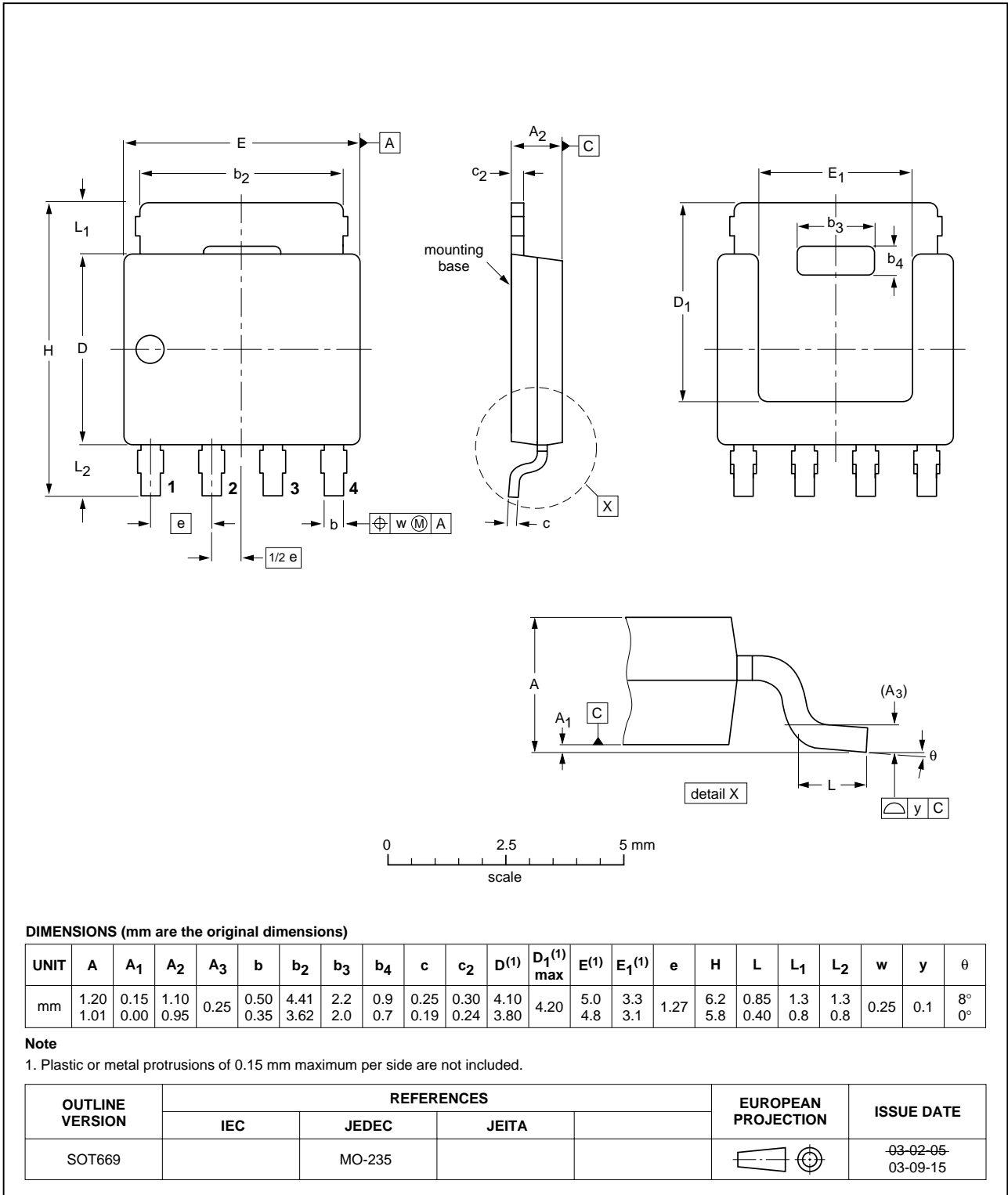


Fig 17. SOT669 (LFPAK).

## 8. Revision history

Table 6: Revision history

Rev	Date	CPCN	Description
01	20040528	-	Product data (9397 750 13189)

## 9. Data sheet status

Level	Data sheet status <sup>[1]</sup>	Product status <sup>[2][3]</sup>	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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