PC100 Registered DIMM(168pin) Intel Type Rev1.2 SPD Specification(128Mb A-die base)

Rev. 0.0

August 1999

M377S1723AT3-C1H/C1L (1.2ver)

- Organization : 16MX72
- Composition : 16MX8 *9
- Used component part # : K4S280832A-TC1H/C1L
- # of rows in module : 1 Row
- # of banks in component : 4 banks
- Feature : 1,500 mil height & double sided component
- Refresh : 4K/64ms
- **Contents** :

Byte #	Function described	Function Supported		Hex value		Note
		-1H	-1L	-1H	-1L	
0	# of bytes written into serial memory at module manufacturer	128bytes		80h		
1	Total # of bytes of SPD memory device	256bytes (2K-bit)		08h		
2	Fundamental memory type	SDRAM		04h		
3	# of row address on this assembly	12		0Ch		1
4	# of column address on this assembly	10		0Ah		1
5	# of module Rows on this assembly	1 Row		01h		
6	Data width of this assembly	72 bits		48h		
7	..... Data width of this assembly	-		00h		
8	Voltage interface standard of this assembly	LVTTL		01h		
9	SDRAM cycle time from clock @CAS latency of 3	10ns	10ns	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	60h	60h	2
11	DIMM configuraion type	ECC		02h		
12	Refresh rate & type	15.625us, support self refresh		80h		
13	Primary SDRAM width	x8		08h		
14	Error checking SDRAM width	x8		08h		
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK		01h		
16	SDRAM device attributes : Burst lengths supported	1, 2, 4 , 8 and full page		8Fh		
17	SDRAM device attributes : # of banks on SDRAM device	4 banks		04h		
18	SDRAM device attributes : CAS latency	2 & 3		06h		
19	SDRAM device attributes : CS latency	0 CLK		01h		
20	SDRAM device attributes : Write latency	0 CLK		01h		
21	SDRAM module attributes	Registered/Buffered DQM, address & control inputs and On-card PLL		1Fh		
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge		0Eh		
23	SDRAM cycle time @CAS latency of 2	10ns	12ns	A0h	C0h	2
24	SDRAM access time @CAS latency of 2	6ns	7ns	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	00h	00h	2
26	SDRAM access time @CAS latency of 1	-	-	00h	00h	2
27	Minimum row precharge time (=tRP)	20ns	20ns	14h	14h	
28	Minimum row active to row active delay (tRRD)	20ns	20ns	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	14h	14h	
30	Minimum activate precharge time (=tRAS)	50ns	50ns	32h	32h	
31	Module Row density	1 Row of 128MB		20h		
32	Command and Address signal input setup time	2ns		20h		
33	Command and Address signal input hold time	1ns		10h		
34	Data signal input setup time	2ns		20h		

SERIAL PRESENCE DETECT INFORMATION

Byte #	Function described	Function Supported		Hex value		Note
		-1H	-1L	-1H	-1L	
35	Data signal input hold time	1ns		10h		
36~61	Superset information (maybe used in future)	-		00h		
62	SPD data revision code	Current release Intel spd 1.2A		12h		
63	Checksum for bytes 0 ~ 62	-		47h	77h	
64	Manufacturer JEDEC ID code	Samsung		CEh		
65~71	..... Manufacturer JEDEC ID code	Samsung		00h		
72	Manufacturing location	Onyang Korea		01h		
73	Manufacturer part # (Memory module)	M		4Dh		
74	Manufacturer part # (DIMM configuration)	3		33h		
75	Manufacturer part # (Data bits)	Blank		20h		
76	..... Manufacturer part # (Data bits)	7		37h		
77	..... Manufacturer part # (Data bits)	7		37h		
78	Manufacturer part # (Mode & operating voltage)	S		53h		
79	Manufacturer part # (Module depth)	1		31h		
80	..... Manufacturer part # (Module depth)	7		37h		
81	Manufacturer part # (Refresh, # of banks in Comp. & inter-	2		32h		
82	Manufacturer part # (Composition component)	3		33h		
83	Manufacturer part # (Component revision)	A		41h		
84	Manufacturer part # (Package type)	T		54h		
85	Manufacturer part # (PCB revision & type)	3		33h		
86	Manufacturer part # (Hyphen)	" - "		2Dh		
87	Manufacturer part # (Power)	C		43h		
88	Manufacturer part # (Minimum cycle time)	1	1	31h	31h	
89	Manufacturer part # (Minimum cycle time)	H	L	48h	4Ch	
90	Manufacturer part # (TBD)	Blank		20h		
91	Manufacturer revision code (For PCB)	3		33h		
92	..... Manufacturer revision code (For component)	A-die (2nd Gen.)		41h		
93	Manufacturing date (Week)	-		-		3
94	Manufacturing date (Year)	-		-		3
95~98	Assembly serial #	-		-		4
99~125	Manufacturer specific data (may be used in future)	Undefined		-		5
126	System frequency for 100MHz	100MHz		64h		
127	Intel Specification details	Detailed 100MHz Information		8Fh	8Dh	
128+	Unused storage locations	Undefined		-		5

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year with BCD format.
4. These bytes are programmed by Samsung ′s own Assembly Serial # system. All modules may have different unique serial #.
5. These bytes are Undefined and can be used for Samsung ′s own purpose.

M377S3320AT3-C1H/C1L (1.2ver)

- Organization : 32MX72
- Composition : 32MX4 *18
- Used component part # : K4S280432A-TC1H/C1L
- # of rows in module : 1 Row
- # of banks in component : 4 banks
- Feature : 1,700 mil height & double sided component
- Refresh : 4K/64ms
- **Contents** :

Byte #	Function described	Function Supported		Hex value		Note
		-1H	-1L	-1H	-1L	
0	# of bytes written into serial memory at module manufacturer	128bytes		80h		
1	Total # of bytes of SPD memory device	256bytes (2K-bit)		08h		
2	Fundamental memory type	SDRAM		04h		
3	# of row address on this assembly	12		0Ch		1
4	# of column address on this assembly	11		0Bh		1
5	# of module Rows on this assembly	1 Row		01h		
6	Data width of this assembly	72 bits		48h		
7	..... Data width of this assembly	-		00h		
8	Voltage interface standard of this assembly	LVTTL		01h		
9	SDRAM cycle time from clock @CAS latency of 3	10ns	10ns	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	60h	60h	2
11	DIMM configuraion type	ECC		02h		
12	Refresh rate & type	15.625us, support self refresh		80h		
13	Primary SDRAM width	x4		04h		
14	Error checking SDRAM width	x4		04h		
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK		01h		
16	SDRAM device attributes : Burst lengths supported	1, 2, 4 & 8 page		0Fh		
17	SDRAM device attributes : # of banks on SDRAM device	4 banks		04h		
18	SDRAM device attributes : CAS latency	2 & 3		06h		
19	SDRAM device attributes : CS latency	0 CLK		01h		
20	SDRAM device attributes : Write latency	0 CLK		01h		
21	SDRAM module attributes	Registered/Buffered DQM, address & control inputs and On-card PLL		1Fh		
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge		0Eh		
23	SDRAM cycle time @CAS latency of 2	10ns	12ns	A0h	C0h	2
24	SDRAM access time @CAS latency of 2	6ns	7ns	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	00h	00h	2
26	SDRAM access time @CAS latency of 1	-	-	00h	00h	2
27	Minimum row precharge time (=tRP)	20ns	20ns	14h	14h	
28	Minimum row active to row active delay (tRRD)	20ns	20ns	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	14h	14h	
30	Minimum activate precharge time (=tRAS)	50ns	50ns	32h	32h	
31	Module Row density	1 Row of 256MB		40h		
32	Command and Address signal input setup time	2ns		20h		
33	Command and Address signal input hold time	1ns		10h		
34	Data signal input setup time	2ns		20h		

SERIAL PRESENCE DETECT INFORMATION

Byte #	Function described	Function Supported		Hex value		Note
		-1H	-1L	-1H	-1L	
35	Data signal input hold time	1ns		10h		
36~61	Superset information (maybe used in future)	-		00h		
62	SPD data revision code	Current release Intel spd 1.2A		12h		
63	Checksum for bytes 0 ~ 62	-		E0h	10h	
64	Manufacturer JEDEC ID code	Samsung		CEh		
65~71	..... Manufacturer JEDEC ID code	Samsung		00h		
72	Manufacturing location	Onyang Korea		01h		
73	Manufacturer part # (Memory module)	M		4Dh		
74	Manufacturer part # (DIMM configuration)	3		33h		
75	Manufacturer part # (Data bits)	Blank		20h		
76	..... Manufacturer part # (Data bits)	7		37h		
77	..... Manufacturer part # (Data bits)	7		37h		
78	Manufacturer part # (Mode & operating voltage)	S		53h		
79	Manufacturer part # (Module depth)	3		33h		
80	..... Manufacturer part # (Module depth)	3		33h		
81	Manufacturer part # (Refresh, # of banks in Comp. & inter-	2		32h		
82	Manufacturer part # (Composition component)	0		30h		
83	Manufacturer part # (Component revision)	A		41h		
84	Manufacturer part # (Package type)	T		54h		
85	Manufacturer part # (PCB revision & type)	3		33h		
86	Manufacturer part # (Hyphen)	" - "		2Dh		
87	Manufacturer part # (Power)	C		43h		
88	Manufacturer part # (Minimum cycle time)	1	1	31h	31h	
89	Manufacturer part # (Minimum cycle time)	H	L	48h	4Ch	
90	Manufacturer part # (TBD)	Blank		20h		
91	Manufacturer revision code (For PCB)	3		33h		
92	..... Manufacturer revision code (For component)	A-die (2ndGen.)		41h		
93	Manufacturing date (Week)	-		-		3
94	Manufacturing date (Year)	-		-		3
95~98	Assembly serial #	-		-		4
99~125	Manufacturer specific data (may be used in future)	Undefined		-		5
126	System frequency for 100MHz	100MHz		64h		
127	Intel Specification details	Detailed 100MHz Information		8Fh	8Dh	
128+	Unused storage locations	Undefined		-		5

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year with BCD format.
4. These bytes are programmed by Samsung ′s own Assembly Serial # system. All modules may have different unique serial #.
5. These bytes are Undefined and can be used for Samsung ′s own purpose.

M377S3323AT0-C1H/C1L

- Organization : 32MX72
- Composition : 16MX8 *18
- Used component part # : K4S280832A-TC1H/C1L
- # of banks in module : 2 Rows
- # of banks in component : 4 banks
- Feature : 1,700 mil height & double sided component
- Refresh : 4K/64ms
- **Contents** :

Byte #	Function described	Function Supported		Hex value		Note
		-1H	-1L	-1H	-1L	
0	# of bytes written into serial memory at module manufacturer	128bytes		80h		
1	Total # of bytes of SPD memory device	256bytes (2K-bit)		08h		
2	Fundamental memory type	SDRAM		04h		
3	# of row address on this assembly	12		0Ch		1
4	# of column address on this assembly	10		0Ah		1
5	# of module Rows on this assembly	2 Rows		02h		
6	Data width of this assembly	72 bits		48h		
7	..... Data width of this assembly	-		00h		
8	Voltage interface standard of this assembly	LVTTL		01h		
9	SDRAM cycle time from clock @CAS latency of 3	10ns	10ns	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	60h	60h	2
11	DIMM configuraion type	ECC		02h		
12	Refresh rate & type	15.625us, support self refresh		80h		
13	Primary SDRAM width	x8		08h		
14	Error checking SDRAM width	x8		08h		
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK		01h		
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page		8Fh		
17	SDRAM device attributes : # of banks on SDRAM device	4 banks		04h		
18	SDRAM device attributes : CAS latency	2 & 3		06h		
19	SDRAM device attributes : CS latency	0 CLK		01h		
20	SDRAM device attributes : Write latency	0 CLK		01h		
21	SDRAM module attributes	Registered/Buffered DQM, address & control inputs and On-card PLL		1Fh		
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge		0Eh		
23	SDRAM cycle time @CAS latency of 2	10ns	12ns	A0h	C0h	2
24	SDRAM access time @CAS latency of 2	6ns	7ns	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	00h	00h	2
26	SDRAM access time @CAS latency of 1	-	-	00h	00h	2
27	Minimum row precharge time (=tRP)	20ns	20ns	14h	14h	
28	Minimum row active to row active delay (tRRD)	20ns	20ns	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	14h	14h	
30	Minimum activate precharge time (=tRAS)	50ns	50ns	32h	32h	
31	Module Row density	2 Rows of 128MB		20h		
32	Command and Address signal input setup time	2ns		20h		
33	Command and Address signal input hold time	1ns		10h		
34	Data signal input setup time	2ns		20h		

SERIAL PRESENCE DETECT INFORMATION

Byte #	Function described	Function Supported		Hex value		Note
		-1H	-1L	-1H	-1L	
35	Data signal input hold time	1ns		10h		
36~61	Superset information (maybe used in future)	-		00h		
62	SPD data revision code	Current release Intel spd 1.2A		12h		
63	Checksum for bytes 0 ~ 62	-		48h	78h	
64	Manufacturer JEDEC ID code	Samsung		CEh		
65~71	..... Manufacturer JEDEC ID code	Samsung		00h		
72	Manufacturing location	Onyang Korea		01h		
73	Manufacturer part # (Memory module)	M		4Dh		
74	Manufacturer part # (DIMM configuration)	3		33h		
75	Manufacturer part # (Data bits)	Blank		20h		
76	..... Manufacturer part # (Data bits)	7		37h		
77	..... Manufacturer part # (Data bits)	7		37h		
78	Manufacturer part # (Mode & operating voltage)	S		53h		
79	Manufacturer part # (Module depth)	3		33h		
80	..... Manufacturer part # (Module depth)	3		33h		
81	Manufacturer part # (Refresh, # of banks in Comp. & inter-	2		32h		
82	Manufacturer part # (Composition component)	3		33h		
83	Manufacturer part # (Component revision)	A		41h		
84	Manufacturer part # (Package type)	T		54h		
85	Manufacturer part # (PCB revision & type)	0		30h		
86	Manufacturer part # (Hyphen)	" - "		2Dh		
87	Manufacturer part # (Power)	C		43h		
88	Manufacturer part # (Minimum cycle time)	1	1	31h	31h	
89	Manufacturer part # (Minimum cycle time)	H	L	48h	4Ch	
90	Manufacturer part # (TBD)	Blank		20h		
91	Manufacturer revision code (For PCB)	0		30h		
92	..... Manufacturer revision code (For component)	A-die (2nd Gen.)		41h		
93	Manufacturing date (Week)	-		-		3
94	Manufacturing date (Year)	-		-		3
95~98	Assembly serial #	-		-		4
99~125	Manufacturer specific data (may be used in future)	Undefined		-		5
126	System frequency for 100MHz	100MHz		64h		
127	Intel Specification details	Detailed 100MHz Information		8Fh	8Dh	
128+	Unused storage locations	Undefined		-		5

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year with BCD format.
4. These bytes are programmed by Samsung ′s own Assembly Serial # system. All modules may have different unique serial #.
5. These bytes are Undefined and can be used for Samsung ′s own purpose.

M377S6428AT3-C1H/C1L (1.2ver)

- Organization : 64MX72
- Composition : 64MX4 *18
- Used component part # : K4S560632A-TC1H/C1L
- # of rows in module : 2 Rows
- # of banks in component : 4 banks
- Feature : 1,700 mil height & double sided component
- Refresh : 4K/64ms
- **Contents** :

Byte #	Function described	Function Supported		Hex value		Note
		-1H	-1L	-1H	-1L	
0	# of bytes written into serial memory at module manufacturer	128bytes		80h		
1	Total # of bytes of SPD memory device	256bytes (2K-bit)		08h		
2	Fundamental memory type	SDRAM		04h		
3	# of row address on this assembly	12		0Ch		1
4	# of column address on this assembly	11		0Bh		1
5	# of module Rows on this assembly	2 Rows		02h		
6	Data width of this assembly	72 bits		48h		
7	..... Data width of this assembly	-		00h		
8	Voltage interface standard of this assembly	LVTTL		01h		
9	SDRAM cycle time from clock @CAS latency of 3	10ns	10ns	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	60h	60h	2
11	DIMM configuraion type	ECC		02h		
12	Refresh rate & type	15.625us, support self refresh		80h		
13	Primary SDRAM width	x4		04h		
14	Error checking SDRAM width	x4		04h		
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK		01h		
16	SDRAM device attributes : Burst lengths supported	1, 2, 4 & 8 page		0Fh		
17	SDRAM device attributes : # of banks on SDRAM device	4 banks		04h		
18	SDRAM device attributes : CAS latency	2 & 3		06h		
19	SDRAM device attributes : CS latency	0 CLK		01h		
20	SDRAM device attributes : Write latency	0 CLK		01h		
21	SDRAM module attributes	Registered/Buffered DQM, address & control inputs and On-card PLL		1Fh		
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge		0Eh		
23	SDRAM cycle time @CAS latency of 2	10ns	12ns	A0h	C0h	2
24	SDRAM access time @CAS latency of 2	6ns	7ns	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	00h	00h	2
26	SDRAM access time @CAS latency of 1	-	-	00h	00h	2
27	Minimum row precharge time (=tRP)	20ns	20ns	14h	14h	
28	Minimum row active to row active delay (tRRD)	20ns	20ns	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	14h	14h	
30	Minimum activate precharge time (=tRAS)	50ns	50ns	32h	32h	
31	Module Row density	2 Rows of 256MB		40h		
32	Command and Address signal input setup time	2ns		20h		
33	Command and Address signal input hold time	1ns		10h		
34	Data signal input setup time	2ns		20h		

SERIAL PRESENCE DETECT INFORMATION

Byte #	Function described	Function Supported		Hex value		Note
		-1H	-1L	-1H	-1L	
35	Data signal input hold time	1ns		10h		
36~61	Superset information (maybe used in future)	-		00h		
62	SPD data revision code	Current release Intel spd 1.2A		12h		
63	Checksum for bytes 0 ~ 62	-		E1h	11h	
64	Manufacturer JEDEC ID code	Samsung		CEh		
65~71	..... Manufacturer JEDEC ID code	Samsung		00h		
72	Manufacturing location	Onyang Korea		01h		
73	Manufacturer part # (Memory module)	M		4Dh		
74	Manufacturer part # (DIMM configuration)	3		33h		
75	Manufacturer part # (Data bits)	Blank		20h		
76	..... Manufacturer part # (Data bits)	7		37h		
77	..... Manufacturer part # (Data bits)	7		37h		
78	Manufacturer part # (Mode & operating voltage)	S		53h		
79	Manufacturer part # (Module depth)	6		36h		
80	..... Manufacturer part # (Module depth)	4		34h		
81	Manufacturer part # (Refresh, # of banks in Comp. & inter-	2		32h		
82	Manufacturer part # (Composition component)	8		38h		
83	Manufacturer part # (Component revision)	A		41h		
84	Manufacturer part # (Package type)	T		54h		
85	Manufacturer part # (PCB revision & type)	3		33h		
86	Manufacturer part # (Hyphen)	" - "		2Dh		
87	Manufacturer part # (Power)	C		43h		
88	Manufacturer part # (Minimum cycle time)	1	1	31h	31h	
89	Manufacturer part # (Minimum cycle time)	H	L	48h	4Ch	
90	Manufacturer part # (TBD)	Blank		20h		
91	Manufacturer revision code (For PCB)	3		33h		
92	..... Manufacturer revision code (For component)	A-die (2nd Gen.)		41h		
93	Manufacturing date (Week)	-		-		3
94	Manufacturing date (Year)	-		-		3
95~98	Assembly serial #	-		-		4
99~125	Manufacturer specific data (may be used in future)	Undefined		-		5
126	System frequency for 100MHz	100MHz		64h		
127	Intel Specification details	Detailed 100MHz Information		8Fh	8Dh	
128+	Unused storage locations	Undefined		-		5

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year with BCD format.
4. These bytes are programmed by Samsung ′s own Assembly Serial # system. All modules may have different unique serial #.
5. These bytes are Undefined and can be used for Samsung ′s own purpose.