

Document Title

**128Kx8 Super Low Power and Low Voltage
Full CMOS SRAM Data Sheets for 48-CSP**

Revision History

<u>Rev. No.</u>	<u>History</u>	<u>Draft Data</u>	<u>Remark</u>
Rev. 0.0	- 1'st edition - Package Dimension Finalized	Feb. 6'th, 1997	Preliminary
Rev. 0.1	- 2'nd edition - Change speed marking method Marking was indicate speed at high power, that change to speed at low power	Apr. 18'th, 1997	Preliminary

The attached data sheets are prepared and approved by SAMSUNG Electronics. SAMSUNG Electronics CO., LTD. reserve the right to change the specifications. SAMSUNG Electronics will evaluate and reply to your requests and questions on the parameters of this device. If you have any questions, please contact the SAMSUNG branch office near your office, call or contact Headquarters.

KM68FS1000Z, KM68FR1000Z Family

128Kx8 bit Super Low Power and Low Voltage Full CMOS SRAM with 48-CSP(Chip Scale Package)

FEATURES SUMMARY

- Process Technology : 0.4μm Full CMOS
- Organization : 128Kx8
- Power Supply Voltage
 - KM68FS1000Z Family : 2.3V(Min) ~ 3.3V(Max)
 - KM68FR1000Z Family : 1.8V(Min) ~ 2.7V(Max)
- Low Data Retention Voltage : 1.5V(Min)
- Three state output and TTL Compatible
- Package Type : 48-CSP with 0.75mm ball pitch

GENERAL DESCRIPTION

The KM68FS1000Z and KM68FR1000Z family are fabricated by SAMSUNG's advanced Full CMOS process technology. The family can support various operating temperature ranges and has very small size with 0.75 ball pitch and 6 x 8 ball array. The family also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

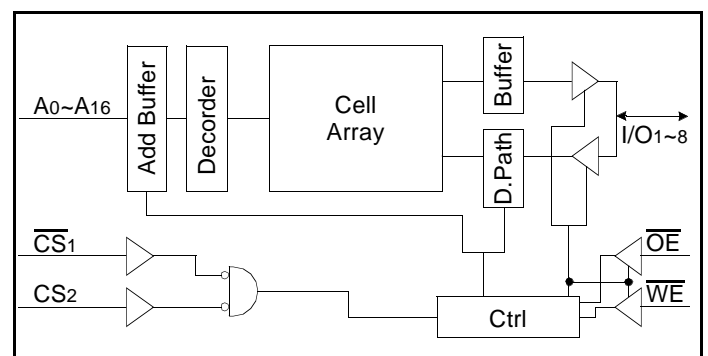
Product Family	Operating Temp.Range	Vcc Range	Speed (ns)	Power Dissipation		PKG Type
				Standby (I _{SB1})	Operating (I _{CC2})	
KM68FS1000Z	Commercial (0~70°C)	2.3~3.3V	100* @ V _{CC} =3.0±0.3V 150* @ V _{CC} =2.5±0.2V	10μA (Max)	55mA(Max) 30mA(Max)	48-CSP (6x8 ball area with 0.75mm ball pitch)
KM68FR1000Z		1.8~2.7V	300* @ V _{CC} =2.0±0.2V		15mA(Max)	
KM68FS1000ZI	Industrial (-40~85°C)	2.3~3.3V	100* @ V _{CC} =3.0±0.3V 150* @ V _{CC} =2.5±0.2V	10μA (Max)	55mA(Max) 30mA(Max)	
KM68FR1000ZI		1.8~2.7V	300* @ V _{CC} =2.0±0.2V		15mA(Max)	

48-CSP PIN TOP VIEW

	1	2	3	4	5	6
A	A0	A1	CS ₂	A3	A6	A8
B	I/O ₅	A2	\overline{WE}	A4	A7	I/O ₁
C	I/O ₆		NC	A5		I/O ₂
D	V _{SS}					V _{CC}
E	V _{CC}					V _{SS}
F	I/O ₇		NC	NC		I/O ₃
G	I/O ₈	\overline{OE}	\overline{CS}_1	A16	A15	I/O ₄
H	A9	A10	A11	A12	A13	A14

* See last page for package dimension.

FUNCTIONAL BLOCK DIAGRAM



Name	Function	Name	Function
A0~A16	Address Inputs	V _{CC}	Power
\overline{WE}	Write Enable Input	V _{SS}	Ground
\overline{CS}_1, CS_2	Chip Select Input	I/O ₁ ~I/O ₈	Data Inputs/Outputs
\overline{OE}	Output Enable	N.C.	No Connection

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KM68FS1000Z, KM68FR1000Z Family

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PRODUCT LIST & ORDERING INFORMATION

PRODUCT LIST

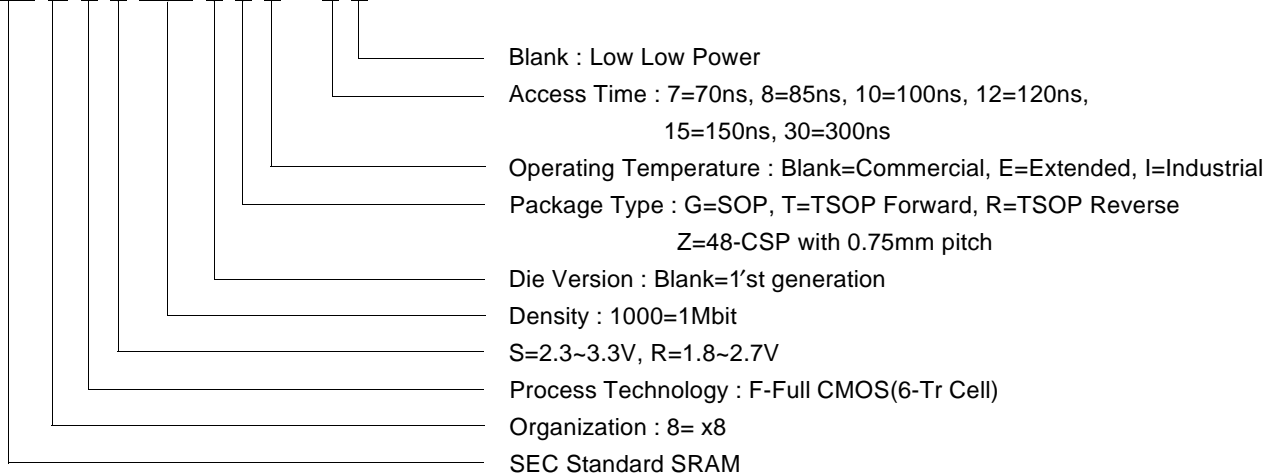
Commercial Temp Product (0~70°C)		Industrial Temp Product (-40~85°C)	
Part Name	Function	Part Name	Function
KM68FS1000Z-15	48-CSP, 2.5V/3.0V, 150/100ns	KM68FS1000Z-15	48-CSP, 2.5V/3.0V, 150/100ns
KM68FR1000Z-30	48-CSP, 1.8V/2.5V, 300ns	KM68FR1000Z-30	48-CSP, 1.8V/2.5V, 300ns

* The meaning of 2.5V/3.0V, 150/100ns is that the operating V_{cc} is ranged from 2.3V(Min) to 3.3V(Max) with speed 150ns @2.5V±0.2 and 100ns @3.0V±0.3. This type of meaning is applied to other notations like the example.

** But in case of KM68FR1000Z-30, there is only one speed bin, 300ns though it supports wide range operating V_{cc}.

ORDERING INFORMATION

KM6 8 X X 1000 X X X - X X



KM68FS1000Z, KM68FR1000Z Family

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ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-0.2 to 3.6V	V	-
Voltage on Vcc supply relative to Vss	V _{CC}	-0.2 to 4.0V	V	-
Power Dissipation	P _D	1.0	W	-
Storage temperature	T _{STG}	-55 to 150	°C	-
Operating Temperature	T _A	0 to 70	°C	KM68FS1000Z KM68FR1000Z
		-40 to 85	°C	KM68FS1000ZI KM68FR1000ZI
Soldering temperature and time	T _{SOLDER}	260°C, 5sec(Lead Only)	-	-

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Item	Symbol	Product	Min	Typ**	Max	Unit	
Supply voltage	V _{CC}	KM68FS1000Z Family	2.3	2.5/3.0	3.3	V	
		KM68FR1000Z Family	1.8	2.0/2.5	2.7	V	
Ground	V _{SS}	All Family	0	0	0	V	
Input high voltage	V _{IH}	KM68FS1000Z Family	V _{CC} =3.0V±0.2V	2.2	-	V _{CC} +0.2	V
			V _{CC} =2.5V±0.2V	2.0	-	V _{CC} +0.2	V
		KM68FR1000Z Family	V _{CC} =2.5V±0.2V	2.0	-	V _{CC} +0.2	V
			V _{CC} =2.0V±0.2V	1.6	-	V _{CC} +0.2	V
Input low voltage	V _{IL}	All Family	-0.2***	-	0.4	V	

* 1) Commercial Product : T_A=0 to 70°C, unless otherwise specified

2) Industrial Product : T_A=-40 to 85°C, unless otherwise specified

** T_A=25°C

*** V_{IL}(Min)=-1.5V for ≤30ns pulse width

CAPACITANCE* (f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C _{IN}	V _{IN} =0V	-	8	pF
Input/Output capacitance	C _{IO}	V _{IO} =0V	-	10	pF

* Capacitance is sampled not, 100% tested

KM68FS1000Z, KM68FR1000Z Family

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DC AND OPERATING CHARACTERISTICS

Item	Symbol	Test Conditions ¹⁾	Min	Typ**	Max	Unit		
Input leakage current	I _{LI}	V _{IN} =V _{SS} to V _{CC}	-1	-	1	μA		
Output leakage current	I _{LO}	$\overline{CS}_1=V_{IH}$ or $CS_2=V_{IL}$ or $\overline{WE}=V_{IL}$, V _{IO} =V _{SS} to V _{CC}	-1	-	1	μA		
Operating power supply current	I _{CC}	$\overline{CS}_1=V_{IL}$, CS ₂ =V _{IH} V _{IN} =V _{IH} or V _{IL} , I _{IO} =0mA	Read	-	-	5 ⁵⁾	mA	
			Write	-	-	15 ⁵⁾		
Average operating current	I _{CC1}	Cycle time=1μs 100% duty, $\overline{CS}_1 \leq 0.2V$, CS ₂ ≥ V _{IN} ≥ V _{CC} -0.2V	Read	-	-	5 ⁵⁾	mA	
			Write	-	-	15 ⁵⁾		
	I _{CC2}	Min cycle, 100% duty, I _{IO} =0mA, $\overline{CS}_1=V_{IL}$, or CS ₂ =V _{IH}	V _{CC} =3.3V@100ns	-	-	55 ⁴⁾	mA	
V _{CC} =2.7V@150ns	-	-	30					
V _{CC} =2.2V@300ns	-	-	15					
Output low voltage	V _{OL}	I _{OL}	V _{CC} =3.0V	2.1mA	-	-	0.4	V
			V _{CC} =2.5V	0.5mA	-	-	0.4	
			V _{CC} =2.0V	0.33mA	-	-	0.4	
Output high voltage	V _{OH}	I _{OH}	V _{CC} =3.0V	-1.0mA	2.4	-	-	V
			V _{CC} =2.5V	-0.5mA	2.0	-	-	
			V _{CC} =2.0V	-0.44mA	1.6	-	-	
Standby Current(TTL)	I _{SB}	$\overline{CS}_1=V_{IH}$, or CS ₂ =V _{IL}	-	-	0.3	mA		
Standby Current (CMOS)	KM68FS1000Z KM68FR1000Z	I _{SB1}	$\overline{CS}_1 \geq V_{CC}-0.2V$ CS ₂ ≥ V _{CC} -0.2V or CS ₂ ≤ 0.2V, Other input =0~V _{CC}	Low Low Power	-	0.05	5 ²⁾	μA
	KM68FS1000ZI KM68FR1000ZI			Low Low Power	-	0.05	5 ²⁾	μA

1) - Commercial Product

T_A=0 to 70°C, V_{CC}=2.3V(Min) ~ 3.3V(Max) for 68FS1000Z Family, V_{CC}=1.8V(Min) ~ 2.7V(Max)V for 68FR1000Z Family

- Industrial Product

T_A=-40 to 85°C, V_{CC}=2.3V(Min) ~ 3.3V(Max) for 68FS1000ZI Family, V_{CC}=1.8V(Min)~2.7V(Max) for 68FR1000ZI Family.

2) The value has difference by ±1μA.

Measured at V_{CC}=3.3V(Max)

3) The value is not 100% tested but obtained statistically at Temp=25°C

4) - The value is measured at V_{CC}=3.0V±0.3V

- I_{CC2}=30mA with 120ns cycle at V_{CC}=2.5V±0.2V, but this value is not 100% tested but obtained statistically.

- I_{CC2}=15mA with 300ns cycle at V_{CC}=2.0V±0.2V, but this value is not 100% tested but obtained statistically.

5) The value is measured at V_{CC}=3.0V±0.3V

KM68FS1000Z, KM68FR1000Z Family

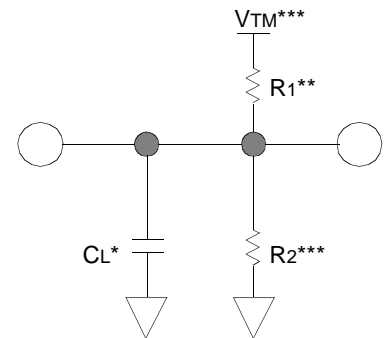
Preliminary
CMOS SRAM

AC OPERATING CONDITIONS

TEST CONDITIONS(1. Test Load and Test Input/Output Reference)*

Item	Value	Remark
Input pulse level	0.4 to 2.2V	V _{CC} =3.0V, 2.5V
	0.4 to 1.8V	V _{CC} =2.0V
Input rising and falling time	5ns	-
input and output reference voltage	1.5V	V _{CC} =3.0V
	1.1V	V _{CC} =2.5V
	0.9V	V _{CC} =2.0V,
Output load (See right)	C _L =100pF	See Test Condition #2
	C _L =30pF	

* See test condition of DC and Operating characteristics



* Including scope and jig capacitance

**R₁=3070Ω, R₂=3150Ω

***V_{TM}=2.8V for V_{CC} = 3.0V/3.3V
2.3V for V_{CC} = 2.5V
1.8V for V_{CC} = 2.0V

TEST CONDITIONS(2. Temperature and V_{CC} Conditions)

Product Family	Temperature	V _{CC} Range	Typical Supply V _{CC}	Speed	Comments
KM68FR1000Z	0~70°C	1.8(Min)~2.7(Max)	2.0V±0.2 Operation	300*ns	Commercial
KM68FS1000Z	0~70°C	2.3(Min)~3.3(Max)	2.5V±0.2 Operation	150*ns	
			3.0V±0.3 Operation	100*ns	
KM68FR1000ZI	-40~85°C	1.8(Min)~2.7(Max)	2.0V±0.2 Operation	300*ns	Industrial
KM68FS1000ZI	-40~85°C	2.3(Min)~3.3(Max)	2.5V±0.2 Operation	150*ns	
			3.0V±0.3 Operation	100*ns	

* All the parameters are measured with 30pF test load

AC CHARACTERISTICS

Parameter List		Symbol	Speed Bins						Units
			100ns		150ns		300ns		
			Min	Max	Min	Max	Min	Max	
Read	Read cycle time	t _{RC}	100	-	150	-	300	-	ns
	Address access time	t _{AA}	-	100	-	150	-	300	ns
	Chip select to output	t _{CO1}	-	100	-	150	-	300	ns
	Output enable to valid output	t _{OE}	-	50	-	75	-	150	ns
	Chip select to low-Z output	t _{LZ1,tLZ2}	10	-	20	-	50	-	ns
	Output enable to low-Z output	t _{OLZ}	5	-	20	-	30	-	ns
	Chip disable to high-Z output	t _{HZ1,tHZ2}	0	30	0	40	0	60	ns
	Output disable to high-Z output	t _{OHZ}	0	30	0	40	0	60	ns
	Output hold from address change	t _{OH}	15	-	15	-	30	-	ns
Write	Write cycle time	t _{WC}	100	-	150	-	300	-	ns
	Chip select to end of write	t _{CW}	80	-	120	-	300	-	ns
	Address set-up time	t _{AS}	0	-	0	-	0	-	ns
	Address valid to end of write	t _{AW}	80	-	120	-	300	-	ns
	Write pulse width	t _{WP}	70	-	100	-	200	-	ns
	Write recovery	t _{WR}	0	-	0	-	0	-	ns
	Write to output high-Z	t _{WHZ}	0	30	0	40	0	60	ns
	Data to write time overlap	t _{DW}	40	-	60	-	120	-	ns
	Data hold from write time	t _{DH}	0	-	0	-	0	-	ns
	End write to output low-Z	t _{OW}	5	-	5	-	20	-	ns

DATA RETENTION CHARACTERISTICS

Item	Symbol	Test Condition*	Min	Typ**	Max	Unit
Vcc for data retention	VDR	$\overline{CS}_1^{***} \geq V_{cc} - 0.2V$	1.5	-	3.6	V
Data retention current	IDR	$V_{cc} = 3.0V$ $\overline{CS}_1 \geq V_{cc} - 0.2V$ Low Low Power	-	0.05	5	μA
Data retention set-up time	tSDR	See data retention waveform	0	-	-	ns
Recovery time	tRDR		tRC	-	-	

* 1) Commercial Product : $T_A = 0$ to $70^\circ C$, unless otherwise specified

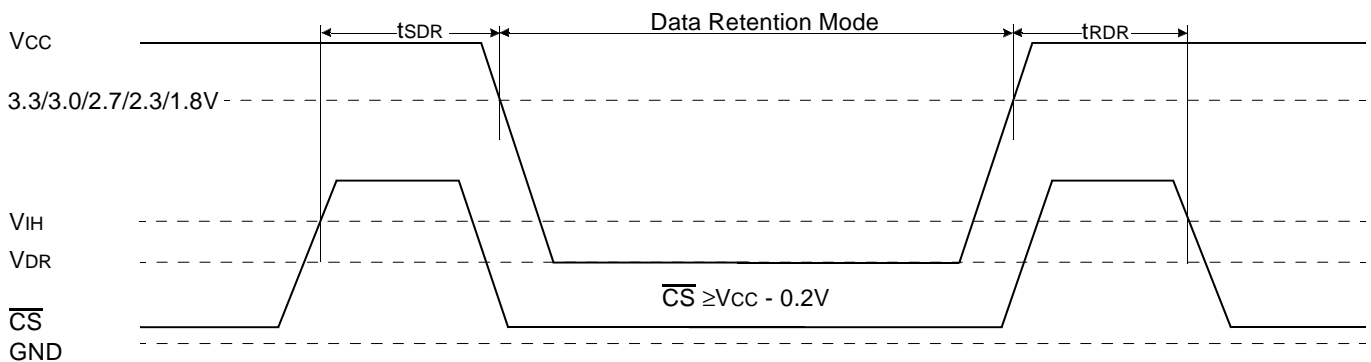
2) Industrial Product : $T_A = -40$ to $85^\circ C$, unless otherwise specified

** $T_A = 25^\circ C$, the value is too small to detect by test machine, $0.01 \mu A$ statistically

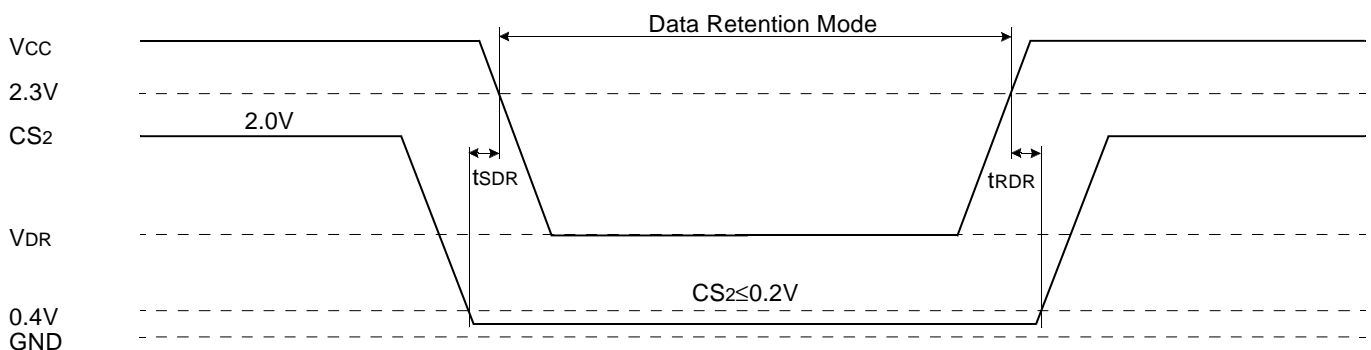
*** $\overline{CS}_1 \geq V_{cc} - 2.0V$, $CS_2 \geq V_{cc} - 2.0V$ (\overline{CS}_1 controlled) or $CS_2 \leq 2.0V$ (CS_2 controlled)

DATA RETENTION TIMING DIAGRAM

1) \overline{CS}_1 controlled

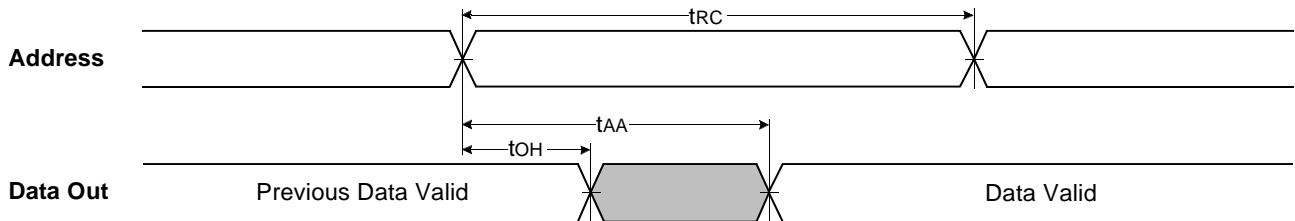


2) CS_2 controlled

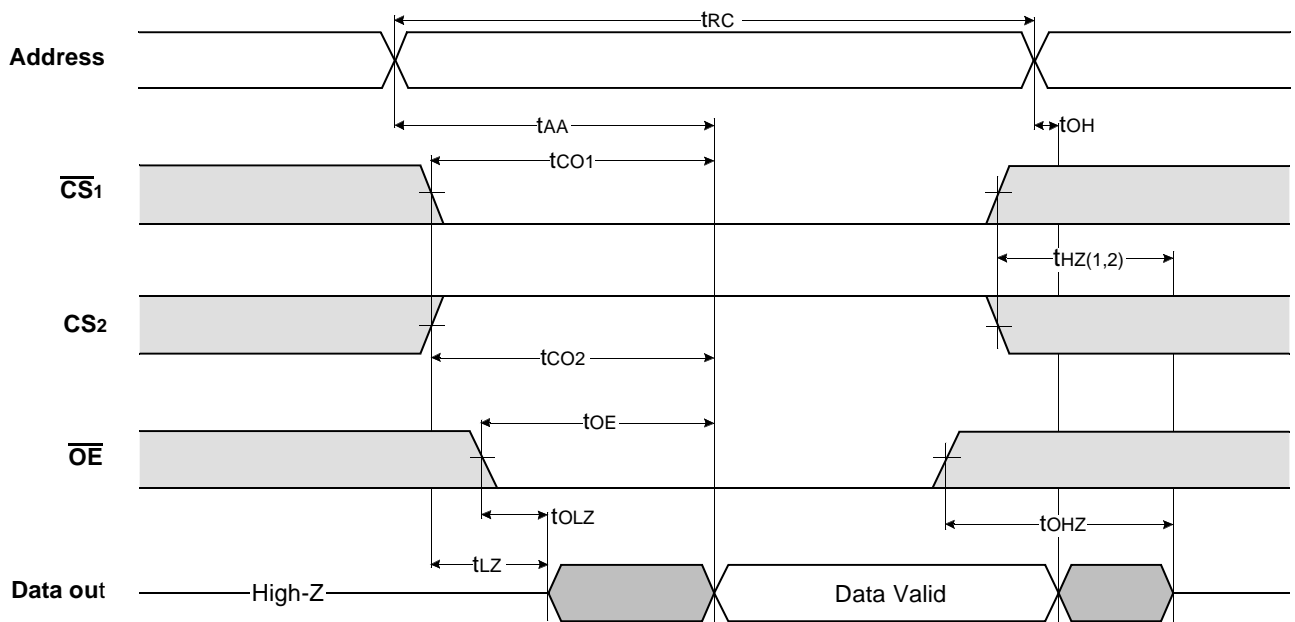


TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (1) (Address Controlled)
($\overline{CS}=\overline{OE}=V_{IL}$, $\overline{WE}=V_{IH}$, \overline{UB} or, and $\overline{LB}=V_{IL}$)



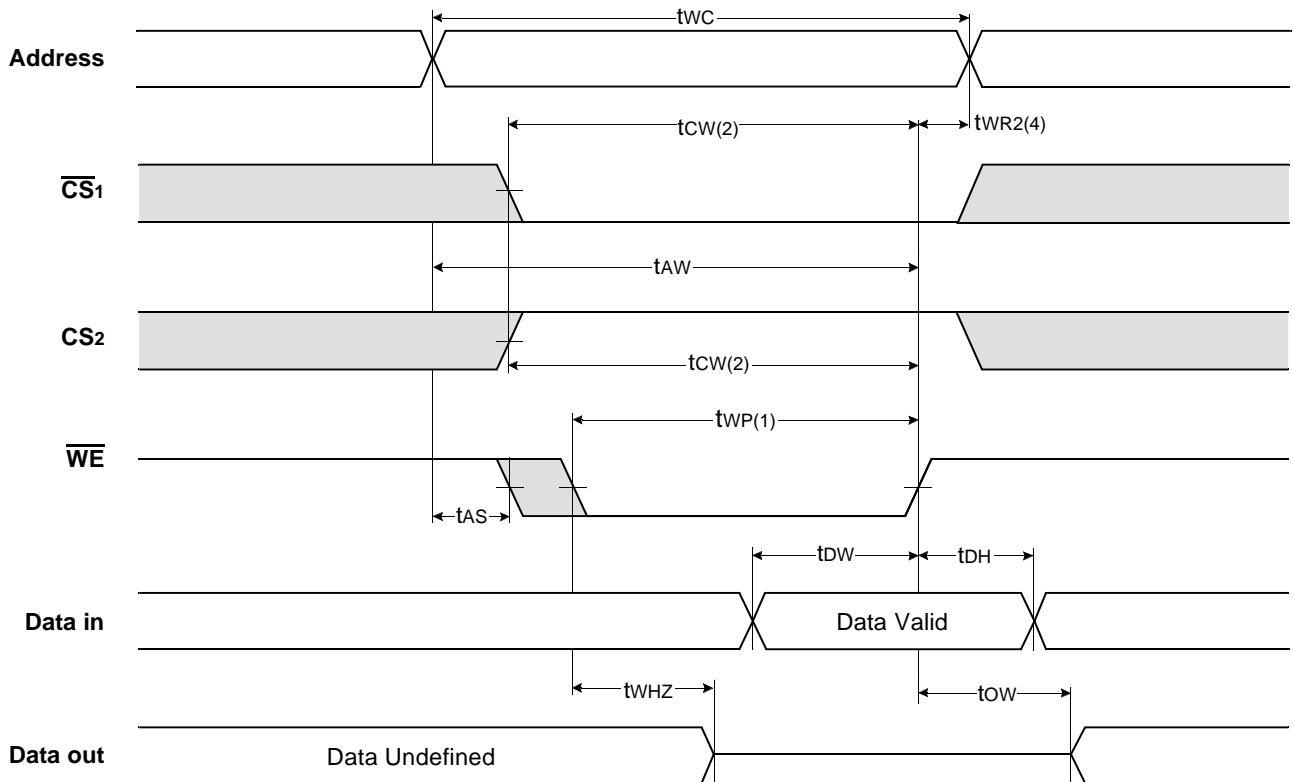
TIMING WAVEFORM OF READ CYCLE (2) ($\overline{WE}=V_{IH}$)



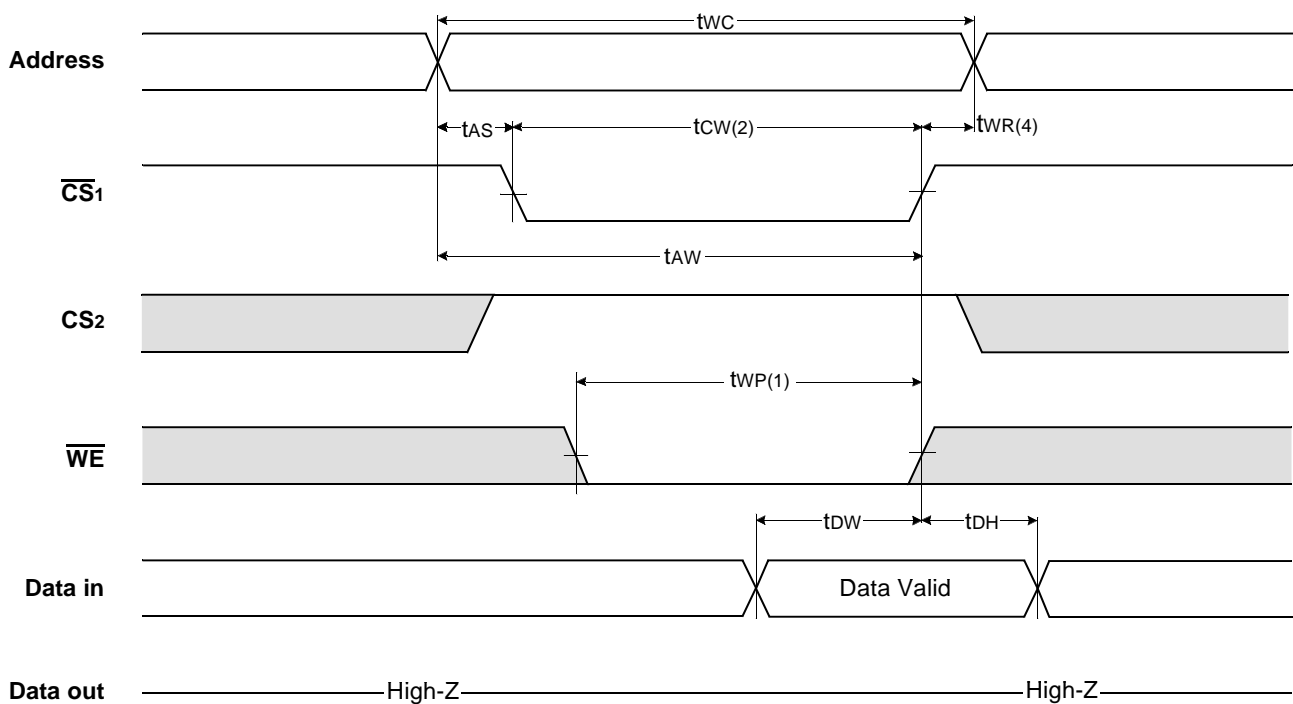
NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, $t_{HZ}(\text{Max.})$ is less than $t_{LZ}(\text{Min.})$ both for a given device and from device to device interconnection.

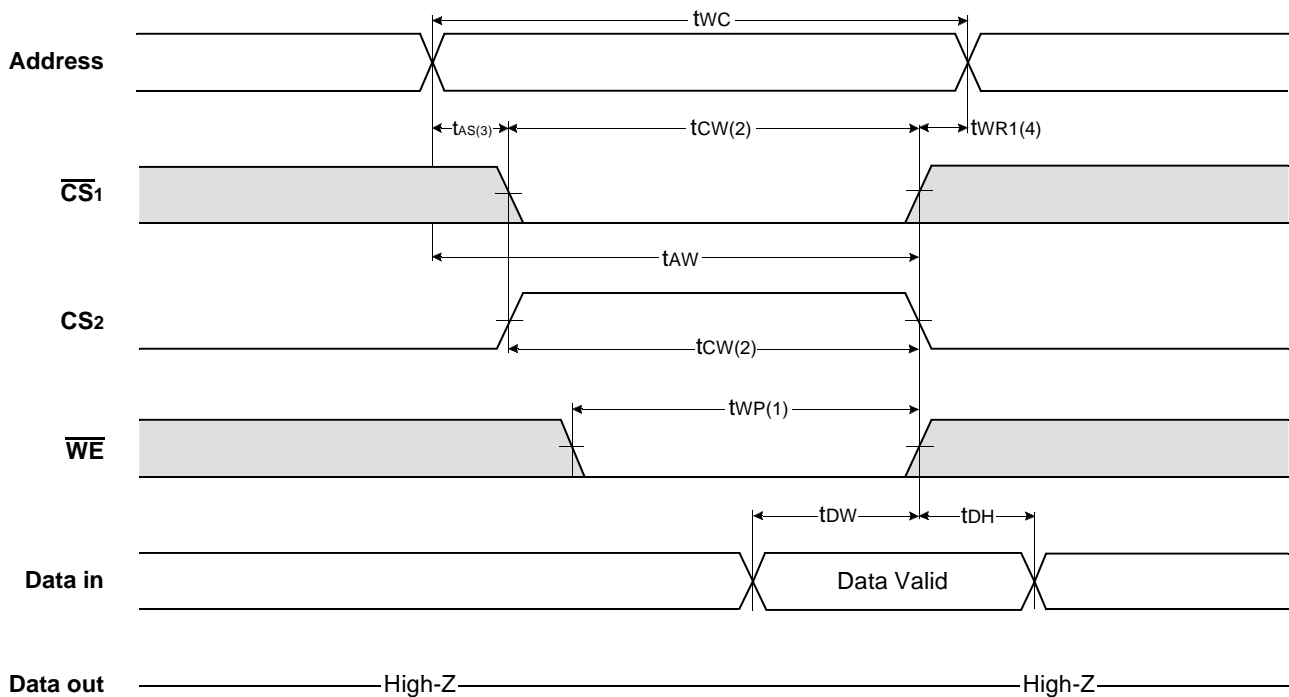
TIMING WAVEFORM OF WRITE CYCLE(1) \overline{WE} Controlled



TIMING WAVEFORM OF WRITE CYCLE(2) $\overline{CS1}$ Controlled



TIMING WAVEFORM OF WRITE CYCLE(3) (CS₂ Controlled)



NOTES (WRITE CYCLE)

1. A write occurs during the overlap of a low \overline{CS}_1 and a high CS₂ low \overline{WE} . A write begins at the latest transition among \overline{CS}_1 going low, CS₂ going high and \overline{WE} goes low. A write ends at the earliest transition among \overline{CS}_1 going high, CS₂ going low and \overline{WE} going high. t_{WP} is measured from the beginning of write to the end write.
2. t_{CW} is measured from the later of \overline{CS}_1 going low or CS₂ going high to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR1} applied in case a write ends at \overline{CS}_1 or \overline{WE} going high, t_{WR2} applied in case a write ends at CS₂ going to low.

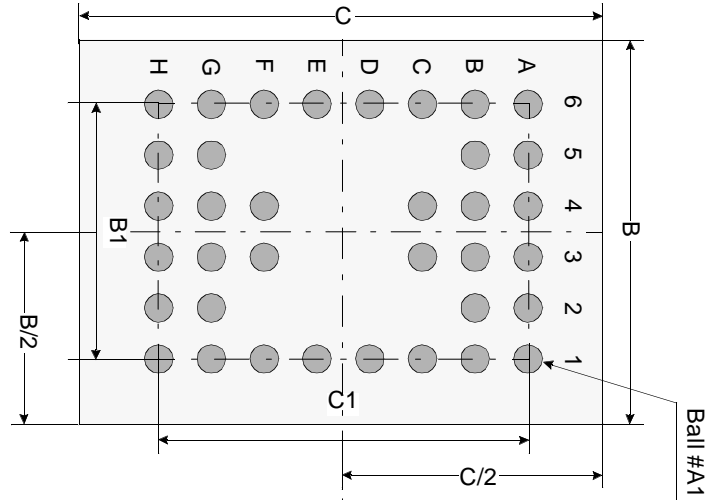
FUNCTIONAL DESCRIPTION

\overline{CS}_1	CS ₂	\overline{WE}	\overline{OE}	Mode	I/O _{1~8}	Current Mode
H	X*	X	X	Power Down	High-Z	ISB
X	L	X	X	Power Down	High-Z	ISB, ISB1
L	H	H	H	Output Disable	High-Z	I _{CC}
L	H	H	L	Read	Dout	I _{CC}
L	H	L	X	Write	Din	I _{CC}

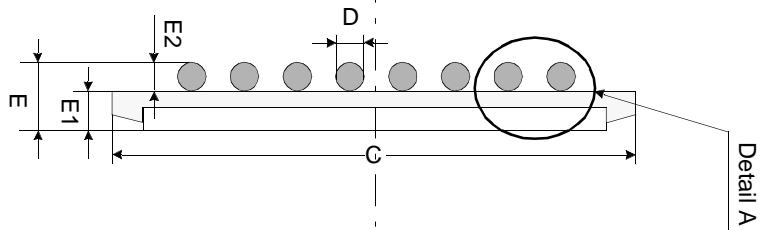
* X means do care (high or low)

PACKAGE DIMENSIONS (Units : mm)

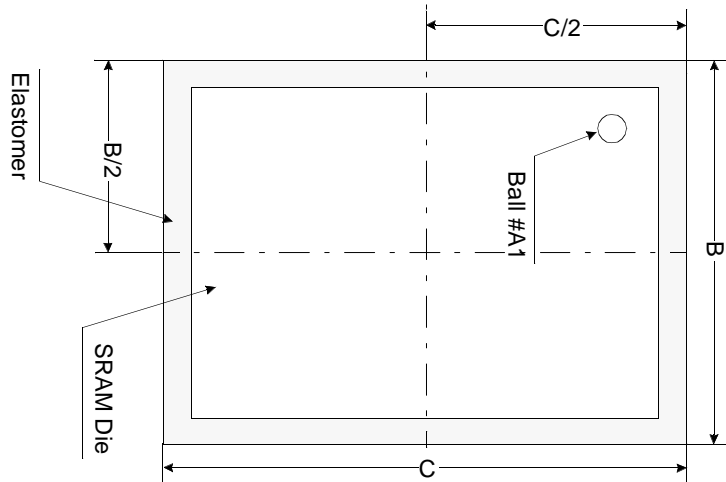
	Min	Typ	Max
A	-	0.75	-
B	5.90	6.00	6.10
B1	-	3.75	-
C	7.90	8.00	8.10
C1	-	5.25	-
D	0.30	0.35	0.40
E	-	0.80	0.81
E1	-	0.55	-
E2	-	0.25	-
Y	-	-	0.08



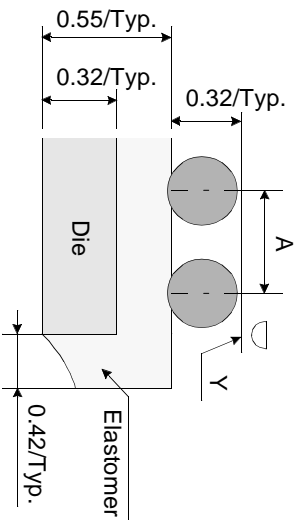
Bottom View



Side View



Top View



Detail A

- Notes:**
1. Bump counts : 48(8row x 6row)
 2. Bump pitch : (x,y)=(0.75 x 0.75)(typ.)
 3. All tolerance are +/-0.050 unless otherwise specified.
 4. Typ : Typical
 5. Y is coplanarity : 0.08(Max)