FM25040 FRAM® Serial Memory

*Product Preview**

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Features

- 4Kbit Nonvolatile Ferroelectric RAM Organized as 512 x 8
- Low Power CMOS Technology
  - 10µA Standby Over Industrial Temperature Range
  - 5µA Standby Over Commercial Temperature Range
- Reliable Thin Film Ferroelectric Technology
  - 10 Billion (10^{10}) Cycle Read/Write Endurance
  - 10 Year Data Retention
- High Performance
  - No Write Delay
  - Unlimited Sequential Write
- Simple Three Wire Bus
  - SPI Compatible (CPOL = 0, CPHA = 0)
  - 2.1MHz Maximum Clock Rate
- Multiple Levels of Write Protection
  - Hardware Write Protect Pin
  - Internal Write Enable Latch
  - Block Protect Bits
  - Low Voltage Lockout
- ESD Protection — Greater Than 2,000V On All Pins
- True 5V Only Operation
- 8-Pin Mini DIP and SOIC Packages
- -40° to +85°C Operating Range

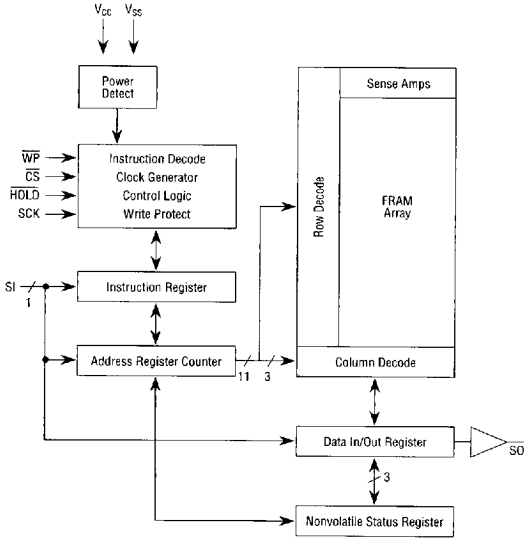
Description

Ramtron's FM25040 ferroelectric random access memory, or FRAM® memory provides nonvolatile data integrity in a compact package. A three wire serial interface provides access to any byte within the memory while reducing the cost of the processor interface (as compared to parallel access memories). The FM25040 is useful in a wide variety of applications for the storage of configuration information, user programmable data/features, and calibration data.

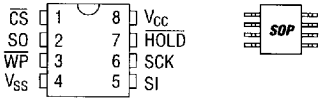
With Ramtron's ferroelectric technology, all writes are nonvolatile, eliminating long delays, extra page mode control, or high voltage pins. The technology is designed for highly reliable operation, offering extended endurance and 10 year data retention.

The FM25040 uses the industry standard three wire SPI protocol for serial chip communication. It is available in 300 mil mini-DIP and 150 mil SOP packages.

Functional Diagram



Pin Configurations



Pin Names

Pin Names	Function
$\overline{CS}$	Chip Select
SO	Serial Data Out
$\overline{WP}$	Write Protect
V_{SS}	Ground
SI	Serial Data In
SCK	Serial Clock
$\overline{HOLD}$	Hold Input
V_{CC}	Supply Voltage

*This document describes a product under development. Ramtron reserves the right to change or discontinue this product without notice.

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Absolute Maximum Ratings

Description	Ratings
Ambient Storage or Operating Temperature to Guarantee Nonvolatility of Stored Data	-40°C to +85°C
Voltage on Any Pin with Respect to Ground	-1.0 to +7.0V
D.C. Output Current	5mA
Lead Temperature (Soldering, 10 Seconds)	300°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only, and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Operating Conditions

T_A = -40°C to +85°C, V_{CC} = 5.0V ± 10%, Unless Otherwise Specified

Symbol	Parameter	Min	Typ(1)	Max	Units	Test Conditions
V_{CC}	Power Supply Voltage	4.5	5.0	5.5	V	
I_{CC}	V_{CC} Supply Current		1.0	1.5	mA	SCK @ 2.1MHz, Read or Write SCK CMOS Levels, All Other Inputs = V_{SS} or V_{CC} - 0.3V
I_{CC}	V_{CC} Supply Current		500	700	µA	SCK @ 1.0MHz, Read or Write SCK CMOS Levels, All Other Inputs = V_{SS} or V_{CC} - 0.3V
I_{SB}	Standby Current 0 to 70°C		1	5	µA	SCK = SI = V_{CC}, All Other Inputs = V_{SS} or V_{CC}
I_{SB}	Standby Current -40 to 85°C		1	10	µA	SCK = SI = V_{CC}, All Other Inputs = V_{SS} or V_{CC}
I_{LI}	Input Leakage Current			10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current			10	µA	V_{OUT} = V_{SS} to V_{CC}
V_{IL}	Input Low Voltage	-1.0		V_{CC} x 0.3	V	
V_{IH}	Input High Voltage	V_{CC} x 0.7		V_{CC} + 0.5	V	
V_{OL1}	Output Low Voltage			0.4	V	I_{OL} = 2mA
V_{OH}	Output High Voltage	V_{CC} - .8			V	I_{OH} = -1mA
V_{HYS}(2)	Input Hysteresis	V_{CC} x .05			V	

(1) Typical values at 25°C, 5.0V.
(2) This parameter is periodically sampled and not 100% tested.

Endurance and Data Retention

Parameter	Min	Max	Units
Endurance	10 Billion		R/W Cycles
Data Retention	10		Years

Power-Up Timing (3)

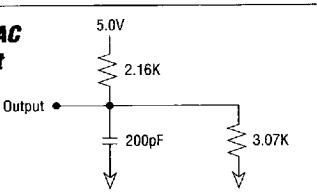
Symbol	Parameter	Max	Units
t_{PUR}(2)	Power Up to Read Operation	1	µs
t_{PUW}(2)	Power Up to Write Operation	1	µs

(3) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated. These parameters are periodically sampled and not 100% tested.

AC Conditions of Test

AC Conditions	Test
Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	10ns
Input and Output Timing Levels	V_{CC} x 0.5

Equivalent AC Load Circuit



Capacitance

T_A = 25°C, f = 1.0MHz, V_{CC} = 5V

Symbol	Test	Max	Units	Conditions
C_{OUT}(2)	Output Capacitance	8	pF	$V_{I/O}$ = 0V
C_{IN}(2)	Input Capacitance	6	pF	V_{IN} = 0V

(2) This parameter is periodically sampled and not 100% tested.

Pin Descriptions

Serial Output (SO)

This pin is active only during a read operation. The pin is high impedance at all other times and when /HOLD is low. During a read operation, this line is driven high or low depending on the current data output bit. Data is clocked out of the FM25040 on the falling edge of the serial clock.

Serial Input (SI)

Data is clocked into the FM25040 via this pin on the rising edge of the serial clock signal. Beyond the setup and hold times around this clock edge, the state on this pin is ignored. However, this pin should be driven to a valid logic level at all times to prevent excessive power dissipation.

Serial Clock (SCK)

Information is clocked into or out of the FM25040 using this pin when /CS is low and /HOLD is high. Input values are latched on the rising edge, while data output changes occur after the falling edge of this signal. The maximum clock rate is 2.1MHz. The FM25040 is a completely static design, so clocking may be interrupted at any point in time, or the clock rate may be arbitrarily slow.

Chip Select (/CS)

When this signal is low, the FM25040 will respond to transitions on the SCK signal. When it is high, inputs are ignored, outputs are placed in a high impedance state, and the FM25040 goes into its low power standby mode. A high to low transition is required on this pin before each opcode.

Write Protect (/WP)

If held low, this pin will inhibit all write operations within the part, regardless of the state of the internal write enable latch. If held high, writes are permitted only if the internal write enable latch is set. Read operations always proceed normally, regardless of the state of this pin.

Hold (/HOLD)

/HOLD may be used to pause the sequence if the CPU must process some other event in the middle of an operation. While /HOLD is low, the FM25040 will ignore any transitions on the SCK and /CS pins. When /HOLD is high, all operations will proceed normally. Transitions on the /HOLD pin must occur while SCK is low.

Device Operation

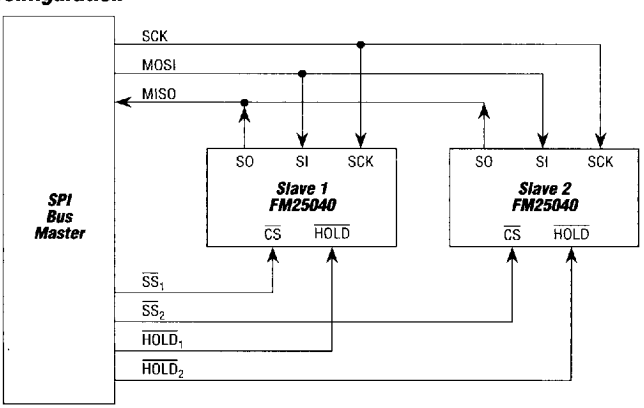
The FM25040 is a serial ferroelectric memory designed to interface easily with the Serial Peripheral Interface (SPI) port common to many MC6805 and MC68HC11 processors. The SPI communications channel uses three wires (clock, serial data in, and serial data out) that can be shared among a number of devices. Additionally, a fourth pin (chip select) selects the device on the time multiplexed bus that should respond to the access request. A typical system configuration is shown in Figure 1.

Data is transferred to and from the FM25040 in bytes of eight bits each, governed by edges on the SCK signal. Data is transferred with the most significant bit (MSB) first. For any operation the first byte to be transferred is the operation code (opcode) which determines what is to be performed by the memory. There are six operations that may be performed by the FM25040. Table 1 lists the operation with its corresponding opcode.

Table 1. Opcode Commands

Opcode	Description	Name
0000 0110	Set Write Enable Latch	WREN
0000 0100	Write Disable	WRDI
0000 0101	Read Status Register	RDSR
0000 0001	Write Status Register	WRSR
0000 A011	Read Data	READ
0000 A010	Write Data	WRITE

Figure 1. Typical System Configuration



Master Acronym Definitions
MOSI: Master Out Slave In
MISO: Master In Slave Out
SS: Slave Select

Status Register

Table 2 shows the organization of the status register. The register is read using the RDSR instruction. Bits 0 and 4 through 7 are unused. When read, they return a 0. The value of the status register is transmitted directly after the RDSR opcode. Executing of the RDSR instruction has no effect on the status register bits. (This is unlike the WRSR instruction which clears the Write Enable Latch [WEL] bit.)

Bit 1 is the WEL. When set, writes may take place to the part. When reset, all writes will be ignored.

Bits 2 and 3 are nonvolatile block protect bits (BP0 and BP1). These bits provide further protection to portions of the array as specified in Table 3. Note that bytes within blocks that are *not* protected with BP0 and BP1 will still only be written if the write enable latch is set.

Writing to the status register is a two step process:

i) The WEL bit must be set to enable a write. This is done using the WREN instruction.

ii) The WRSR instruction is then used to change the block protect bits. Note that execution of the WRSR instruction clears the WEL bit.

Table 2. Status Register Organization

Bit	7	6	5	4	3	2	1	0
Name	0	0	0	0	BP1	BP0	WEL	0

Table 3. Memory Block Protect Bits

BP1	BP0	Protected Address Range (Hex)
0	0	None
0	1	180 → 1FF (upper 1/4 of the array)
1	0	100 → 1FF (upper 1/2 of the array)
1	1	000 → 1FF (all of the array)

Write Enable Latch

The internal write enable latch on the FM25040 prevents writes to the data within the part while it is cleared. /WEL = 0 protects the nonvolatile memory array *and* the status register bits. When set to a 1, writes proceed normally. It is automatically cleared on power up or whenever the power supply falls below 3.5V (typical). It is also cleared after all write operations (including WRSR) and cleared whenever /WP is brought low. Note that /WP going low asynchronously clears the WEL bit regardless of the status of the /HOLD pin.

The user can set or reset this bit by transmitting the corresponding opcode to the FM25040 (WREN or WRDI, respectively). No address or data bytes follow the opcode. Note that following the write enable latch instruction (WREN), chip select must rise again before a write sequence may be started. The FM25040 will ignore all bits transmitted after the opcode but before the rise of /CS.

Read and Write Sequences

For a read or write operation, an address byte must be transmitted to the FM25040 after the opcode. Bit 3 of the opcode is address bit A_8. Following the address byte, data bytes should be transferred MSB first. Any number of bytes may be read or written in sequential order starting with the specified address, and wrapping around to address 0 after the byte at address 1FF (hex) is accessed. The read or write sequence continues until /CS is brought high.

Note that on the FRAM device, any number of bytes may be written with a single write sequence, while EEPROM based 25040 devices are limited to one through four bytes only. To accommodate this feature, the actual write to the nonvolatile array takes place after the eighth bit in each byte is transmitted. If /CS rises during a write operation, only the byte that has not been completely transmitted will be ignored.

Low Voltage Protection

When powering up, the FM25040 will automatically perform an internal reset and await a high to low transition on /CS from the bus master. The bus master should wait T_{PUR} (or T_{PUW}) after V_{CC} reaches 4.5V before selecting the part. Additionally, whenever V_{CC} falls below 3.5V (typical), the part goes into its low voltage protection mode. In this mode, all accesses to the part are inhibited and the part performs an internal reset. If an access was in progress when the power supply fails, it will be automatically aborted by the FM25040.

Serial Data Output Timing

Serial output timing is shown in Figure 2. Data is placed by the FM25040 on it serial output pin (SO) t_{ODV} seconds after the falling edge of SCK. The clock frequency is arbitrary with a maximum clock rate of 2.1MHz. This is the timing sequence that applies to the reading of the status register bits and nonvolatile memory.

Serial Data Output Timing Parameters(4,5)

Symbol	Parameter	Min	Max	Units
f_{CK}	Clock Frequency	0	2.1	MHz
t_{CH}	Clock High Time	190		ns
t_{CL}	Clock Low Time	190		ns
t_{CSL}	Chip Select Lag Time	240		ns
t_{OD}	Output Disable Time		240	ns
t_{ODV}	Output Data Valid Time		240	ns
t_{OH}	Output Hold Time	0		ns

(4) T_A = -40°C to +85°C, V_{CC} = 5.0V ±10%, Unless Otherwise Specified
(5) Switching Times Measured from 50% VCC to 50% VCC, Unless Otherwise Specified

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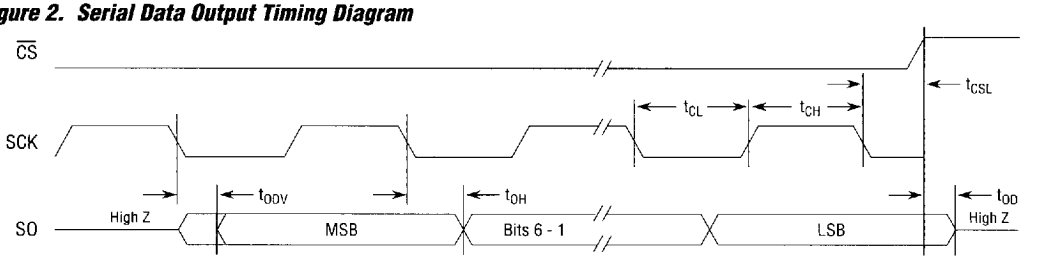
Figure 2. Serial Data Output Timing Diagram



Serial Data Input Timing

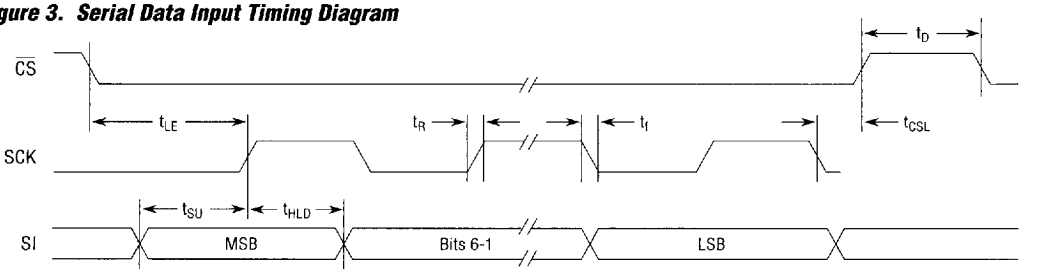
Serial input timing is shown in Figure 3. Input data is latched on the rising edge of SCK. The data bit must be valid t_{SU} seconds before this rising edge. In addition, data must be held t_{HLD} seconds after this rising edge. This is the timing sequence that applies to the clocking of all opcodes, addresses, and data to be written to the status register and memory.

Serial Data Input Timing Parameters(4)

Symbol	Parameter	Min	Max	Units
t_D	Deselect Time	240		ns
t_F(6)	Data Fall Time		2.0	µs
t_{HLD}	Data Hold Time	100		ns
t_{LE}	Chip Select Lead Time	240		ns
t_R(6)	Data Rise Time		2.0	µs
t_{SU}	Data Setup Time	100		ns

(4) T_A = -40°C to +85°C, V_{CC} = 5.0V ±10%, Unless Otherwise Specified
(6) Rise and Fall Times Measured Between 10% and 90% Points of Waveform

Figure 3. Serial Data Input Timing Diagram



Hold Timing

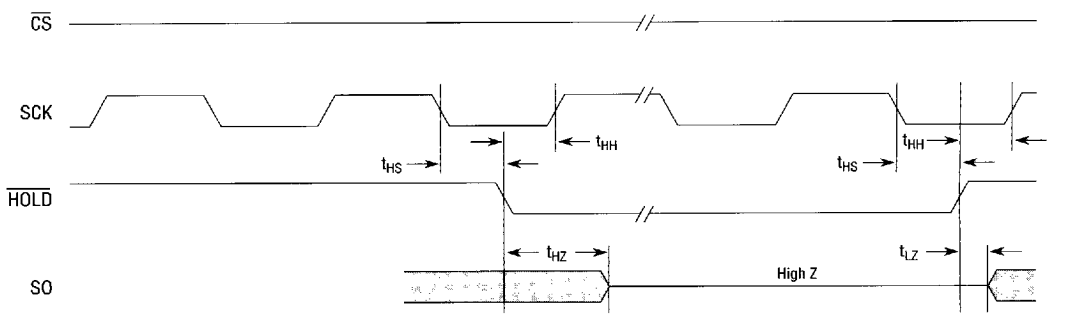
Hold timing is shown in Figure 4. Hold is used to pause a timing sequence to allow the processor to service a higher priority task. Note that /CS and SCK must be low during transitions of the /HOLD signal.

Hold Timing Parameters(4)

Symbol	Parameter	Min	Max	Units
t_{HH}	Hold Hold Time	90		ns
t_{HS}	Hold Setup Time	90		ns
t_{HZ}	$\overline{HOLD}$ Low to High Z		100	ns
t_{LZ}	$\overline{HOLD}$ High to Low Z		100	ns

(4) T_A = -40°C to +85°C, V_{CC} = 5.0V ±10%, Unless Otherwise Specified

Figure 4. Hold Timing Diagram



Read Protocol

The detailed read protocol is shown in Figure 5. The sequence is as follows:

i) The master initiates the sequence by pulling /CS low.

ii) The very next rising edge of SCK begins the input clocking of the opcode into the FM25040.

iii) The eight bit opcode is clocked into the FM25040. Note that bit 3 is address bit A_8.

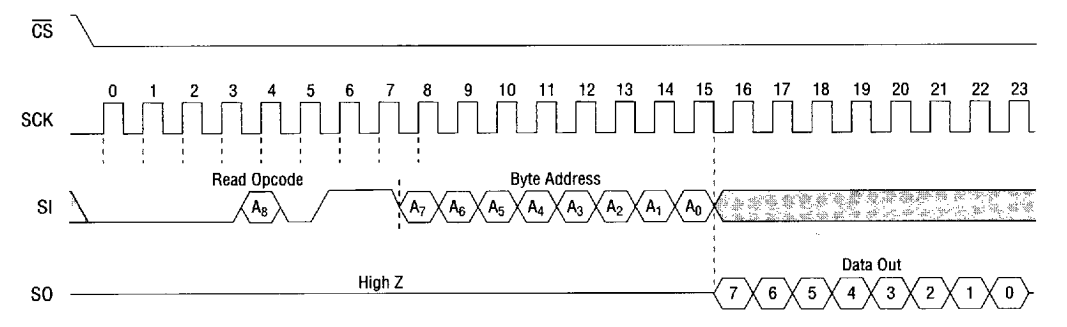
iv) The byte address (A_7 through A_0) follows immediately.

v) The data is shifted out of the FM25040 (on SO) immediately following the byte address using the falling edge of SCK.

vi) Data can be continuously shifted out of the FM25040 by continually supplying clock pulses. When the highest byte address is read, the address counter wraps to zero and reading continues.

vii) The master terminates the read by taking /CS high.

Figure 5. Read Sequence



Write Protocol

The detailed write protocol is shown in Figures 6 and 7. The sequence is as follows:

i) The master must enable writes to the FM25040 by issuing the WREN instruction as shown in Figure 6. Note that /CS must be taken high after the LSB of the WREN instruction is transmitted from the master to the FM25040.

ii) The master writes the write opcode, byte address, and any number of sequential bytes to the FM25040 as shown in Figure 7. Again, the operation must be terminated by taking /CS high after the LSB in the last byte.

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Figure 6. WREN Instruction

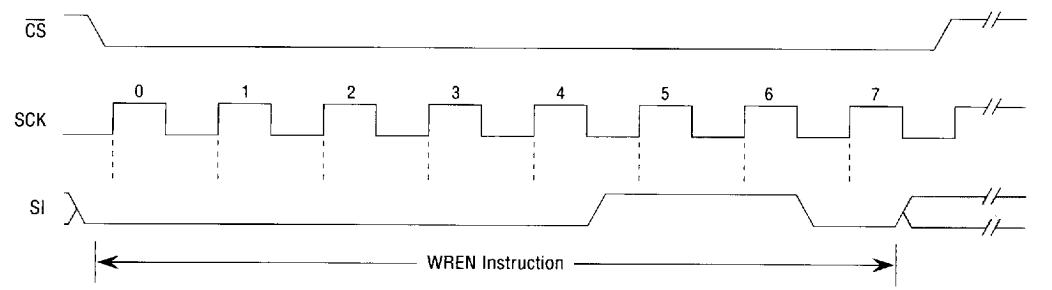
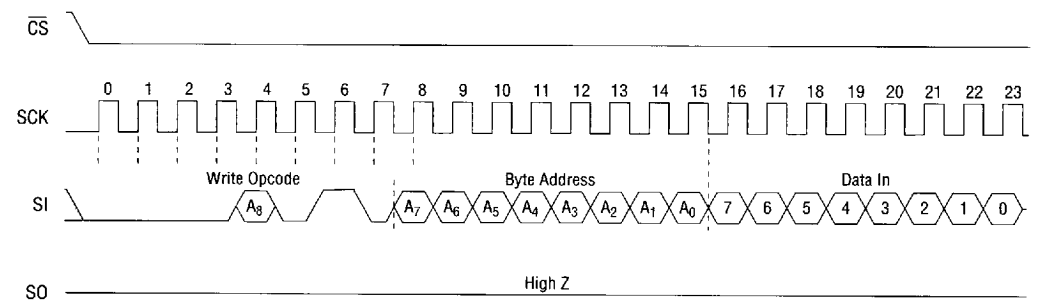
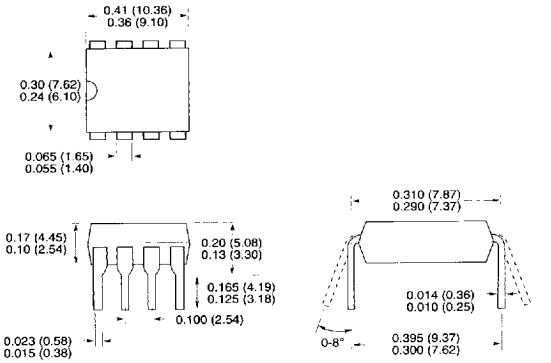


Figure 7. Write Sequence

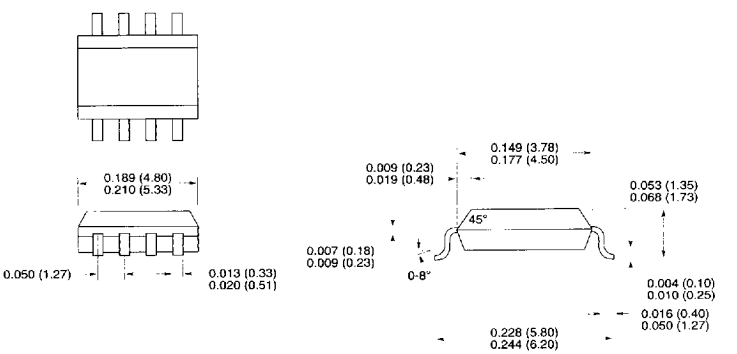


Packaging Information

8-Pin Plastic or Ceramic DIP



8-Pin SO (JEDEC)



Ordering Information

FM 25040 - PS

Package Type (8-Pin)
PS - Plastic Skinny DIP
PT - Thin Plastic Skinny DIP
S - Plastic SOP
C - CERDIP

4K Serial FRAM Memory

Ramtron Ferroelectric Memory