Am95C60

Quad Pixel Dataflow Manager

PRELIMINARY

DISTINCTIVE CHARACTERISTICS

- Generates mixed text and graphics within Display Memory
- Draws vectors up to 3.3 million pixels per second, or places text at 50,000 characters per second
- One chip handles four Display Memory planes of any size up to 4K x 4K bits and screen sizes to 2K x 2K pixels
- Capable of cascading to handle multiple memory planes without system performance degradation
- Reflects GKS, CGI, and NAPLPS software standards
- Supports windowing, panning, and scrolling
- Supports drawing of anti-aliased vectors, circles, and arcs with various user-definable line styles
- Fills arbitrary polygons
- Supports dual-port video DRAMs
- CMOS technology
- Provides memory and video refresh at user-definable rates
- Interfaces to any 8- or 16-bit system bus
- Comprehensive instruction set

GENERAL DESCRIPTION

The Am95C60 Quad Pixel Dataflow Manager (QPDM) is a CMOS graphics processor which contains the necessary circuitry and control functions for driving four bit-mapped memory arrays. Featuring a maximum system clock speed of 20 MHz, the Am95C60 can interface to any 8- or 16-bit system bus and can draw vectors up to 3.3 million pixels per second, or place text at a rate of 50,000 characters per second. Such performance allows the user to efficiently mix text and graphics within the bit map. The Am95C60 QPDM also contains graphics primitives which smoothly interface with the GKS, CGI, and NAPLPS software standards.

The Am95C60 interfaces directly to memory planes consisting of dual-port video dynamic memories (VRAMs) and is capable of supporting four planes up to 4K by 4K bits and display screens up to 2K by 2K pixels. The Am95C60 is fully cascadable and can manage up to 256 memory planes with no system performance degradation.

The Am95C60 QPDM provides support for the drawing of anti-aliased vectors, circles, and arcs with various user-defined linestyles. Other features include windowing, independent X and Y zoom factors, pan and scroll, picking, clipping, and logical PEL. The Am95C60 is packaged in a 145-lead Pin Grid Array (PGA), and a 160-pin Plastic Quad Flatpack (PQFP).

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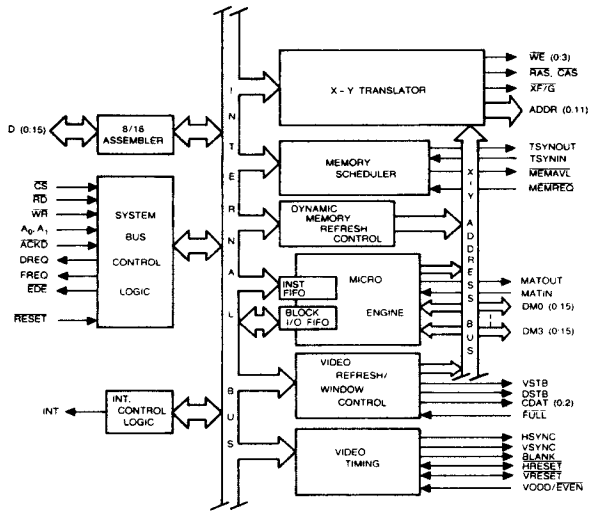
BLOCK DIAGRAM



BD005863

Publication #	Rev.	Amendment
07013	C	/0

Issue Date: October 1988

CONNECTION DIAGRAMS

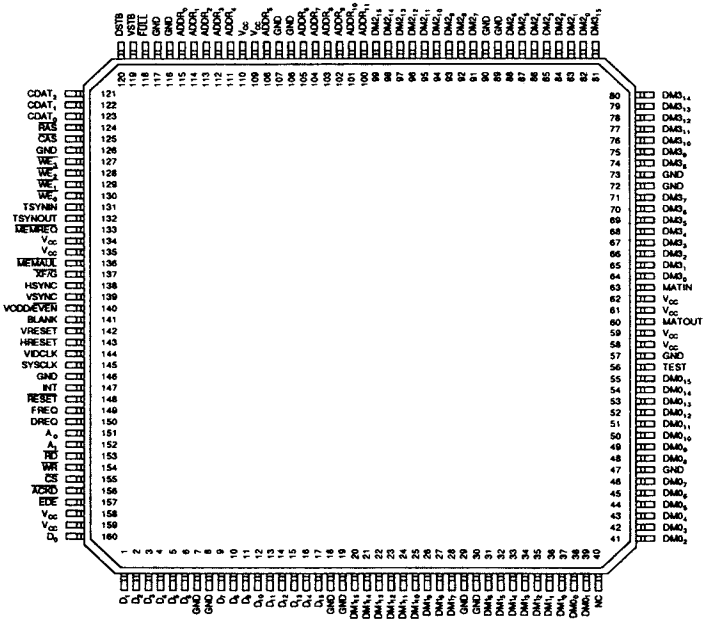
PGA

(Pins Facing Up)

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	
1	$DM3_{14}$	$DM3_{13}$	$DM3_{11}$	$DM3_{10}$	$DM3_7$	$DM3_5$	$DM3_3$	$DM3_1$	TEST	$DM0_{12}$	$DM0_{10}$	$DM0_9$	$DM0_7$	$DM0_5$	$DM0_1$	1
2	$DM2_0$	$DM3_{15}$	$DM3_{12}$	$DM3_8$	$DM3_4$	$DM3_2$	$DM3_0$	MATOUT	$DM0_{14}$	$DM0_{13}$	$DM0_{11}$	$DM0_8$	$DM0_2$	$DM0_3$	$DM0_0$	2
3	$DM2_2$	$DM2_4$	$DM2_1$	$DM3_9$	GND	$DM3_6$	V_{CC}	MATIN	V_{CC}	$DM0_{15}$	GND	$DM0_6$	$DM0_4$	$DM1_4$	$DM1_0$	3
4	$DM2_6$	$DM2_7$	$DM2_5$	NC									$DM1_1$	$DM1_3$	$DM1_2$	4
5	$DM2_9$	$DM2_{11}$	$DM2_3$										$DM1_7$	$DM1_6$	$DM1_5$	5
6	$DM2_{13}$	$DM2_8$	GND										GND	$DM1_8$	$DM1_9$	6
7	$DM2_{15}$	$DM2_{12}$	$DM2_{10}$										$DM1_{14}$	$DM1_{10}$	$DM1_{11}$	7
8	$DM2_{14}$	$ADDR_{10}$	$ADDR_{11}$										$DM1_{12}$	$DM1_{13}$	$DM1_{15}$	8
9	$ADDR_8$	$ADDR_9$	GND										GND	D_{14}	D_{15}	9
10	$ADDR_6$	$ADDR_5$	V_{CC}										D_{13}	D_{12}	D_{11}	10
11	$ADDR_4$	$ADDR_7$	$ADDR_1$										GND	D_{10}	D_9	11
12	$ADDR_3$	$ADDR_2$	GND										D_8	D_7	D_6	12
13	$\overline{FULL}$	$ADDR_0$	$\overline{RAS}$	$\overline{WE_0}$	$\overline{CAS}$	$\overline{XF/G}$	V_{CC}	VODD/$\overline{EVEN}$	DREQ	INT	V_{CC}	$\overline{WR}$	D_5	D_3	D_4	13
14	VSTB	$CDAT_2$	$CDAT_0$	$\overline{WE_1}$	TSYNIN	$\overline{MEMAVL}$	VSYNC	BLANK	$\overline{HRESET}$	SYSCLK	$\overline{RESET}$	$\overline{RD}$	$\overline{ACKD}$	D_1	D_2	14
15	DSTB	$CDAT_1$	$\overline{WE_3}$	$\overline{WE_2}$	TSYNOUT	$\overline{MEMREQ}$	HSYNC	$\overline{VRESET}$	VIDCLK	FREQ	A_0	A_1	$\overline{CS}$	$\overline{EDE}$	D_0	15
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	

Flatpack

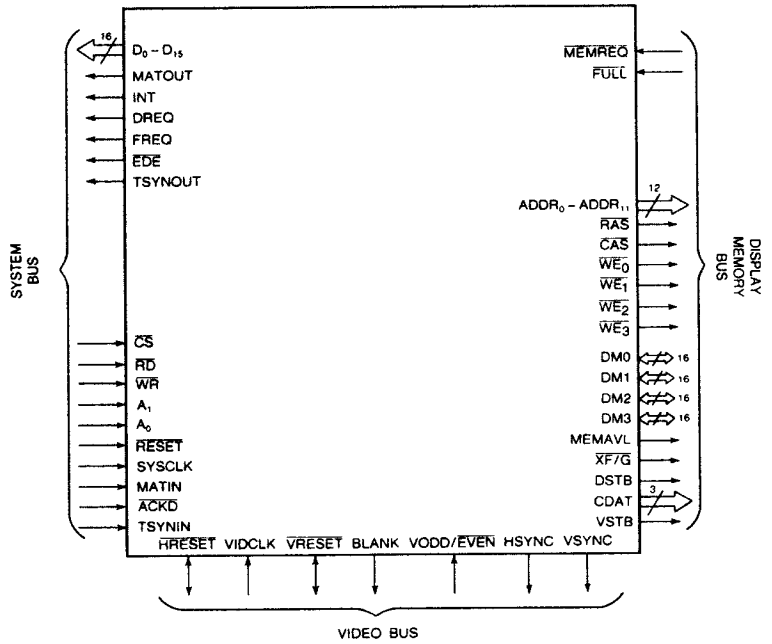
(Top View)



07013-007A

CD011720

LOGIC SYMBOL



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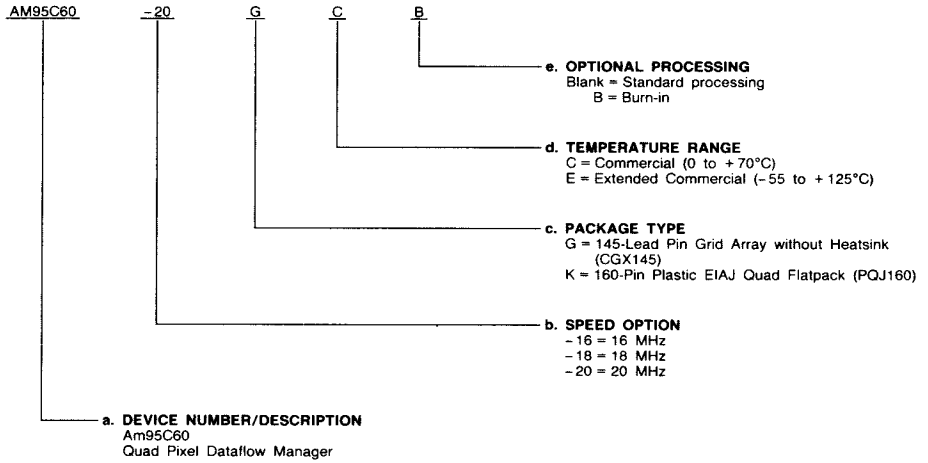
ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM95C60-16	GC, GCB, GE, GEB, KC
AM95C60-18	
AM95C60-20	

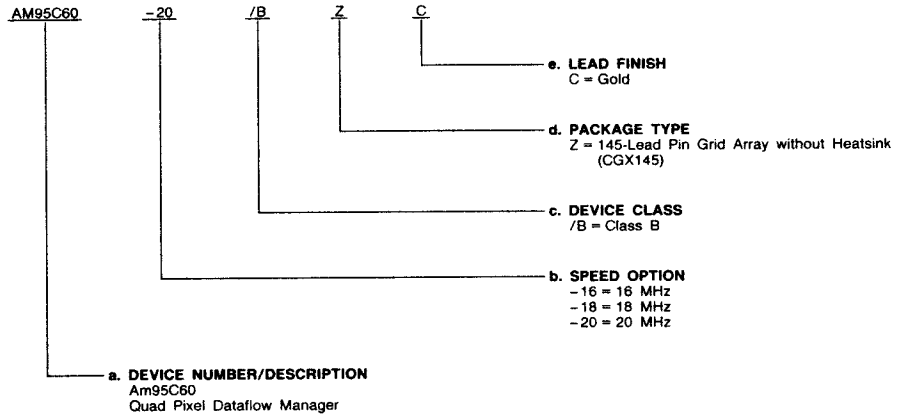
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defence applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish



Valid Combinations	
AM95C60-16	/BZC
AM95C60-18	
AM95C60-20	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

PIN DESCRIPTION

The Am95C60 interfaces through three buses: the System Bus, the Display Memory Bus, and the Video Bus.

System Bus

A_0, A_1 Port Address (Input)
These two inputs are used for selecting the appropriate port to be read or written.

$\overline{ACKD}$ Acknowledge DMA (Input; Active LOW)
The external DMA device may drive this pin LOW in response to a DMA request to strobe in or read out data in fly-by DMA transfer format.

$\overline{CS}$ Chip Select (Input; Active LOW)
Signal used for selecting the Am95C60 from several peripherals connected to the same system bus.

D(0:15) Command/Data/Status (Input/Output; Three-State)
These sixteen lines are used for transferring commands/data/status on the System Bus. The nature of the information transferred on the D(0:15) lines is specified with the port address pins A_0, A_1.

DREQ Data FIFO Request (Output; Open Drain)
Signal used to start and suspend a transfer of data between the System Memory and the Display Memory.

$\overline{EDE}$ External Driver Enable (Output; Active LOW)
This pin is used to enable external data bus drivers on the system bus. $\overline{EDE}$ is inactive (HIGH) during an output block operation on those Am95C60 devices that do not participate in the output. This signal eliminates contention on the system bus.

FREQ Instruction FIFO request (Output; Open Drain)
This signal is used to start and suspend a transfer of instructions from the system memory into the QPDM instruction FIFO.

INT Interrupt (Output; Active HIGH)
High-level interrupt output used to signal that an exception has occurred. The nature of the exception can be determined by reading the Status register.

MATIN Match In (Input, Active HIGH)
This pin is connected to the output of the AND gate connected to the MATOUT outputs.

MATOUT Match Out (Output; Active HIGH)
This pin is used in multiple-QPDM applications to search for a matching color pattern. As long as the pattern is not found, this pin stays LOW. When the matching pattern is found the pin is driven HIGH. Since all the MATOUT outputs are logically ANDed externally, a match in a multiple-QPDM environment is visible on MATIN when all the MATOUT outputs are HIGH. This pin is also used for instruction-execution synchronization by re-aligning the Am95C60 devices in a system at the beginning of each instruction execution and at the beginning of each word transfer in Block I/O instruction.

$\overline{RD}$ Read (Input; Active LOW)
Signal used for reading information (data/status) from the Am95C60 QPDM on the D(0:15) lines by a bus master.

$\overline{RESET}$ System Reset (Input; Active LOW)
The $\overline{RESET}$ signal brings all Am95C60s in the system to the same initial state. All the outputs are brought into the inactive state. If $\overline{RESET}$ is activated during the time when the Am95C60 was active, all the activities will be suspended.

SYSCLK System Clock (Input)
20 MHz maximum frequency clock. Controls the Am95C60 QPDM internal timing except for video timing.

TSYNIN Timing Synchronization (Input; Active HIGH)
All TSYNIN input pins are connected to the AND of the TSYNOUT.

TSYNOUT Timing Synchronization (Output, Active HIGH)
In conjunction with TSYNIN, this pin is used to synchronize Display Memory Bus activities. The TSYNOUT pins of all Am95C60 devices in a system are ANDed together and connected to the TSYNIN input pins of all Am95C60s. User-transparent information signals all Am95C60 devices about Display Memory Bus activities.

$\overline{WR}$ Write (Input; Active LOW)
Signal used for strobing information (commands/data) into the Am95C60 from the D(0:15) lines.

Display Memory Bus

ADDR(0:11) Address (Output)
The twelve lines of address are used for addressing bit-map planes each up to 4K x 4K bits. The addresses are multiplexed and contain row and column addresses and bank-select bits.

$\overline{CAS}$ Column Address Strobe (Output; Active LOW)
This line is used to strobe the column address from the multiplexed ADDR lines into the array.

DM0-3(0:15) Display Memory Bus (Input/Output)
These 64 lines are used for transferring data between the Am95C60 and the Display Memory. There are sixteen lines for each of the four planes.

$\overline{MEMAVL}$ Memory Bus Available (Output; Active LOW)
This line is used to inform external devices that are requesting the bus that the Am95C60 is not driving the data lines.

$\overline{MEMREQ}$ Memory Request (Input; Active LOW)
This asynchronous signal is used by an external device to request access to the Display Memory Bus.

$\overline{RAS}$ Row Address Strobe (Output; Active LOW)
This line is used to strobe the Row address from the multiplexed ADDR lines into the array.

$\overline{WE}$(0:3) Write Enable (Output; Active LOW)
The $\overline{Write\ Enable}$, when active, signifies that the current transaction on the Display Memory Bus is a write to the corresponding bit plane.

$\overline{XF/G}$ Transfer/Output Enable (Output; Active LOW)
This pin interfaces directly to the video DRAM. During a transfer cycle this pin indicates a transfer to the video DRAMs. During a random read cycle, this pin enables the output buffer of the video DRAMs.

Video Control Bus

BLANK Blank Video (Output; Active HIGH)
BLANK is an active HIGH output which serves to blank out inactive display areas of the CRT. This output is held HIGH when the Am95C60 is reset.

CDAT(0:2) Control Data (Output; Active HIGH)
These lines are used to output 3 bits of information to the VDAF. Information is sent to the VDAF during the transfer cycle and at VSTB time.

DSTB Data Strobe (Output; Active HIGH)
This clock signal loads 8 bits of video data into the VDAF. DSTB is synchronous with SYSCLK and has twice the frequency of VSTB.

$\overline{\text{FULL}}$ $\overline{\text{Full}}$ (Input; Active LOW)
This input alerts the Am95C60 that the VDAF cannot accept more video data. If the $\overline{\text{FULL}}$ signal is active, the Am95C60 stops generating the VSTB and DSTB signals.

$\overline{\text{HRESET}}$ $\overline{\text{Horizontal Reset}}$ (Input/Output; Active LOW)
This pin is an output for horizontal video masters, and an input for horizontal video slaves. It is used for vertical video synchronization to other Am95C60s or to an external video source.

HSYNC Horizontal Sync (Output; Active HIGH)
HSYNC is an active HIGH output which causes horizontal retrace of the CRT's electron beam. This output is held LOW when the Am95C60 is reset to prevent any uncontrolled synchronization to the CRT, which may cause damage to the tube.

VIDCLK Video Clock (Input)
15 MHz maximum frequency clock used for generating video synchronization signals.

VODD/$\overline{\text{EVEN}}$ Vertical Odd/$\overline{\text{Even}}$ (Input)
This input is optionally used in the interlaced Display mode to distinguish between the even frame and the odd frame specified by an external device.

VSTB Video Strobe (Output, Active HIGH)
This strobe signal is used in a system with video dynamic RAMs (VRAMs) and an external VDAF (Am8171/8172 Video Data Assembly FIFO or a similar circuit built of discrete components) to shift video data out of the Video Memory. With every strobe, a 16-bit-wide word is shifted out of the Video Memory.

VSYNC Vertical Sync (Output; Active HIGH)
VSYNC is an active HIGH output which causes vertical retrace of the CRT's electron beam. This output is held LOW when the Am95C60 is reset.

$\overline{\text{VRESET}}$ $\overline{\text{Vertical Reset}}$ (Input/Output; Active LOW)
This pin is an output for vertical video masters and an input for vertical video slaves. It is used for vertical video synchronization to other Am95C60 devices or to an external video source.

Power Connections

GND Ground
Each GND pin must be connected to the power supply ground.

TEST Test
This pin may be grounded or it may be pulled up to V_{CC}; it must not be allowed to float. This pin for factory test purposes only.

V_{CC} Power Supply
Each V_{CC} must be connected to a +5-V power supply.

FUNCTIONAL DESCRIPTION

The Am95C60 Quad Pixel Dataflow Manager is a graphics processor which maintains, updates, and displays information in four bit-mapped video planes. As depicted in Figure 1, the System Interface communicates with either an 8- or 16-bit host CPU while the Display Memory Interface controls four bit-mapped memory planes. These planes consist of dual-port video dynamic memories (VRAMs). The Am95C60 connects to the random ports while the serial ports are used to access video information for the screen refresh. When used in conjuction with the Am8172 Video Data Assembly FIFO, the Am95C60 is capable of displaying a hardware window with the associated features of smooth pan and soft scroll.

The Am95C60 QPDM performs three fundamental functions described below:

Video Refresh

The Am95C60 QPDM manages the screen (display) refresh function by generating the addresses to the bit-map VRAMs as required to access data for display on the screen. The data from the VRAMs are serialized externally to the Am95C60.

The Video Refresh operation is fully programmable, allowing the user to tailor the system as required. The screen display can be aligned on any pixel boundary and can also include one hardware window overlay. Additionally, the total video process can be externally synchronized to any external source at the horizontal or vertical synchronization rate. Video Refresh can be disabled for operation as a slave device.

Dynamic Memory Refresh

The Am95C60 performs the Dynamic Memory Refresh function for the Display Memory. The Dynamic Memory Refresh process is interleaved with the Video Refresh and with the Display Memory updating. The refresh rate is programmed by loading the 10-bit Dynamic Memory Refresh Rate register. This register holds the number of SYSCLK cycles between two refresh cycles.

The Dynamic Memory Refresh Rate register is loaded into a counter, which is down-counted by the SYSCLK. When the counter reaches its zero state, it sends a refresh request to the Memory Scheduler. As soon as the Memory Scheduler arbitrates a time slice for the Dynamic Memory Refresh block, a refresh cycle is initiated.

The Am95C60 executes $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycles.

Display Memory Update

The Am95C60 has access to the Display Memory Bus for updating purposes, except when it is performing Video or Dynamic Memory Refresh.

Placing an instruction in the execution FIFO (see Block Diagram) signals the Micro Engine to begin operation. If the execution of the instruction requires access to the Display Memory Bus (this is the case in most instructions), the Am95C60 continues the instruction execution unless the Display Memory Bus is occupied by the Video Refresh or the Dynamic Memory Refresh process. If the Display Memory Bus cannot be accessed momentarily, the execution is suspended until the Display Memory is available.

The drawing instruction set includes Line, Circle, Filled Triangle, String and many others which will be briefly described in the following pages.

Feature Description

Window Display Mechanism

The Am95C60 QPDM, in conjunction with the Am8172 Video Data Assembly FIFO (VDAF) or the equivalent, can support a single non-destructive hardware window. The image to appear in the window is located in some other area of Display Memory than that visible on the screen (this is shown in Figure 2). The size and position of the window is programmed into a set of registers on the Am95C60. Since the window position is dynamically programmable, it is easy to 'drag' a rectangular area containing an object. It is also easy to perform soft scrolling and smooth panning of either background or foreground.

Clipping

The clipping feature on the Am95C60 allows a rectangular region to be defined outside of which vectors and arcs will not be drawn, blocks will not be moved or modified, and polygons will not be filled. The clipping window is specified by the user, and remains in effect until changed or disabled.

Picking

If a drawing consists of a large number of objects and each object is defined by a number of drawing primitives, any object can be identified by the following picking process.

First, the picking area is defined as a rectangular region in Display Memory. Whenever a drawing intersects the picking area, a 'Pick Detect' bit in the status register is set. Objects to be displayed are labeled by using the Signal instruction which will return the label of the object that intersected the picking area.

Multiple Am95C60 Operation

In order to accomodate systems requiring access to more than four bit-planes, the Am95C60 is designed to be fully cascadable with no performance degradation. Multiple Am95C60 devices can communicate with each other to share timing information for synchronization purposes and status information for color comparisons in depth.

Instructions are broadcast to all Am95C60 devices at once. Each plane will use the instruction in conjunction with its own activity and color bits to decide whether to execute or to ignore the instruction. Each plane may execute the instruction differently, depending on the contents of the individual memory plane and the contents of plane-specific status information.

Broadcasting is accomplished by chip-selecting all Am95C60 QPDMs simultaneously and writing to Port 0. (Write to the instruction FIFO.)

TSYNOUT and TSYNIN are used to synchronize Display Memory operations in a multiple Am95C60 system.

MATOUT and MATIN are used to exchange color searching information in a multiple Am95C60 device system and to synchronize instruction execution.

Interface Description

System Bus Interface

The host connects to the system side of the Am95C60 as depicted in the Logic Symbol diagram. There is a 16-bit data path, and the 8- or 16-bit option allows the Am95C60 QPDM to be connected to an 8- or 16-bit host processor.

The normal bus interface control lines are supported through $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, and two address bits. The address bits are decoded to select one of four ports:

A_1	A_0	WRITE FUNCTION	READ FUNCTION
0	0	Write Instruction FIFO	Read Status
0	1	Write Block Input FIFO	Read Block Output FIFO
1	0	Write Register Addresss	Read Register Address
1	1	Write Register	Read Register

The Am95C60 QPDM can be supported with a DMA controller, allowing blocks of information or instructions to be transferred without tying up the host. In addition to the normal flow-through DMA operations, the Am95C60 also supports fly-by operations.

The Am95C60 also can use interrupts to signal the occurrence of certain events. Some events are repetitive (e.g., Frame), some indicate error conditions (e.g., Stack Overflow), and some merely report status (e.g., Idle). There are registers for masking interrupts, reading interrupt requests, and acknowledging interrupts.

Display Memory Bus Interface

On the Display Memory side, the Am95C60 is capable of controlling four bit planes. Addresses, $\overline{RAS}$, and $\overline{CAS}$ are common signals to all the bit planes while each plane has its own set of data lines and write enable ($\overline{WE}$). Typically, eight or nine address lines (multiplexed Row/Column) go to the VRAM devices while the others may be used for bank select. If multiple banks of memory are used for each bit plane, row addresses must be decoded to select the proper bank.

Each bit plane has a 16-bit data bus used for the Display Memory Update function. Typically, to write a single pixel (one bit in each plane), the Am95C60 would perform simultaneous 16-bit reads from all planes, followed by simultaneous 16-bit writes to all planes. Logic is also provided in the Am95C60 to perform individual pixel writes.

The Am95C60 is intended to be used with a variety of dual-ported Video RAMS (VRAMs). Prior to the beginning of each scan line, the Am95C60 executes a transfer cycle which copies the contents of the scan line into shift registers on the VRAM devices. The scan line image is then shifted out of the VRAM devices 16 bits at a time and further serialized at the dot clock rate for display purposes. The primary VRAM port is available during this time for Display Memory Update.

Display Memory/RAM Size Examples

BIT MAP SIZE	VRAM SIZE	VRAMS/ PLANE	VRAMS/ Am95C60
1024 x 1024	64K x 4	4	16
1024 x 2048	64K x 4	8	32
2048 x 2048	64K x 4	16	64
4096 x 4096	256K x 4	16	64

MEMREQ and MEMAVL are used to allow another processor direct access to the Display Memory.

Video Bus Interface

The Am95C60 generates video timing. Horizontal timing is programmed in terms of VIDCLK cycles and vertical timing is programmed in terms of ½ scan lines.

$\overline{HRESET}$ and $\overline{VRESET}$ are either inputs or outputs depending on the Am95C60's master/slave status. In the case where multiple Am95C60s control the display, one Am95C60 would be programmed as the timing master and the others would be programmed as timing slaves.

Power Connections

The Am95C60 uses +5 volts only.

Performance Figures

Working with VRAMs, the Am95C60 can easily manage high resolution screen formats requiring dot clock rates up to 160 MHz. Moreover, it performs the bit-map update function as indicated in Table 1.

TABLE 1. PERFORMANCE FIGURES OF Am95C60

Instruction	Instruction Overhead	Intermediate Overhead	Execution Time	Comments
Line	12.9 μs	(Not Applicable)	300 nx/pixel	
Line	12.9 μs	(Not Applicable)	4750 ns/pixel	Anti-Aliased
Polyline	10.6 μs	4.8 μs/segment	300 ns/pixel	Connected Segments
Arc	28.2 μs	2.7 μs/octant	750 ns/pixel	
Arc	28.2 μs	2.7 μs/octant	4750 ns/pixel	Anti-Aliased
Circle	9.9 μs	2.7 μs/octant	750 ns/pixel	
Circle	9.9 μs	2.7 μs/octant	4750 ns/pixel	Anti-Aliased
Copy Block	10.9 μs	1.8 μs/scan line	59 ns/pixel	BITBLT
Transform Block	11.0 μs	(Included)	1280 ns/pixel	3X Zoom
Seed Fill	10.0 μs	12.1 μs/scan line	280 ns/pixel	Intermediate Overhead varies with shape
Filled Rectangle	11.9 μs	2.2 μs/scan line	19 ns/pixel	Graphical SET
Filled Triangle	54.9 μs	8.0 μs/scan line	19 ns/pixel	Intermediate Overhead varies with shape
String	6.3 μs	9.4 μs/character	2000 ns/scan line	

The Am95C60 provides extremely fast access at the host interface. A host write requires as little as 80 ns, while a register may be read in as little as 120 ns.

Consult the technical manual (Order No. 07785) to see how these performance measurements are determined.

Register Description

The Am95C60 QPDM contains a number of registers which are programmable from the host. These registers are listed below:

Video Control uses nine registers which define video operation parameters:

- Horizontal Sync Pulse Width (HSYNC)
- Horizontal Scan Delay (HDEL)
- Horizontal Active (HACT)
- Horizontal Total Count (HTOT)
- Vertical Sync Pulse Width (VSYNC)
- Vertical Scan Delay Odd (VDELODD)
- Vertical Scan Delay Even (VDELEVEN)
- Vertical Active Lines (VACT)
- Vertical Total Lines (VTOT)

Visible Screen Coordinates use four registers which contain the (x,y) address in real memory of the top-left and bottom-right corner of the visible screen in Display Memory:

- Screen X Start
- Screen Y Start
- Screen X Terminate
- Screen Y Terminate

Window Control uses six registers which specify where the window is on the screen (the apparent window) and where it begins in memory (the real window):

- Window Apparent X Start
- Window Apparent Y Start
- Window Apparent X Terminate
- Window Apparent Y Terminate
- Window Real X
- Window Real Y

Video Mode Register is used to indicate to each Am95C60 whether it is a timing master or slave, and whether or not interlaced display mode is to be used.

Memory Mode Register specifies Display Memory configuration in terms of memory width and device size (e.g., 4K wide/256K devices).

Dynamic Memory Refresh Rate Register specifies the number of SYSCLK clock cycles between row refreshes in Dynamic Memory Refresh.

Interrupt Enable Register indicates which conditions are allowed to cause interrupts to the host.

Interrupt Acknowledge Register indicates that a specific interrupt condition is known to the host and that the request is to be cancelled in the Am95C60.

Video Timing Enable is a 1-bit register used to enable and disable video sync and output.

Video Refresh Enable is a 1-bit register used to enable and disable the collection of video information from the Display RAM.

System Bus Width Register configures the Am95C60 to 8-bit system bus modes.

Instruction Set

The Am95C60 QPDM is a graphics processor with a powerful instruction set oriented toward graphics processing. One may use any of four addressing modes to specify locations in the display memory: 1) Absolute, 2) Relative, 3) Viewpoint, or 4) Indirect. Each member of the Am95C60 QPDM instruction set is briefly described as follows:

Arc draws the image of a circular arc in Display Memory. The parameters are the center of the arc, the radius of the arc, and the two end-points. The image may be drawn using anti-aliasing, line style, and a logical PEL.

Arc Current draws the image of a circular arc in Display Memory. It is similar to Arc except the start point is taken to be the current pen position (rather than being specified).

Call begins fetching instructions from Display Memory rather than from the instruction FIFO. The parameters specify the

location of the program to be executed. A stack in Display Memory is used to contain the return location.

Circle draws the image of a circle in Display Memory. The parameters are the circle's center and radius. The image may be drawn using anti-aliasing, line style, and a logical PEL.

Circle Current draws the image of a circle in Display Memory. It is similar to Circle, except the center is taken to be the current pen position.

Control Clipping enables or disables the clipping function. When clipping is enabled, all drawing primitives will change only that portion of Display Memory which lies within the rectangular clipping region.

Control Picking enables or disables the picking function. When picking is enabled, drawing primitives will not execute any writes to the Display Memory. The Pick Detect status bit is set whenever a drawing primitive intersects the picking area.

Copy Block moves a block of data within Display Memory and may optionally combine the source image with the destination image. The size of the block will have been determined by a Set Block Size instruction. The location of each block, source and destination, is determined by the instruction.

Copy Block Current is identical to the Copy Block instruction except that the source operand is the current pen position.

Define Logical PEL specifies the logical PEL (pen size and content) used by the drawing primitives. This can be used to draw thick lines.

Fill Bounded Region fills an arbitrary polygon with a specific color. The polygon is defined as the group of dots completely contained within a boundary of pixels of the edge color. All pixels will be changed to the current drawing color. The location of the seed is specified in the instruction.

Fill Bounded Region Current fills an arbitrary polygon with a specific color. The polygon is defined as the group of dots completely contained within a boundary of pixels of the edge color. All pixels in the region will be changed to the current drawing color. The location of the seed is the current pen position.

Fill Connected Region fills an arbitrary polygon with a specific color. The polygon is defined as any group of connected dots of the seed's color. All pixels connected to the seed point having the same color will be changed to the current drawing color. The location of the seed is specified in the instruction.

Fill Connected Region Current fills an arbitrary polygon with a specific color. The polygon is defined as any group of connected dots of the seed's color. All pixels connected to the seed point having the same color will be changed to the current drawing color. The location of the seed is the current pen position.

Filled Rectangle creates the image of a rectangle and fills it. The parameters specify two opposite corners of the rectangle. The color of the filled rectangle is the current drawing color.

Filled Rectangle Current is similar to Fill Rectangle except the current pen position is taken to be the starting corner of the rectangle. The other corner is specified by the instruction.

Filled Triangle creates the image of a triangle and fills it. The parameters specify the three vertices of the triangle. The color of the filled triangle is the current drawing color.

Filled Triangle Current creates the image of a triangle and fills it. The parameters specify two vertices of the triangle. The current pen position is taken to be the third vertex of the triangle. The color of the filled triangle is the current drawing color.

Input Block transfers a rectangular block of data from the host to Display Memory. The size of the block will have been determined by a Set Block Size instruction. The destination address in the Display Memory is specified in the instruction. The data to be stored in Display Memory is written into the Data FIFO.

Input Block Current transfers a rectangular block of data from the host to Display Memory. The size of the block will have been determined by a Set Block Size instruction. The destination address in the Display Memory is the current pen position. The data to be stored in Display Memory is written into the Data FIFO.

Jump unconditionally changes the location counter when executing instructions from Display Memory.

Line draws the image of a line in Display Memory. The input parameters are the two ends of the line. The image may be drawn using anti-aliasing, line style, and a logical PEL. Multiple lines may be drawn with a single line instruction.

Line Current is similar to Line, except the current drawing position is taken to be the starting point of the line.

Line Reversible draws the image of a line in Display Memory. It is exactly the same as Line except that the standard algorithm is modified to guarantee that the same set of pixels is chosen regardless of the order of the end points.

Line Reversible Current is similar to Line Reversible except that the current pen position is taken to be the starting point of the line.

Move Pen sets the current pen position.

No Operation ensures that no operation is performed.

Output Block transfers a rectangular block of data from Display Memory to the host. The size of the block will have been determined by a Set Block Size instruction. The source address in the Display Memory is specified in the instruction. The host is expected to remove the data from the Data FIFO.

Output Block Current transfers a rectangular block of data from Display Memory to the host. The size of the block will have been determined by a Set Block Size instruction. The source address in the Display Memory is the current pen position. The host is expected to remove the data from the Data FIFO.

Point draws the image of the current logical PEL at the location specified in the instruction.

Point Current draws the image of the current logical PEL at the current pen position.

Return exits from a subroutine or from program mode when executing instructions from Display Memory.

Set Activity Bits indicates which of the four Display Memory planes, controlled by the Am95C60, are to be written into.

Set Anti-Aliasing Distance programs the anti-aliasing distance deviation from the ideal line.

Set Block Size specifies the number of pixels moved in any block operation. This is used for Input Block, Output Block, Copy Block, Transform Block, and the logical PEL.

Set Character Font Base specifies the character font address in the Display Memory. The character font contains the patterns of letters and numbers used by the String instruction.

Set Character Font Base Current specifies the character font addresses in Display Memory.

Set Clipping Boundary specifies where the clipping region is in Display Memory. When clipping is enabled, all drawing primitives will change only that portion of Display Memory which

lies within the rectangular clipping region. The parameters are the addresses of two opposite corners of the clipping rectangle.

Set Clipping Boundary Current specifies where the clipping region is in Display Memory. When clipping is enabled, all drawing primitives will change only that portion of Display Memory which lies within the rectangular clipping region. The current pen position is taken to be the start corner of the clipping rectangle.

Set Color Bits sets the current drawing color.

Set Search Color specifies the edge color used in Fill instructions.

Set Line Style specifies the line style. This defines the dash length, the interspace length, and the dot length.

Set Line Style Phase indicates where the line begins within the line style cycle.

Set Listen Bits indicates which planes take part in polygon and color change operations. If set, the corresponding plane does not participate in the color matching.

Set Picking Region specifies the rectangular area to be picked. The parameters are two opposite corners of the picking rectangle. When picking is enabled, drawing primitives that intersect the picking region will cause the "Pick Detect" bit in the status register to be set and no writes will be executed to Display Memory.

Set Picking Region Current specifies the rectangular area to be picked. The parameters are two opposite corners of the picking rectangle. The current pen position is taken to be the start corner of the picking region. When picking is enabled, drawing primitives that intersect the picking region will cause the "Pick Detect" bit in the status register to be set and no writes will be executed to Display Memory.

Set QPDM Position specifies the logical addresses for each Display Memory plane.

Set Scale Factor provides values used to multiply the operands of instructions which address the bit map.

Set Search Color specifies the color of the boundary for Fill Boundary Area operations.

Set Stack Boundaries specifies to the Am95C60 which area of Display Memory has been set aside for the stack. Stack overflow is detected and signaled to the host with an interrupt.

Set Viewpoint Location specifies the base address for Viewpoint Addressing Mode.

Signal is used to indicate to the host when a particular point in the instruction stream has been reached, to delimit objects during picking, or to pause operation pending a signal from the host.

Store Immediate deposits a specified number of 16-bit words in the Display Memory.

Store Immediate Current deposits a specified number of 16-bit words in Display Memory beginning at the current pen position.

String is used to create the image of a string of text in the Display Memory. The parameters are the address at which the string should begin, followed by a variable length list of 16-bit pointers. Each pointer is used to look up a pattern in the character font table.

String Current is similar to String except the address at which the string should begin is set to the current pen position.

Transform Block allows a block of data to be taken from Display Memory, operated on, and written to a different area of Display Memory. The operations which may be performed are Rotate (90 degree increments), Zoom (by pixel replication), and Mirror. The Zoom in X, and Zoom in Y are independently specified. The size of the source block (prior to rotation and zooming) will have been specified by a Set Block Size instruction.

Transform Block Current is similar to Transform Block except the source operand is at the current pen position.

APPLICATIONS

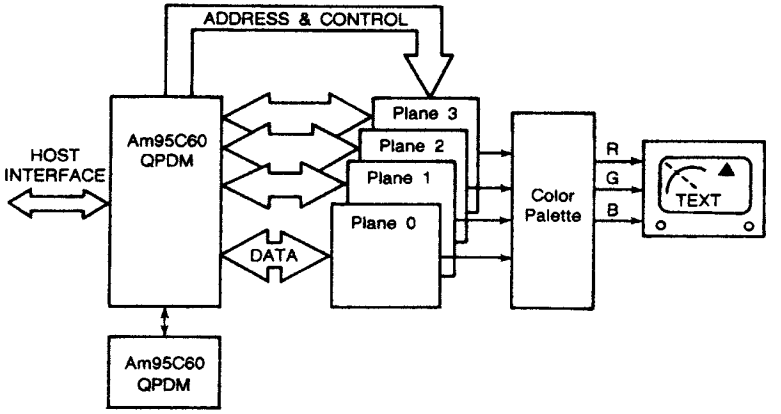


Figure 1. Typical System Application

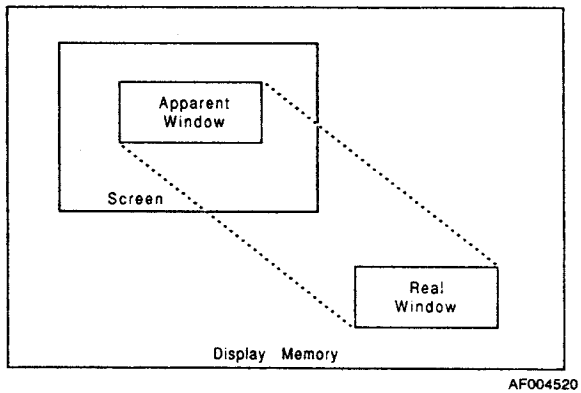


Figure 2. Windows

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Operating Temperature ..... −55 to +125°C
Maximum V_{CC} Relative to V_{SS} ..... −0.3 to +7.0 V
DC Voltage Applied to Any
Pin Relative to V_{SS} ..... −0.5 to V_{CC} +0.3 V

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Ambient Temperature (T_A) ..... 0 to +70°C
Supply Voltage (V_{CC}) ..... +4.75 to +5.25 V

Military (M) and Extended-Commercial (E) Devices
Case Temperature (T_C) ..... −55 to +125°C
Supply Voltage (V_{CC}) ..... +4.50 to 5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating ranges unless otherwise specified (for APL products, Group A, Subgroups 1, 2, 3, 7, 8 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
V_{IL}	Input LOW Voltage			−0.3	+0.8	V
V_{IH}	Input HIGH Voltage		COM'L	+2.0	V_{CC} + 0.3	V
			MIL & E-COM'L	+2.2		
V_{OL}	Output LOW Voltage COM'L Devices CAS and $\overline{XF/G}$	I_{OL} = 4.0 mA			0.4	V
	Output LOW Voltage Commercial Devices All Other Outputs	I_{OL} = 2.0 mA			0.4	
	Output LOW Voltage Military Devices CAS and $\overline{XF/G}$	I_{OL} = 12 mA			0.45	
	Output LOW Voltage Military Devices All Other Outputs	I_{OL} = 8.0 mA			0.45	
V_{OH}	Output HIGH Voltage	I_{OH} = 250 µA		2.4		V
I_{OZ}	Output Leakage Current	0.4 < V_{OUT} < V_{CC}			±10	µA
I_I	Input Current	0.4 < V_{IN} < V_{CC}			±10	µA
I_{CC}	Power Supply Current (Note 1)				250	mA

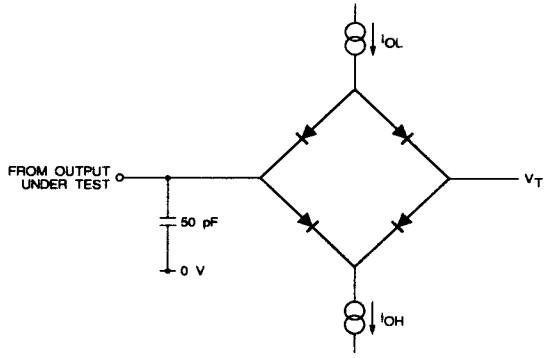
CAPACITANCE*

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
C_{IN}	Input Capacitance			15	pF
$C_{I/O}$	I/O Pin Capacitance			25	pF
C_{OUT}	Output Pin Capacitance			25	pF

*Parameters are not 100% "Tested." Characterization data on file.

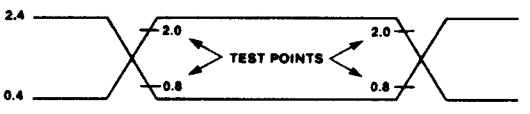
Notes: 1. For operation with SYSCLK less than 20 MHz, deduct approximately 6.5 mA/MHz.

SWITCHING TEST CIRCUIT

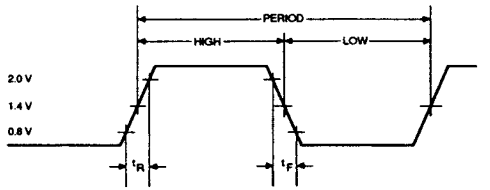


TC003860

SWITCHING TEST WAVEFORMS



WF009541



WF025740

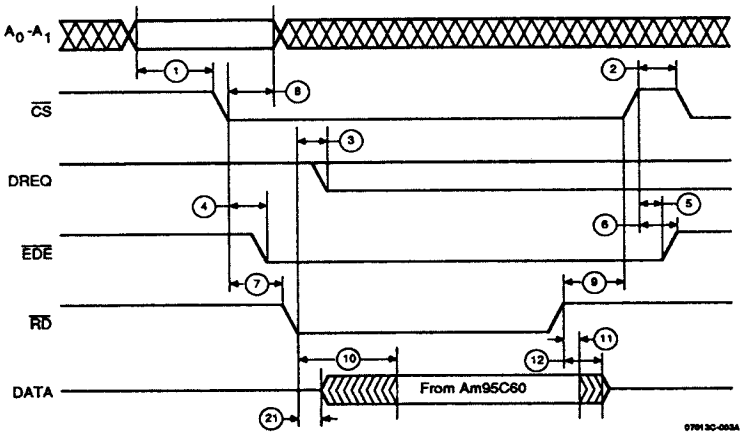
VIDCLK/SYSCLK Waveform

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

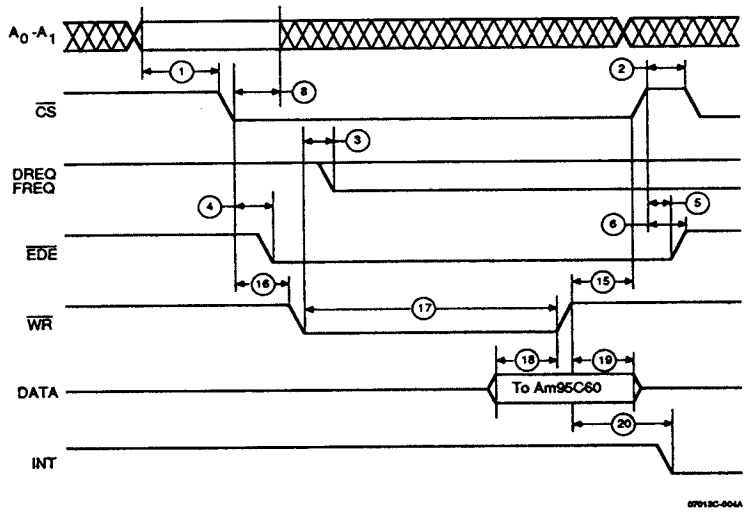
KS000010

SWITCHING WAVEFORMS/CHARACTERISTICS



WF026510

Processor/DMA Flow-Through Read Cycle

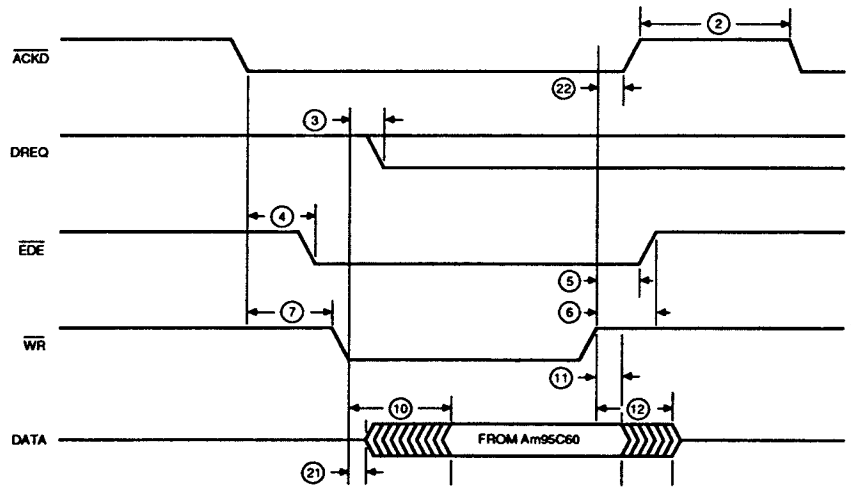


WF026520

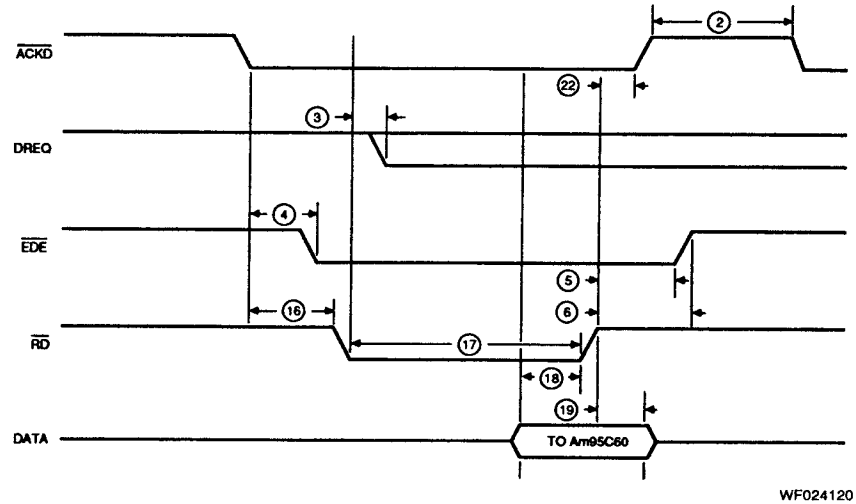
Processor/DMA Flow-Through Write Cycle

3

SWITCHING WAVEFORMS/CHARACTERISTICS (Cont'd.)



DMA Fly-By Read Cycle



DMA Fly-By Write Cycle

SWITCHING WAVEFORMS/CHARACTERISTICS over operating ranges unless otherwise specified (for APL products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

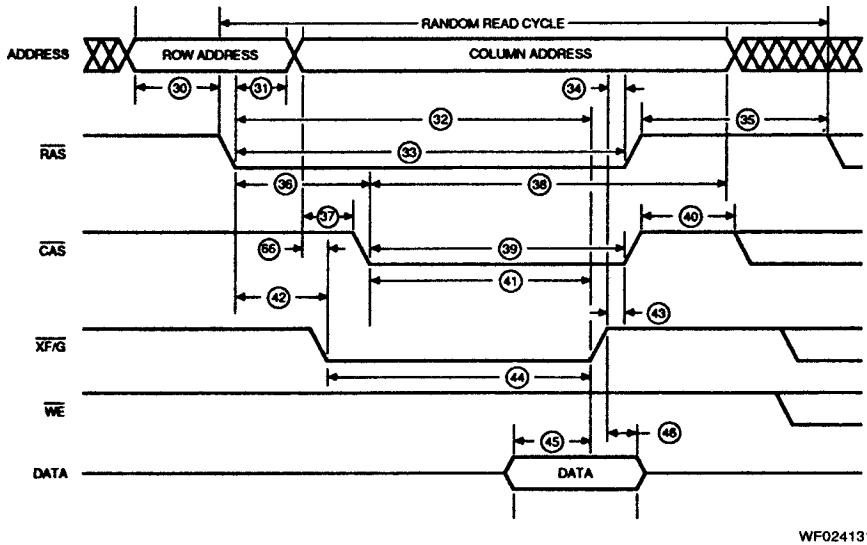
System Bus Timing

No.	Parameter Symbol	Parameter Description		-20 Min.	-20 Max.	-18 Min.	-18 Max.	-16 Min.	-16 Max.	Unit
1	t_S	Requires that the address be valid a minimum of ‖ ns before $\overline{CS}$ begins to fall.		0		0		0		ns
2	t_W (Note 1)	Requires that both $\overline{CS}$ and $\overline{ACKD}$ be inactive a minimum of ‖ ns before either can go active.		65		65		95		ns
3	t_{PHL}	Guarantees that DREQ will become inactive a maximum of ‖ ns after $\overline{RD}$ or $\overline{WR}$ becomes active.			55		55		60	ns
4	t_{PHL} (Note 1)	Guarantees that $\overline{EDE}$ will become active a maximum of ‖ ns after $\overline{CS}$ becomes active. Also guarantees that $\overline{EDE}$ will become active a maximum of ‖ ns after $\overline{ACKD}$ becomes active.			60		60		60	ns
5	t_{PLH} (Notes 1, 3)	Guarantees that $\overline{EDE}$ will remain active a minimum of ‖ ns after $\overline{CS}$ becomes inactive. Also guarantees that $\overline{EDE}$ will remain active a minimum of ‖ ns after $\overline{RD}$ has become inactive.		10		10		10		ns
6	t_{PLH} (Notes 1, 3)	Guarantees that $\overline{EDE}$ will have gone inactive no more than ‖ ns after $\overline{CS}$ has become inactive. Also guarantees that $\overline{EDE}$ will have gone inactive no more than ‖ ns after $\overline{RD}$ has become inactive.			65		65		70	ns
7	t_S (Notes 1, 2)	Requires that $\overline{CS}$ be valid a minimum of ‖ ns before $\overline{RD}$ can begin to go active. Also requires that $\overline{ACKD}$ be valid a minimum of ‖ before $\overline{WR}$ can begin to go active.		0		0		0		ns
8	t_H	Requires that the address remain valid a minimum of ‖ ns after $\overline{CS}$ has gone active.		20		20		20		ns
9	t_H	Requires that $\overline{CS}$ remain active a minimum of ‖ ns after $\overline{RD}$ has gone inactive.		0		0		0		ns
10	t_{PD} (Note 2)	Guarantees that the read data will be valid within ‖ ns of $\overline{RD}$ becoming active. Also guarantees that the read data will be valid within ‖ ns of $\overline{WR}$ becoming active in a Fly-By Read Cycle.			110		110		110	ns
11	t_H (Notes 2, 3)	Guarantees that the read data will remain valid a minimum of ‖ ns after $\overline{RD}$ has gone inactive. Also guarantees that the read data will remain valid a minimum of ‖ ns after $\overline{WR}$ has gone inactive in a Fly-By Read Cycle.		10		10		10		ns
12	t_{PD} (Notes 2, 3)	Guarantees that the read buffers will become under high impedance within ‖ ns of $\overline{RD}$ having gone inactive. Also guarantees that the read buffers will become under high impedance within ‖ ns of $\overline{WR}$ having gone inactive in a Fly-By Read Cycle.			40		40		40	ns
13	(Not used)	Not Used								
14	(Not used)	Not Used								
15	t_H	Requires that $\overline{CS}$ remain active a minimum of ‖ ns after $\overline{WR}$ has gone inactive.		10		10		20		ns
16	t_S (Notes 1, 2)	Requires that $\overline{CS}$ be active a minimum of ‖ ns before $\overline{WR}$ can begin to go active. Also requires that $\overline{ACKD}$ be active a minimum of ‖ ns before $\overline{RD}$ can begin to go active in a Fly-By Write Cycle.		0		0		0		ns
17	t_W	Requires that $\overline{WR}$ be active for a minimum of ‖ ns. Also requires that $\overline{RD}$ be active a minimum of ‖ ns in the case of a Fly-By Write Cycle. Also requires that $\overline{ACKD}$ remain active a minimum of ‖ ns after $\overline{RD}$ has gone active in a Fly-By Write Cycle.		70		70		90		ns
18	t_S (Notes 2, 3)	Requires that the write data be active for a minimum of ‖ ns before $\overline{WR}$ begins to go inactive. Also requires that the write data be active for a minimum of ‖ ns before $\overline{RD}$ or $\overline{ACKD}$ (whichever is first) begins to go inactive in a Fly-By Write Cycle.		55		55		75		ns
19	t_H (Notes 2, 3)	Requires that the write data be kept valid for a minimum of ‖ ns after $\overline{WR}$ has gone inactive. Also requires that the write data be kept valid for a minimum of ‖ ns after $\overline{RD}$ or $\overline{ACKD}$ (whichever is first) has gone inactive in a Fly-By Write Cycle.	Word Mode	0		0		0		ns
			Byte Mode	15		15		25		ns
20	t_{PHL}	Guarantees that the INT line will become inactive no more than ‖ ns after $\overline{WR}$ has gone inactive.			120		120		150	ns
21	t_{PD}	Guarantees that the data buffers will not become active before $\overline{RD}$ goes active. Also guarantees that the data buffers will not become active before $\overline{WR}$ goes active in a Fly-By Read Cycle.		0		0		0		ns
22	t_H	Requires that $\overline{ACKD}$ be active a minimum of ‖ ns after $\overline{RD}$ or $\overline{WR}$ has gone inactive.		0		0		0		ns
23–29	(Not used)	Not Used								

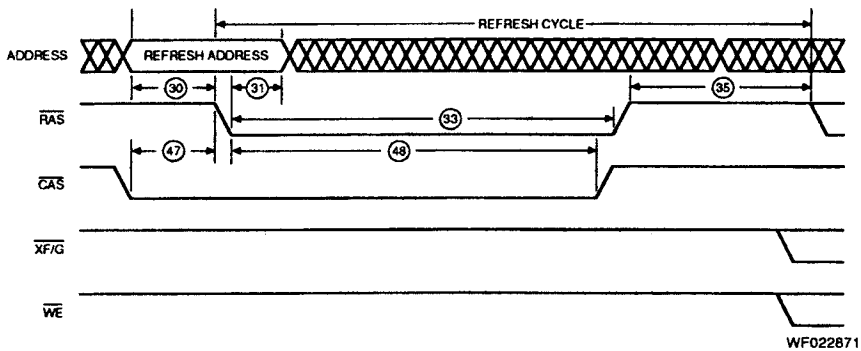
Notes: See notes at end of this section.

3

SWITCHING WAVEFORMS/CHARACTERISTICS (Cont'd.)

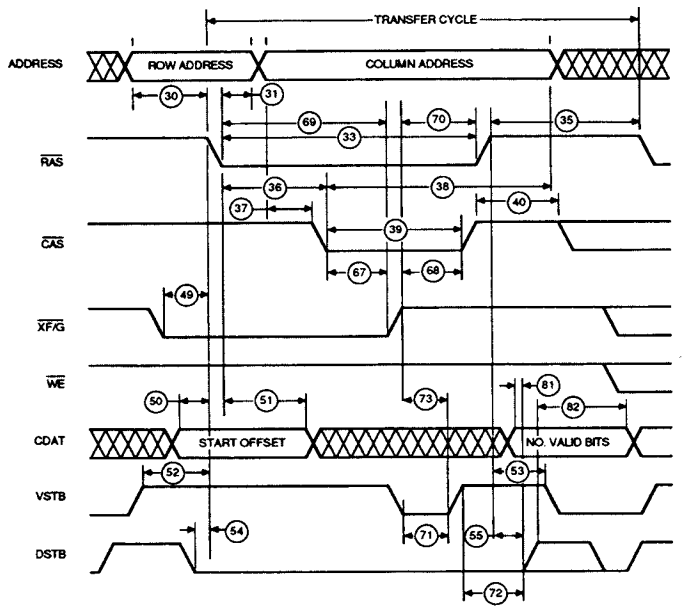


Display Memory Read Cycle

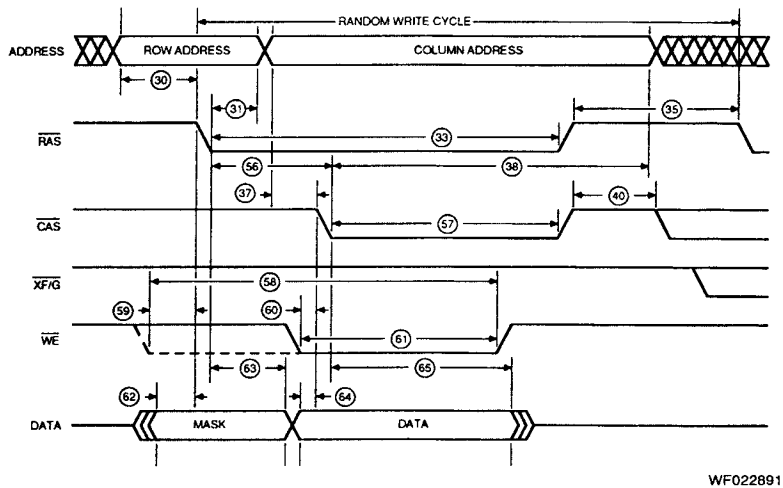


Display Memory Dynamic RAM Refresh Cycle

SWITCHING WAVEFORMS/CHARACTERISTICS (Cont'd.)



Display Memory Transfer Cycle



Display Memory Write Cycle

SWITCHING WAVEFORMS/CHARACTERISTICS (Cont'd.)
Display Memory Interface

No.	Parameter Symbol	Parameter Description	-20 Min.	-20 Max.	-18 Min.	-18 Max.	-16 Min.	-16 Max.	Unit
30	t_S (Note 4)	Guarantees the row address will be stable (valid) a minimum of ‖ ns before $\overline{RAS}$ begins to go active.	15		18		16		ns
31	t_H (Note 4)	Guarantees the row address will remain valid a minimum of ‖ ns after $\overline{RAS}$ has gone active.	35		41		45		ns
32	t_{PD} (Note 4)	Guarantees that $\overline{XF7G}$ will not go inactive until a minimum of ‖ ns after $\overline{RAS}$ has gone active for a read cycle.	160		181		202		ns
33	t_W (Note 4)	Guarantees that $\overline{RAS}$ will be active for a minimum of ‖ ns.	180		204		225		ns
34	t_H (Note 4)	Guarantees that $\overline{RAS}$ will remain active for a minimum of ‖ ns after $\overline{XF7G}$ has gone inactive for a read cycle.	14		5		15		ns
35	t_W (Note 4)	Guarantees that $\overline{RAS}$ will remain not active for a minimum of ‖ ns.			106		115		ns
36	t_{PD} (Note 4)	Guarantees that $\overline{CAS}$ will not become active until a minimum of ‖ ns after $\overline{RAS}$ has gone active. See parameter 56 for write cycles.			74		78		ns
37	t_S (Note 4)	Guarantees that the column address will be valid and stable a minimum of ‖ ns before $\overline{CAS}$ goes active.	13		14		15		ns
38	t_H (Note 4)	Guarantees that the column address will remain valid and stable a minimum of ‖ ns after $\overline{CAS}$ has gone active.	80		92		104		ns
39	t_W (Note 4)	Guarantees that $\overline{CAS}$ will be active a minimum of ‖ ns for a read cycle or a transfer cycle. See parameter 57 for writes cycles.	100		115		130		ns
40	t_W (Note 4)	Guarantees that $\overline{CAS}$ will remain inactive for a minimum of ‖ ns. This is important when a refresh cycle follows any cycle.	40		46		47		ns
41	t_{PD} (Note 4)	Guarantees that $\overline{XF7G}$ will not have gone inactive until a minimum of ‖ ns after $\overline{CAS}$ has gone active for a read cycle.	90		95		113		ns
42	t_{PD} (Note 4)	Guarantees that $\overline{XF7G}$ will not begin to go active until a minimum of ‖ ns after $\overline{RAS}$ has gone active.	39		45		46		ns
43	t_H (Note 4)	Guarantees that $\overline{CAS}$ will remain active until a minimum of ‖ ns after $\overline{XF7G}$ has gone inactive for a read cycle.	13		14.5		16		ns
44	t_W (Note 4)	Guarantees that $\overline{XF7G}$ will be active a minimum of ‖ ns for a read cycle.	105		120		125		ns
45	t_S	Requires that the read data be valid a minimum of ‖ ns before $\overline{XF7G}$ begins to go inactive.	17		20		23		ns

Notes: See notes at end of this section.

SWITCHING WAVEFORMS/CHARACTERISTICS (Cont'd.)

Display Memory Interface (Cont'd.)

No.	Parameter Symbol	Parameter Description	-20		-18		-16		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
46	t_H	Requires that the read data remain valid a minimum of [] ns after $\overline{XF7/G}$ has gone inactive.	0		0		0		ns
47	t_S (Note 4)	Guarantees that $\overline{RAS}$ will not begin to go active until a minimum of [] ns after $\overline{CAS}$ has become active in a refresh cycle.	37		43		45		ns
48	t_H (Note 4)	Guarantees that $\overline{CAS}$ will not begin to go inactive until a minimum of [] ns after $\overline{RAS}$ has gone active in a refresh cycle.	185		204		230		ns
49	t_S (Note 4)	Guarantees that $\overline{RAS}$ will not begin to go active until a minimum of [] ns after $\overline{XF7/G}$ is active in a transfer cycle.	12		12		13		ns
50	t_S (Note 4)	Guarantees that the Start Offset on CDAT will be valid and stable a minimum of [] ns before $\overline{RAS}$ begins to go active in a transfer cycle.			10		11		ns
51	t_H (Note 4)	Guarantees that the Start Offset on CDAT will remain valid and stable a minimum of [] ns after $\overline{RAS}$ has gone active in a transfer cycle.	65		71.5		78		ns
52	t_S (Note 4)	Guarantees that VSTB will be HIGH a minimum of [] ns before $\overline{RAS}$ begins to go active in a transfer cycle.	90		102		109		ns
53	t_H (Note 4)	Guarantees that VSTB will remain HIGH a minimum of [] ns after $\overline{RAS}$ has gone inactive in a transfer cycle.	80		92		99		ns
54	t_S (Note 4)	Guarantees that VSTB will be LOW a minimum of [] ns before $\overline{RAS}$ begins to go active in a transfer cycle.	90		102		109		ns
55	t_H (Note 4)	Guarantees that VSTB will remain LOW a minimum of [] ns after $\overline{RAS}$ has gone inactive in a transfer cycle.	80		92		99		ns
56	t_{PD} (Note 4)	Guarantees that $\overline{CAS}$ will not become active until a minimum of [] ns after $\overline{RAS}$ has gone active. This is for a write cycle. See parameter 36 for read and transfer cycles.	90		99.5		109		ns
57	t_W (Note 4)	Guarantees that $\overline{CAS}$ will be active a minimum of [] ns for a write cycle. See parameter 39 for read and transfer cycles.	80		90		100		ns
58	t_W (Note 4)	Guarantees that $\overline{WE_0}$-$\overline{WE_3}$ will be active a minimum of [] in the case of a masked write.	180		204		225		ns
59	t_S (Notes 4, 5)	Guarantees that $\overline{WE_0}$-$\overline{WE_3}$ will be active a minimum of [] before $\overline{RAS}$ begins to fall in the case of masked write.	11		12.5		14		ns

Notes: See notes at end of this section.

SWITCHING WAVEFORMS/CHARACTERISTICS (Cont'd.)
Display Memory Interface (Cont'd.)

No.	Parameter Symbol	Parameter Description	-20		-18		-16		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
60	t_S (Note 4)	Guarantees that $\overline{WE_0}$–$\overline{WE_3}$ will be active a minimum of ‖ before $\overline{CAS}$ begins to fall in the case of a unmasked write.	13		13		14		ns
61	t_W (Notes 4, 5)	Guarantees that $\overline{WE_0}$–$\overline{WE_3}$ will be active a minimum of ‖ in the case of an unmasked write.	78		89		100		ns
62	t_S	Guarantees that the write mask will be valid and stable on the DM pins ‖ before $\overline{RAS}$ begins to go active.	2		2		7		ns
63	t_H (Notes 4, 5)	Guarantees that the write mask will remain active ‖ after $\overline{RAS}$ has gone active.	60		66.5		73		ns
64	t_S	Guarantees that the write data will be valid and stable on the DM pins ‖ before $\overline{CAS}$ begins to go active.	2		2		7		ns
65	t_H (Notes 4, 5)	Guarantees that the write data will remain active ‖ after $\overline{CAS}$ has gone active.	60		66.5		73		ns
66	t_S	Guarantees that the column address will be valid ‖ ns before $\overline{XF7/G}$ goes active.	-8		-10		-12		ns
67	t_{PD} (Note 4)	Guarantees that $\overline{XF7/G}$ will not go inactive until a minimum of ‖ ns after $\overline{CAS}$ has gone active for a transfer cycle.	55		64		69		ns
68	t_H (Note 4)	Guarantees that $\overline{CAS}$ will remain active until a minimum of ‖ ns after $\overline{XF7/G}$ has gone inactive for a transfer cycle.	38		44		47		ns
69	t_{PD} (Note 4)	Guarantees that $\overline{XF7/G}$ will not go inactive until a minimum of ‖ ns after $\overline{RAS}$ has gone active for a transfer cycle.	135		153		171		ns
70	t_H (Note 4)	Guarantees that $\overline{RAS}$ will remain active until a minimum of ‖ ns after $\overline{XF7/G}$ has gone inactive for a transfer cycle.	39		45		46		ns
71	t_W (Note 4)	Guarantees that VSTB will remain LOW a minimum of ‖ during a transfer cycle.	35		41		42		ns
72	t_{PH} (Note 4)	Guarantees that the first positive edge on VSTB will have occurred a minimum of ‖ before the first positive edge on DSTB following a transfer cycle.	80		92		99		ns
73	t_S (Note 4)	Guarantees that $\overline{XF7/G}$ will have gone inactive a minimum of ‖ before the first positive edge on VSTB following a transfer cycle.	40		46		47		ns

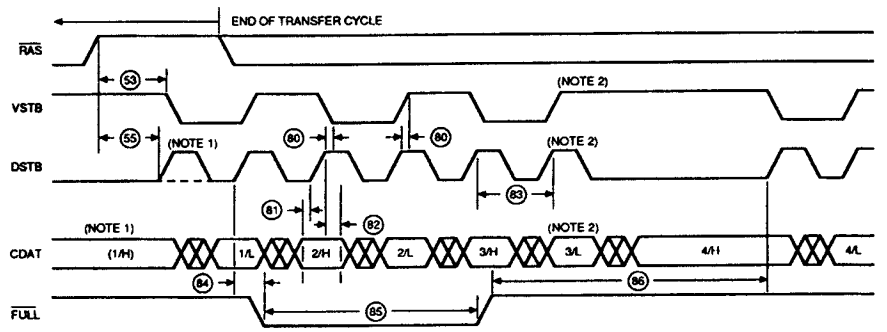
Notes: See notes at end of this section.

SWITCHING WAVEFORMS/CHARACTERISTICS (Cont'd.)

VDAF Interface Timing

No.	Parameter Symbol	Parameter Description	-20 Min.	-20 Max.	-18 Min.	-18 Max.	-16 Min.	-16 Max.	Unit
80	t_{PD}	Guarantees that VSTB will change to the new state within 0–[illegible] ns following the positive edge of DSTB.	-3	10	-3	15	-3	15	ns
81	t_S	Guarantees the value on CDAT will be valid and stable a minimum of [illegible] before DSTB begins to rise.	[illegible]		8		10		ns
82	t_H	Guarantees the value on CDAT will remain valid a minimum of [illegible] after the rising edge of DSTB.	[illegible]		15		20		ns
83	t_{PD} (Note 4)	Guarantees the positive edges on DS[illegible] will occur the same period as SYSCLK.	50		56		62		ns
84	t_S	Guarantees that FULL will be [illegible] the current SYSCLK cycle if it is valid a [illegible] ns before the edge. This is not [illegible] parameter; if this setup time is not met, the part will not go metastable.		25		28		30	ns
85	t_W (Note 4)	Requires that FULL remain active at least one SYSCLK period.	50		56		62		ns
86	t_{PLH} (Note 4)	Guarantees that a positive edge will not occur on DSTB until a minimum of [illegible] ns following FULL going inactive.	150		168		186		ns
87–89	(Not used)	Not used							

Notes: See notes at end of this section.



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Notes: 1. DSTB & CDAT for (1/H) only occurs on even boundaries.
2. One less byte may be strobed after FULL active.
3. CDAT 1/H = CDAT for 1st word HIGH byte.

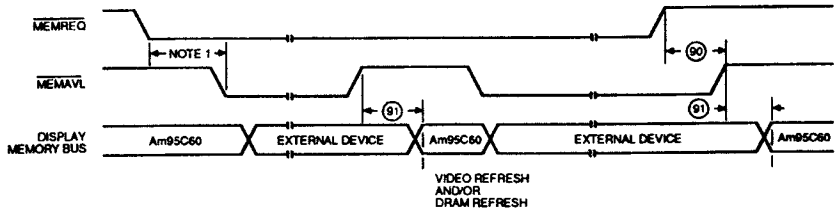
VDAF Interface Timing

SWITCHING WAVEFORMS/CHARACTERISTICS (Cont'd.)

VDAF Interface Timing

No.	Parameter Symbol	Parameter Description	-20 Min.	-20 Max.	-18 Min.	-18 Max.	-16 Min.	-16 Max.	Unit
90	t_{PLH} (Note 4)	Guarantee [illegible] Am95C60 will make MEMAVL [illegible] within [illegible] MEMREQ line inactive.						190	ns
91	t_{PD} (Notes 4, 6)	Guarantee that the Am95C60 will not be [illegible] cycle for a minimum of [illegible] after the rising edge of MEMAVL.					558		ns
92–99	(Not used)	Not Used							

Notes: See notes at end of this section.



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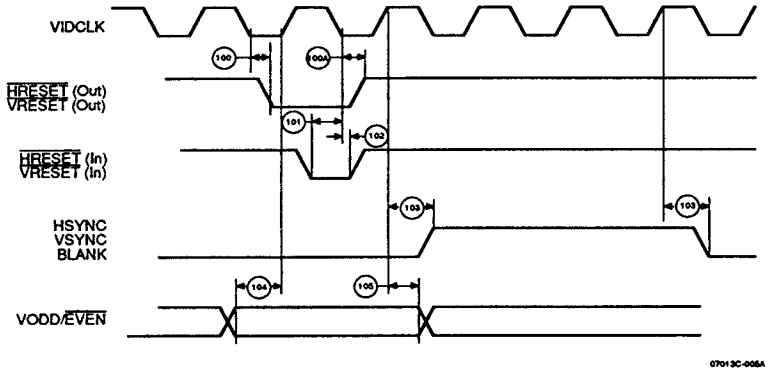
Notes: 1. $\overline{MREQ}$ to $\overline{MEMAVL}$ DELAY = Minimum 6C for arbitration cycle
= Maximum 24C

} Not an operating parameter; provided for reference only.

2. Display Memory Bus = ADDR, $\overline{RAS}$, $\overline{CAS}$, $\overline{XF7G}$, $\overline{WE}$, DATA
3. Parameter 91 is referenced to $\overline{RAS}$ falling edge, which defines the start of the QPDM cycle

Display Memory Arbitration Timing



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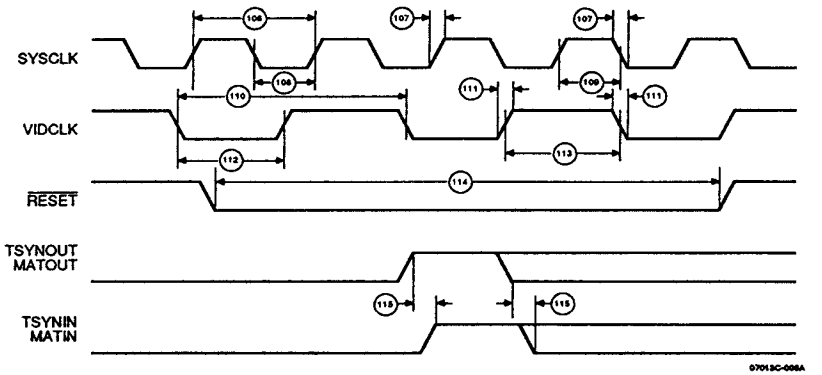
Video Control Timings



WF026540

Clocks, Reset, and Am95C60 Synchronization Timings

SWITCHING WAVEFORMS/CHARACTERISTICS (Cont'd.)

Miscellaneous Timing

No.	Parameter Symbol	Parameter Description	-20 Min.	-20 Max.	-18 Min.	-18 Max.	-16 Min.	-16 Max.	Unit
100	t_{PD}	Guarantees that the HIGH-to-LOW transition on HRESET and VRESET will occur a maximum of || ns following the HIGH-to-LOW transition of VIDCLK. This is effective only if HRESET and VRESET are programmed as output(s).		25		25		30	ns
100A	t_H	Guarantees that the LOW-to-HIGH transition on HRESET will not occur until a minimum of || following the HIGH-to-LOW transition of VIDCLK. This is effective only if HRESET and VRESET are programmed as output(s).	0		0		0		ns
101	t_S	Requires the HRESET and VRESET be valid a minimum of || ns prior to the HIGH-to-LOW transition of VIDCLK.	20		20		25		ns
102	t_H	Requires that HRESET and VRESET remain valid a minimum of || ns following the HIGH-to-LOW transition of VIDCLK.			0		0		ns
103	t_{PD}	Guarantees that transitions on BLANK, HSYNC and VSYNC will occur within a maximum of || ns of rising edge of VIDCLK.		30		30		40	ns
104	t_S	Requires that VODD/$\overline{EVEN}$ be valid a minimum of || ns prior to the rising edge of VIDCLK.	15		15		20		ns
105	t_H	Requires that VODD/$\overline{EVEN}$ remain valid a minimum of || ns after VIDCLK has risen.	15		15		20		ns
106	t_{CYC}	Requires that the period of SYSCLK be between || and || ns.	50	500	56	500	62	500	ns
107	t_T (Note 8)	Requires that SYSCLK transition times be a maximum of || ns.		5		5		5	ns
108	t_W	Requires that SYSCLK LOW time be a minimum of || ns.	23		25		28		ns
109	t_W	Requires that SYSCLK HIGH time be a minimum of || ns.	23		25		28		ns
110	t_{CYC}	Requires that the period of VIDCLK be between || and ||.	66	4000	66	4000	72	4000	ns
111	t_T (Note 8)	Requires that the VIDCLK transition time be a maximum of || ns.		5		5		5	ns
112	t_W	Requires that the VIDCLK LOW time be a minimum of || ns.	27		27		29		ns
113	t_W	Requires that VIDCLK HIGH time be a minimum of || ns.	27		27		29		ns
114	t_W (Note 4)	Requires that $\overline{RESET}$ remain active a minimum of || ns.	200		224		248		ns
115	t_{PD}	Requires that the external delay from TSYNOUT to TSYNIN and the external delay from MATOUT to MATIN be a maximum of || ns.		17		17		20	ns

Notes: 1. Timings are relative to $\overline{CS}$ or $\overline{ACKD}$.
2. $\overline{RD}$ and $\overline{WR}$ reverse operations in Fly-By DMA cycles.
3. Timings are relative to $\overline{RD}$/$\overline{WR}$ or $\overline{ACKD}$ rising edge, whichever occurs first.
4. See Switching Characteristics Formulas.
5. This timing applies for masked writes.
6. All display memory cycles are exactly six SYSCLK cycles.
7. The units of all Switching parameters are ns.
8. Tests for parameters 107 and 111 are not being performed in manufacturing.

Switching Characteristics Formulas

All the Switching Characteristics which reference Note 4 are calculated with the formulas which follow. Each parameter is some number of SYSCLK cycles (or parts of SYSCLK cycles). In addition, there is an adder for each of the three speed classes.

The numbers which are given in the Switching Characteristics are derived by evaluating the formulas assuming the following SYSCLK periods shown below:

FREQ	PERIOD
-20	50 ns
-18	56 ns
-16	62 ns

Users who wish to operate the Am95C60 at more than these SYSCLK periods may use these formulas to calculate the Switching Characteristics for their actual system.

Switching Characteristics Formulas

Parameter No.	Nominal	-20	-18	-16
30	c/2	-10	-10	-15
31	c	-15	-15	-17
32	7c/2	-15	-15	-15
33	4c	-20	-20	-23
34	c/2	-11	-13.5	-16
35	2c	-5	-6	-15
36	3c/2	-10	-10	-15
37	c/2	-12	-14	-16
38	2c	-20	-20	-20
39	5c/2	-25	-25	-25
40	c	-10	-10	-15
41	2c	-20	-20	-24
42	c	-11	-11	-16
43	c/2	-12	-13.5	-15
44	5c/2	-20	-20	-30
47	c	-13	-13	-17
48	4c	-15	-20	-18
49	c/2	-13	-16	-18
50	c/2	-15	-18	-20
51	3c/2	-10	-12.5	-15
52	2c	-10	-10	-15
53	2c	-10	-12.5	-15
54	2c	-10	-10	-15
55	2c	-10	-12.5	-15
56	2c	-10	-12.5	-15
57	2c	-20	-22	-24
58	4c	-20	-20	-23
59	c/2	-14	-15.5	-17
60	c/2	-12	-15	-17
61	2c	-22	-23	-24
63	3c/2	-15	-17.5	-20
65	3c/2	-15	-17.5	-20
67	3c/2	-20	-20	-24
68	c	-12	-12	-15
69	3c	-15	-15	-15
70	c	-11	-11	-16
71	c	-10	-10	-15
72	2c	-10	-10	-15
73	c	-10	-10	-15
83	c	+0	+0	+0
85	c	+0	+0	+0
86	3c	+0	+0	+0
90	5c/2	+35	+35	+35
91	9c	+0	+0	+0
114	4c	+0	+0	+0

Parameter Type Definitions

The following letter(s) specify the parameter type:

t_H	Hold Time	t_S	Setup Time
t_{PHL}	Propagation Delay Time where the output is going from HIGH to LOW	t_W	Width Time
t_{PLH}	Propagation Delay Time where the output is going from LOW to HIGH	t_T	Transition Time
t_{PD}	Propagation Delay Time where the output(s)go either HIGH or LOW orLOW to HIGH	t_{CYC}	Cycle Time
		C	Clock Period