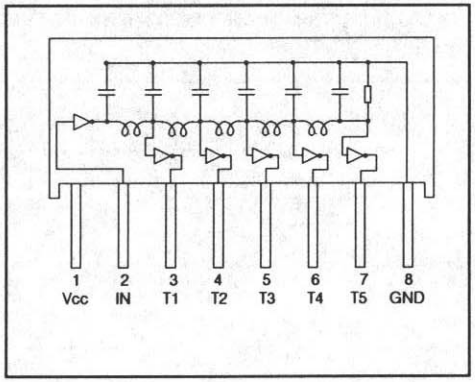
- Schottky TTL buffered
- 5 equally spaced taps
- 8 pin single-in-line package
- Low profile
- TTL compatible

SINGLE - IN - LINE PACKAGE



description

The 70A series of Digital Delay Modules are Schottky buffered delay lines providing precise delay times and direct compatibility with TTL. Five equally spaced fixed delay taps are packaged in a low profile 8 pin single-in-line configuration having an industry standard pin-out. Internal termination of the delay line and compensation for propagation delays are incorporated in the design so that no additional external components are required. These modules offer the highest density solution.

absolute maximum ratings over operating free-air temperature range

Supply voltage V_{CC} 7V
Input voltage 5.5V
Min. pulse width as % of total delay 80%
Input pulse repetition rate PRR . . . . . 3 x pulse width min.
Output rise time 6ns
Operating free-air temperature range . . . . . 0C to 70C
Storage temperature range . . . . . –55C to 125C
Temperature coefficient of delay . . . . . ±300ppm/C
Lead temperature 1.5mm from case for 10 seconds 300C

drive capabilities

Logic 0 output . . . . . 10 TTL loads per tap max.
20 TTL loads per unit max.
Logic 1 output . . . . . 20 TTL loads per unit max.

electrical specifications over operating free-air temperature range, Vcc = 5±0.25V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH} High-level input voltage		2			V
V_{IL} Low-level input voltage				0.8	V
V_{OH} High-level output voltage	V_{IH} =2V, I_{OH}=–1mA V_{CC} =4.75V	2.7	3.4		V
V_{OL} Low-level output voltage	V_{CC} =4.75V I_{OL}=20mA, V_{IL} =0.8V			0.5	V
I_{IH} High-level input current	V_{CC}=5.25V, V_{IH}=2.7V			50	μA
I_{IL} Low-level input current	V_{CC}=5.25V, V_{IL}=0.5V			–2	mA
I_{CC} Supply current outputs high	V_{CC}=5.25V			24	mA
I_{CC} Supply current outputs low	V_{CC}=5.25V			54	mA

delay characteristics Vcc = 5V, Ta = 25C, no load at taps; input test pulse voltage 3.2V, pulse width 100% of total delay, rise time 3.0ns.

delay tolerance from input to tap ±2ns or ±5% whichever is greater

70A SERIES 5 Tap 8 Pin SIP
Package style G

PART No	TOTAL DELAY (ns) ±5% (1)	TAP TO TAP (ns)	PART No	TOTAL DELAY (ns) ±5% (1)	TAP TO TAP (ns)
70A - 5200	20	4 ± 2	70A - 5101	100	20 ± 2
70A - 5250	25	5 ± 2	70A - 5125	125	25 ± 2
70A - 5300	30	6 ± 2	70A - 5151	150	30 ± 2
70A - 5400	40	8 ± 2	70A - 5175	175	35 ± 2
70A - 5500	50	10 ± 2	70A - 5201	200	40 ± 2
70A - 5600	60	12 ± 2	70A - 5251	250	50 ± 2
70A - 5750	75	15 ± 2			

Note: Delays measured at 1.5V on leading edge, Rise Time from 0.75V to 2.4V

(1) or ±2ns whichever is greater