1Mx32 3.3V FLASH MODULE

FEATURES

- Access Times of 100, 120, 150ns
- Packaging
  - 66 pin, PGA Type, 1.185" square, Hermetic Ceramic HIP (Package 401)
  - 68 lead, Low Profile CQFP (G2T), 4.6mm (0.180") square (Package 509)
- 1,000,000 Erase/Program Cycles
- Sector Architecture
  - One 16KByte, two 8KBytes, one 32KByte, and fifteen 64kBytes in byte mode
  - Any combination of sectors can be concurrently erased. Also supports full chip erase
- Organized as 1Mx32
- Commercial, Industrial and Military Temperature Ranges
- 3.3 Volt for Read and Write Operations
- Boot Code Sector Architecture (Bottom)
- Low Power CMOS, 1.0mA Standby
- Embedded Erase and Program Algorithms
- Built-in Decoupling Caps for Low Noise Operation
- Erase Suspend/Resume
  - Supports reading data from or programing data to a sector not being erased
- Low Current Consumption
  Typical values at 5MHz:
  - 40mA Active Read Current
  - 80mA Program/Erase Current
- Weight
  WF1M32B-XG2TX3 -8 grams typical
  WF1M32B-XHX3 -13 grams typical

Note: For programming information refer to Flash Programming 8M3 Application Note.

PIN CONFIGURATION FOR WF1M32B-XHX3

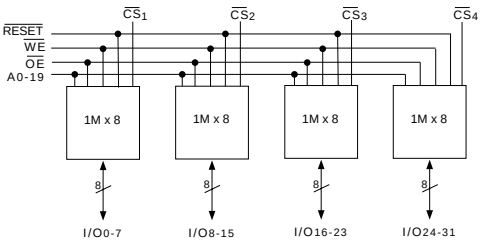
TOP VIEW

1	12	23		34	45	56
I/O8	$\overline{RESET}$	I/O15		I/O24	VCC	I/O31
I/O9	$\overline{CS}_2$	I/O14		I/O25	$\overline{CS}_4$	I/O30
I/O10	GND	I/O13		I/O26	NC	I/O29
A14	I/O11	I/O12		A7	I/O27	I/O28
A16	A10	$\overline{OE}$		A12	A4	A1
A11	A9	A17		NC	A5	A2
A0	A15	$\overline{WE}$		A13	A6	A3
A18	VCC	I/O7		A8	NC	I/O23
I/O0	$\overline{CS}_1$	I/O6		I/O16	$\overline{CS}_3$	I/O22
I/O1	A19	I/O5		I/O17	GND	I/O21
I/O2	I/O3	I/O4		I/O18	I/O19	I/O20
11	22	33		44	55	66

PIN DESCRIPTION

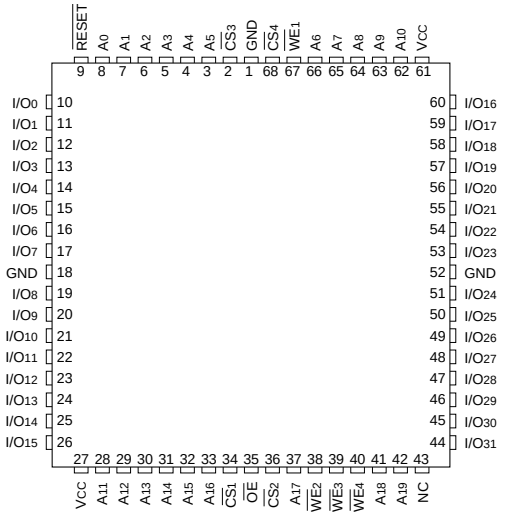
I/O0-31	Data Inputs/Outputs
A0-19	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}_{1-4}$	Chip Selects
$\overline{OE}$	Output Enable
$\overline{RESET}$	Reset
VCC	Power Supply
GND	Ground
NC	Not Connected

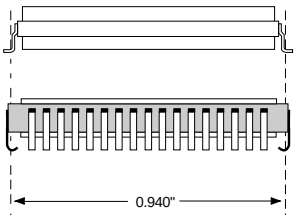
BLOCK DIAGRAM



PIN CONFIGURATION FOR WF1M32B-XG2TX3

TOP VIEW



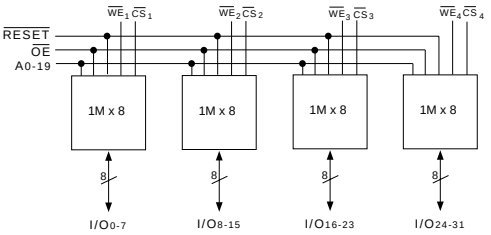


The White 68 lead G2T CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G2T has the TCE and lead inspection advantage of the CQFP form.

PIN DESCRIPTION

I/O0-31	Data Inputs/Outputs
A0-19	Address Inputs
$\overline{WE}_{1-4}$	Write Enables
$\overline{CS}_{1-4}$	Chip Selects
$\overline{OE}$	Output Enable
$\overline{RESET}$	Reset/Powerdown
VCC	Power Supply
GND	Ground

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter		Unit
Operating Temperature	-55 to +125	°C
Supply Voltage Range (V_{CC})	-0.5 to +4.0	V
Signal Voltage Range	-0.5 to Vcc +0.5	V
Storage Temperature Range	-65 to +150	°C
Lead Temperature (soldering, 10 seconds)	+300	°C
Endurance (write/erase cycles)	1,000,000 min.	cycles

NOTES:
1. Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

CAPACITANCE

(T_A = +25°C)

Parameter	Symbol	Conditions	Max	Unit
$\overline{OE}$ capacitance	C_{OE}	V_{IN} = 0 V, f = 1.0 MHz	50	pF
$\overline{WE}_{1-4}$ capacitance	C_{WE}	V_{IN} = 0 V, f = 1.0 MHz	20	pF
CS_{1-4} capacitance	C_{CS}	V_{IN} = 0 V, f = 1.0 MHz	20	pF
Data I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V, f = 1.0 MHz	20	pF
Address input capacitance	C_{AD}	V_{IN} = 0 V, f = 1.0 MHz	50	pF

This parameter is guaranteed by design but not tested.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	3.0	3.6	V
Input High Voltage	V_{IH}	0.7 x Vcc	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	-0.5	+0.8	V
Operating Temp. (Mil.)	T_A	-55	+125	°C
Operating Temp. (Ind.)	T_A	-40	+85	°C

DATA RETENTION

Parameter	Test Conditions	Min	Unit
Minimum Pattern Data Retention Time	150°C	10	Years
	125°C	20	Years

DC CHARACTERISTICS - CMOS COMPATIBLE

(V_{CC} = 3.3V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	Conditions	Min	Max	Unit
Input Leakage Current	I_{LI}	V_{CC} = 3.6, V_{IN} = GND or V_{CC}		10	µA
Output Leakage Current	I_{LOx32}	V_{CC} = 3.6, V_{IN} = GND or V_{CC}		10	µA
V_{CC} Active Current for Read (1)	I_{CC1}	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, f = 5MHz		120	mA
V_{CC} Active Current for Program or Erase (2)	I_{CC2}	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}		140	mA
V_{CC} Standby Current	I_{CC3}	V_{CC} = 3.6, CS = V_{IH}, f = 5MHz		200	µA
Output Low Voltage	V_{OL}	I_{OL} = 5.8 mA, V_{CC} = 3.0		0.45	V
Output High Voltage	V_{OH1}	I_{OH} = -2.0 mA, V_{CC} = 3.0	0.85 x V_{CC}		V
Low V_{CC} Lock-Out Voltage (4)	V_{LKO}		2.3	2.5	V

NOTES:
1. The I_{CC} current listed includes both the DC operating current and the frequency dependent component (at 5 MHz). The frequency component typically is less than 8 mA/MHz, with $\overline{OE}$ at V_{IH}.
2. I_{CC} active while Embedded Algorithm (program or erase) is in progress.
3. DC test conditions: V_{IL} = 0.3V, V_{IH} = V_{CC} - 0.3V
4. Guaranteed by design, but not tested.

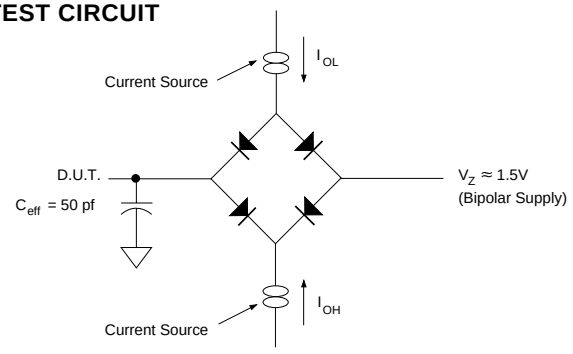
AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS, $\overline{CS}$ CONTROLLED

(V_{CC} = 3.3V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol		-100		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{AVAV}	t_{WC}	100		120		150		ns
Write Enable Setup Time	t_{WLEL}	t_{WS}	0		0		0		ns
Chip Select Pulse Width	t_{ELEH}	t_{CP}	45		50		50		ns
Address Setup Time	t_{AVEL}	t_{AS}	0		0		0		ns
Data Setup Time	t_{DVEH}	t_{DS}	45		50		50		ns
Data Hold Time	t_{EHDX}	t_{DH}	0		0		0		ns
Address Hold Time	t_{ELAX}	t_{AH}	45		50		50		ns
Chip Select Pulse Width High	t_{EHEL}	t_{CPH}	20		20		20		ns
Duration of Byte Programming Operation (1)	t_{WHWH1}			300		300		300	µs
Sector Erase Time	t_{WHWH2}			15		15		15	sec
Read Recovery Time (2)	t_{GHEL}		0		0		0		µs
Chip Programming Time				50		50		50	sec

1. Typical value for t_{WHWH1} is 9µs.
2. Guaranteed by design, but not tested.

AC TEST CIRCUIT



AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	V_{IL} = 0, V_{IH} = 2.5	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:
V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z_0 = 75 Ω.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS - $\overline{WE}$ CONTROLLED

(V_{CC} = 3.3V, T_A = -55°C to +125°C)

Parameter	Symbol		-100		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{AVAV}	t_{WC}	100		120		150		ns
Chip Select Setup Time	t_{ELWL}	t_{CS}	0		0		0		ns
Write Enable Pulse Width	t_{WLWH}	t_{WP}	50		50		65		ns
Address Setup Time	t_{AVWL}	t_{AS}	0		0		0		ns
Data Setup Time	t_{DVWH}	t_{DS}	50		50		65		ns
Data Hold Time	t_{WHDX}	t_{DH}	0		0		0		ns
Address Hold Time	t_{WLAX}	t_{AH}	50		50		65		ns
Write Enable Pulse Width High	t_{WHWL}	t_{WPH}	30		30		35		ns
Duration of Byte Programming Operation (1)	t_{WHWH1}			300		300		300	µs
Sector Erase	t_{WHWH2}			15		15		15	sec
Read Recovery Time before Write (3)	t_{GHWL}		0		0		0		µs
V_{CC} Setup Time	t_{VCS}		50		50		50		µs
Chip Programming Time				50		50		50	sec
Output Enable Setup Time		t_{OES}	0		0		0		ns
Output Enable Hold Time (2)		t_{OEH}	10		10		10		ns

1. Typical value for t_{WHWH1} is 9µs.
2. For Toggle and Data Polling.
3. Guaranteed by design, but not tested.

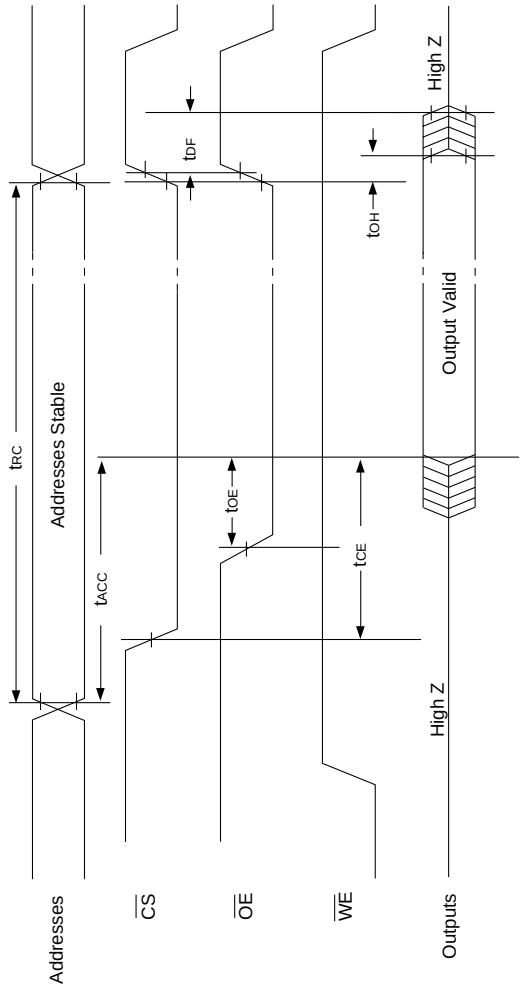
AC CHARACTERISTICS – READ-ONLY OPERATIONS

(V_{CC} = 3.3V, T_A = -55°C to +125°C)

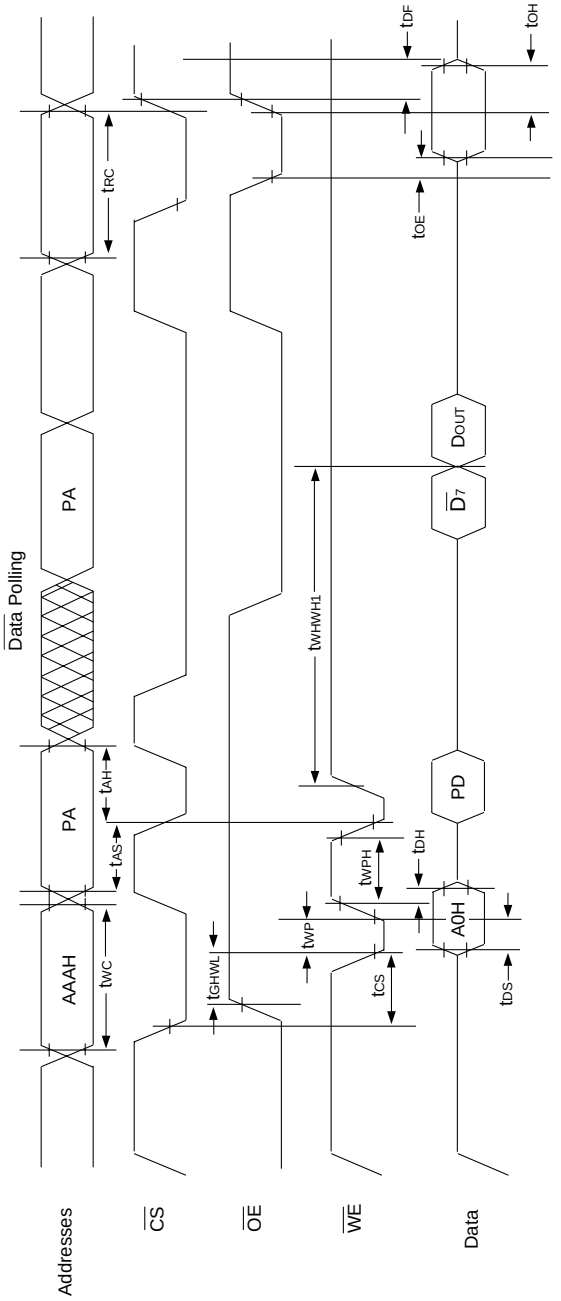
Parameter	Symbol		-100		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{AVAV}	t_{RC}	100		120		150		ns
Address Access Time	t_{AVQV}	t_{ACC}		100		120		150	ns
Chip Select Access Time	t_{ELQV}	t_{CE}		100		120		150	ns
Output Enable to Output Valid	t_{GLQV}	t_{OE}		40		50		55	ns
Chip Select High to Output High Z (1)	t_{EHQZ}	t_{DF}		30		30		40	ns
Output Enable High to Output High Z (1)	t_{GHQZ}	t_{DF}		30		30		40	ns
Output Hold from Addresses, $\overline{CS}$ or $\overline{OE}$ Change, whichever is First	t_{AXQX}	t_{OH}	0		0		0		ns

1. Guaranteed by design, not tested.

AC WAVEFORMS FOR READ OPERATIONS



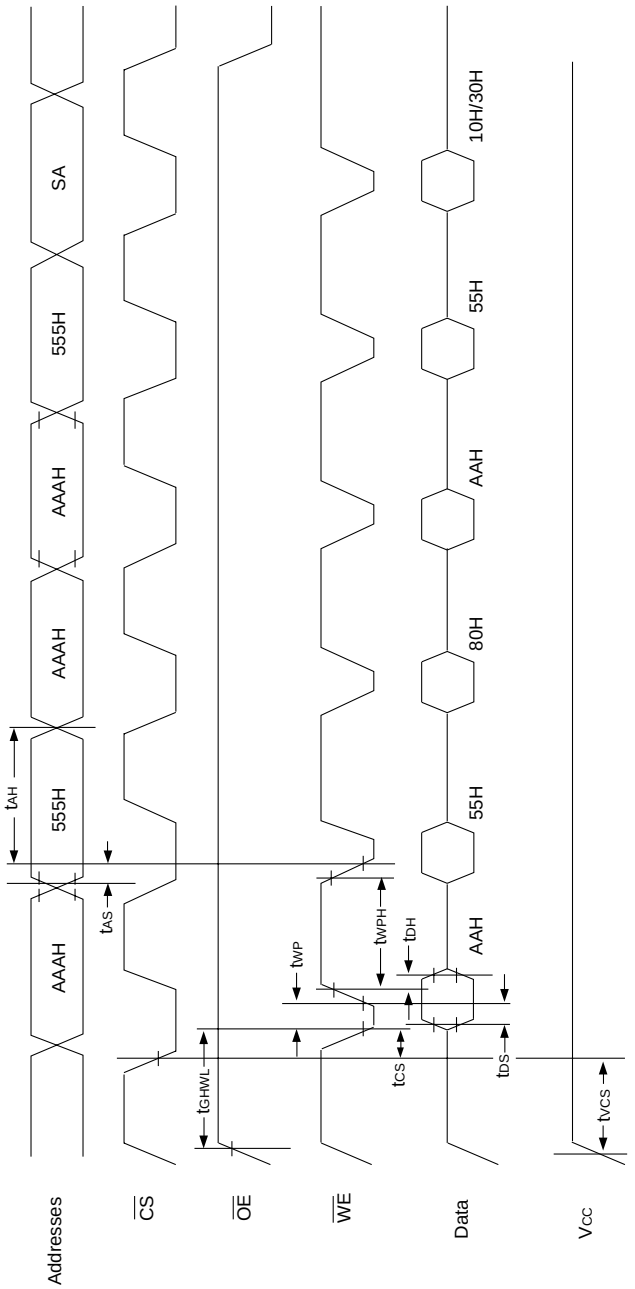
WRITE/ERASE/PROGRAM OPERATION, $\overline{WE}$ CONTROLLED



NOTES:

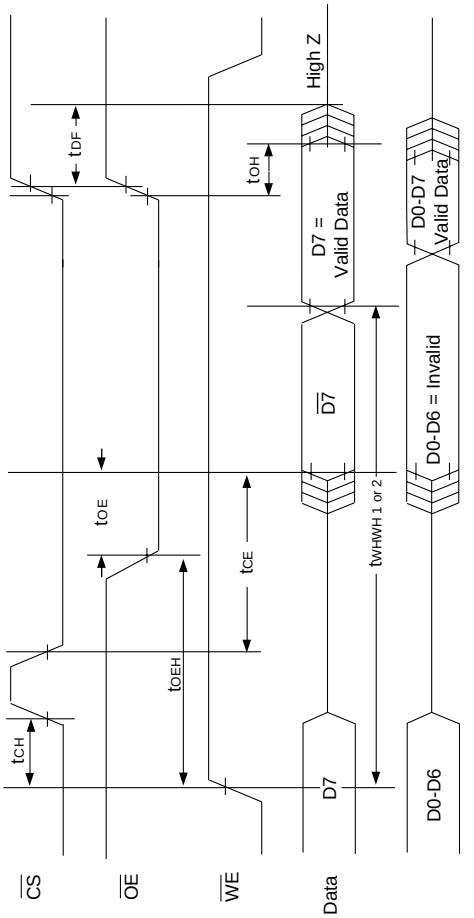
1. PA is the address of the memory location to be programmed.
2. PD is the data to be programmed at byte address.
3. $\overline{D_7}$ is the output of the complement of the data written to each chip.
4. D_{OUT} is the output of the data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.

AC WAVEFORMS CHIP/SECTOR ERASE OPERATIONS

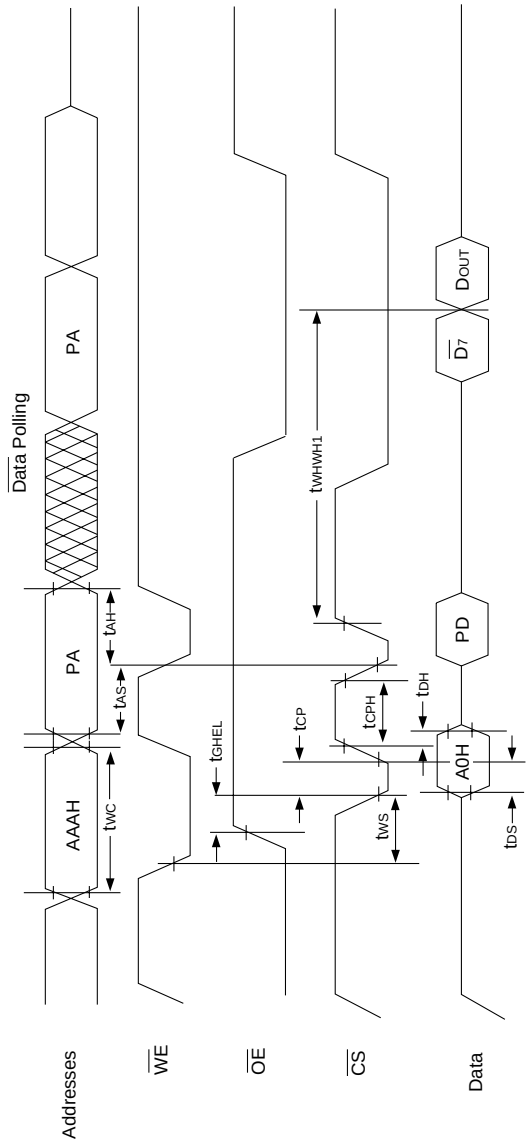


NOTE:
1. SA is the sector address for Sector Erase.

AC WAVEFORMS FOR $\overline{\text{DATA}}$ POLLING DURING EMBEDDED ALGORITHM OPERATIONS



ALTERNATE $\overline{CS}$ CONTROLLED PROGRAMMING OPERATION TIMINGS



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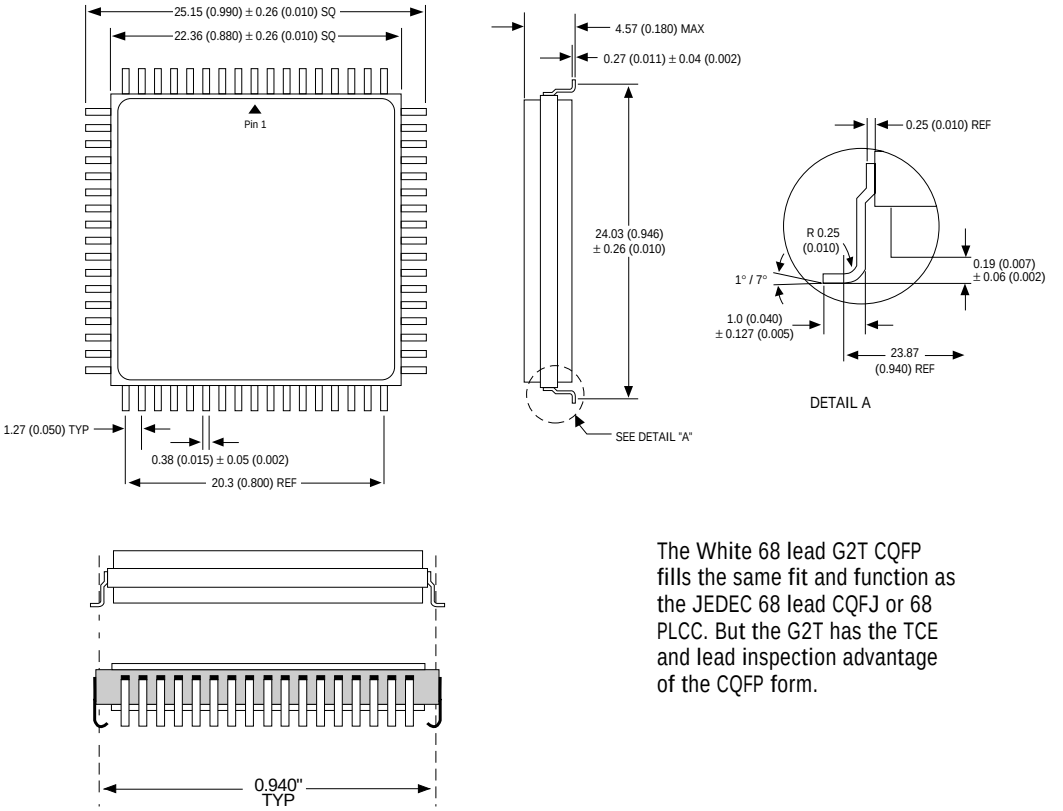
PACKAGE 509: 68 LEAD, LOW PROFILE CERAMIC QUAD FLAT PACK, CQFP (G2T)



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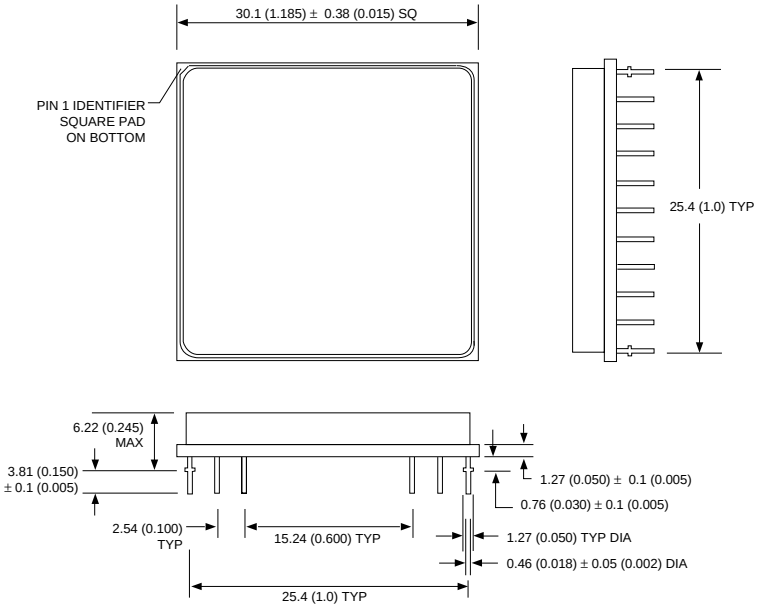
ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE 401: 66 PIN, PGA TYPE, CERAMIC HEX-IN-LINE PACKAGE, HIP (H)



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ORDERING INFORMATION

W F 1M32 B - XXX X X 3 X

LEAD FINISH:
- Blank = Gold plated leads
- A = Solder dip leads

PROGRAMMING VOLTAGE
- 3 = 3.3V

DEVICE GRADE:

M =	Military Screened	-55°C to +125°C
I =	Industrial	-40°C to +85°C
C =	Commercial	0°C to +70°C

PACKAGE TYPE:
- H = Ceramic Hex In line Package, HIP (Package 401)
- G2T = 22mm Ceramic Quad Flat Pack, Low Profile CQFP (Package 509)

ACCESS TIME (ns)

IMPROVEMENT MARK
- B = Boot Block (Bottom Sector)

ORGANIZATION, 1M x 32
- User configurable as 2M x 16 or 4M x 8

Flash

WHITE ELECTRONIC DESIGNS CORP.