1.25-micron Gate Arrays

Array	Useable Gates	Programmable			Power Pins
		TAB	Fine Pitch	Standard Pitch	
GC100K	51,320	436	330	260	12
GC 50K	26,266	312	232	184	12
GC 40K	17,496	260	194	154	12
GC 30K	16,280	246	182	142	12
GC 25K	13,122	220	166	134	12
GC 20K	10,714	196	144	116	12
GC 15K	7,560	168	128	100	12
GC 10K	5,264	136	104	84	12
GC 7K	3,526	116	86	68	12
GC 5K	2,692	98	72	56	12
GC 3K	1,286	72	52	40	12

Standard Cell Circuits

Analog and digital building blocks offer higher density and smaller size for medium to high volume needs

- 1.0 and 1.25-micron Double Metal CMOS Families.
- 3-micron and 2-micron Double Poly, Double Metal CMOS Families
- Cells Created by Expert-based Cell Generator
- Basic Logic, Interface, MSI, 7400 and Megacell Functions
- 2-micron Process includes Analog Functions
- Tailor-made RAMs, ROMs and PLAs Available
- Artificial Intelligence Software Services Available for Digital Netlist Translation and Gate Reduction

Chips designed with these cells, offered in analog and digital formats, surpass gate array density and approach that of cell-based custom designs at half the development cost and development time. They're cost effective for medium to high-volume production.

Standard cells are pre-designed circuit building blocks whose functional, timing and performance parameters exist in Gould AMI's libraries. As with a gate array, you design a standard cell circuit by choosing logic functions from a library installed on a CAE workstation. But while a gate array design specifies only the final metal layers of a pre-fabricated silicon base, all of a standard cell's base and metal layers are custom fabricated from pre-characterized cells. This feature gives standard cells greater design flexibility, but requires an eight week development time.

A standard cell circuit also uses only the number of cells required for a design, whereas gate arrays seldom utilize all of the available cells. This means a smaller die size and lower cost to you for a given circuit function.

Gould AMI offers over 850 cells in its four standard cell families:

- 1.0-micron digital CMOS (CYX Family).
- 1.25-micron digital CMOS (CAB Family).
- 3-micron analog and digital CMOS (CCI Family).
- 2-micron analog and digital CMOS (ABX Family).

Digital Standard Cells

Both the CAB and CYX families use a double metal, single poly, twin tub CMOS process. They are intended primarily for 5 Volt operation but will operate down to 2.5 Volts.