CA3050, CA3051

Dual Differential Amplifiers

Two Darlington-Connected Differential Amplifiers with Diode Bias String

For Low-Power Applications at Frequencies from DC to 20 MHz

Features:

- *Input offset current - 70 nA max.*
- *Input bias current - 500 nA max.*
- *Input offset voltage - 5 mV max.*
- *Input impedance - 460 kΩ typ.*
- *Independently accessible inputs and outputs*

The CA3050 and CA3051 each consists of two differential amplifiers with associated constant current transistors on a common substrate. Each amplifier is driven by Darlington-connected emitter follower inputs to provide high input impedance, low bias current, and low offset current. A string of diodes is included to provide temperature-compensated bias to the constant current transistors and a low impedance bias point for the inputs to the differential amplifiers when a single power supply is used.

The CA3050 is supplied in an hermetic 14-lead Dual-In-Line ceramic package rated for operation over the full military temperature range of −55°C to +125°C.

The CA3051 is supplied in a Dual-In-Line plastic package for applications requiring only a limited temperature range of −25°C to +85°C.

Applications

- *Matched dual amplifiers*
- *Dual sense amplifiers*
- *Dual Schmitt triggers*
- *Dual multivibrators*
- *Doubly balanced detectors and modulators*
- *Balanced quadrature detectors*
- *Synthesizer mixers*
- *Product detectors*

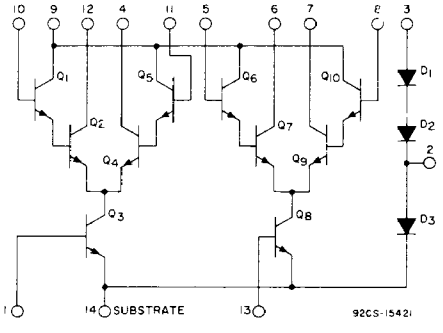


Fig. 1 — Schematic diagram.

CA3049, CA3102

MAXIMUM RATINGS, ABSOLUTE-MAXIMUM VALUES, AT T_A = 25°C

	CA3050	CA3051	
Power Dissipation, P:			
Any one transistor	150	150	mW
Total package	900	750	mW
For $T_A > 55°C$, Derate at	8	6.67	mW/°C
Temperature Range:			
Operating	-55 to +125	-40 to +85	°C
Storage	-65 to +150	-65 to +150	°C
LEAD TEMPERATURE (During Soldering) At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max.	+265°C		

The following ratings apply for each transistor in the device:

Collector-to-Emitter Voltage, V_{CEO}	15	V
Collector-to-Base Voltage, V_{CBO}	20	V
Collector-to-Substrate Voltage, V_{CIO}*	20	V
Emitter-to-Base Voltage, V_{EBO}	5	V
Collector Current, I_C	50	mA

* The collector of each transistor of the CA3050 and CA3051 is isolated from the substrate by an integral diode. *The substrate (terminal 14) must be more negative than all collectors to maintain isolation between transistors and to provide for normal transistor action.*

MAXIMUM VOLTAGE RATINGS

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range between vertical terminal 2 and horizontal terminal 3 is +5 to -2 volts.

TERMINAL No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14
1	–	*	*	*	*	*	*	*	*	*	*	*	*	+1 -5
2			+5 -2	*	*	*	*	*	*	*	*	*	*	+1 -1
3				*	*	*	*	*	*	*	*	*	*	+3 -1
4					*	*	*	*	*	+14 -2.5 Note 3	+14 -2.5 Note 4	*	*	+20 -1
5						+2.5 -14 Note 1	+2.5 -14 Note 1	+10 -10	+1 -20	*	*	*	*	+16 -
6							*	+14 -2.5 Note 2	*	*	*	*	*	+20 -1
7								+14 -2.5 Note 2	*	*	*	*	*	+20 -1
8									+1 -20	*	*	*	*	+16 -
9										+20 -1	+20 -1	*	*	+20 -1
10											+10 -10	+2.5 -14 Note 3	*	+16 -
11												+2.5 -14 Note 4	*	+16 -
12														+20 -1
13														+1 -5
14														Ref. Substrate

MAXIMUM CURRENT RATINGS

TERMINAL No.	I_{IN} mA	I_{OUT} mA
1	5	0.1
2	50	50
3	50	1
4	50	1
5	5	0.1
6	50	1
7	50	1
8	5	0.1
9	50	1
10	5	0.1
11	5	0.1
12	50	1
13	5	0.1
14	100	5

Note 1: This rating is important only when terminal 5 is more positive than terminal 8.

Note 2: This rating is important only when terminal 8 is more positive than terminal 5.

Note 3: This rating is important only when terminal 10 is more positive than terminal 11.

Note 4: This rating is important only when terminal 11 is more positive than terminal 10.

* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	TEST CIR-CUIT	LIMITS CA3050/CA3051			UNITS	TYPICAL CHARAC-TERISTICS CURVES
			FIG.	MIN.	TYP.	MAX.		FIG.
STATIC								
Amplifier Characteristics								
Input Offset Voltage	V_{IO}		–	–	1.5	5	mV	2a,b
Input Offset Current	I_{IO}		–	–	7	70	nA	3a,b
Input Bias Current	I_I		–	–	200	500	nA	4a,b
Quiescent Operating Current Ratio	$\left\lvert \frac{(I_4+I_{12})}{I_3} \text{ or } \frac{(I_6+I_7)}{I_3} \right\rvert$	V_{CC} = + 6 V, I_3 = 2 mA	–	0.9	1.00	1.13	–	5a,b
DC Forward Base-to-Emitter Voltage	V_{BE}	V_{CE} = 3 V, I_C = 50 μA	–	–	0.645	0.700	V	6
		V_{CE} = 3 V, I_C = 1 mA	–	–	0.725	0.800		
		V_{CE} = 3 V, I_C = 3 mA	–	–	0.760	0.850		
		V_{CE} = 3 V, I_C = 10 mA	–	–	0.805	0.900		
Temperature Coefficient of Base-to-Emitter Voltage	$\frac{\Delta V_{BE}}{\Delta T}$	V_{CE} = 3 V, I_C = 1 mA	–	–	-1.9	–	mV/°C	7
Transistor Characteristics								
Collector-Cutoff Current	I_{CBO}	V_{CB} = 10 V, I_E = 0	–	–	0.002	100	nA	8
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1 mA, I_B = 0	–	15	24	–	V	–
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10 μA, I_E = 0	–	20	60	–	V	–
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_C = 10 μA, I_{CI} = 0	–	20	60	–	V	–
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10 μA, I_C = 0	–	5	7	–	V	–
DYNAMIC								
Transistor Characteristics								
Emitter-to-Base Capacitance	C_{EB}	V_{EB} = 3 V, I_E = 0	–	–	0.78	–	pF	9
Collector-to-Base Capacitance	C_{CB}	V_{CB} = 3 V, I_C = 0	–	–	0.47	–	pF	9
Collector-to-Substrate Capacitance	C_{CI}	V_{CS} = 3 V, I_C = 0	–	–	1.92	–	pF	9
Amplifier Characteristics								
Gain-Bandwidth Product (For Single Transistor)	f_T	V_{CE} = 5 V, I_C = 3 mA	–	–	600	–	MHz	10
Forward Transadmittance (With single-ended input and output)	$\lvert y_{21} \rvert$	V_{CC} = 10 V, I_3 = 2 mA f = 1 MHz	11	7	9	11	mmho	11
Bandwidth at -3 dB Point	BW	V_{CC} = 10 V, I_3 = 2 mA	11	–	4.3	–	MHz	11
Input Impedance	Z_{IN}	V_{CC} = 10 V, I_3 = 2 mA f = 1 KHz	12	–	460	–	kΩ	12
Output Impedance	Z_{OUT}	I_3 = 2 mA, f = 1 KHz	13	–	170	–	kΩ	13
Common-Mode Rejection Ratio	CMR	I_3 = 2 mA, f = 1 KHz	–	–	65	–	dB	–
AGC Range	AGC	I_3 = 2 mA, f = 1 KHz Terminal No.3 Grounded	11	–	60	–	dB	–

CA3050, CA3051

TYPICAL STATIC CHARACTERISTICS

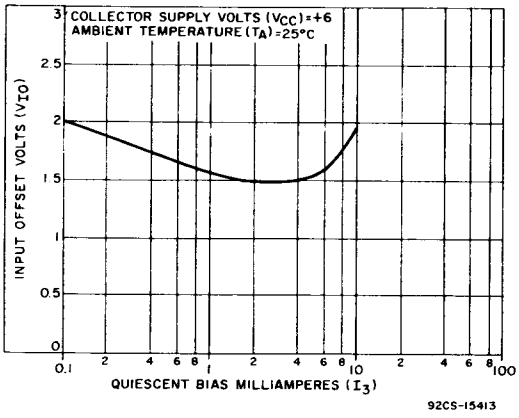


Fig.2(a) - Typical input offset voltage vs quiescent bias current.

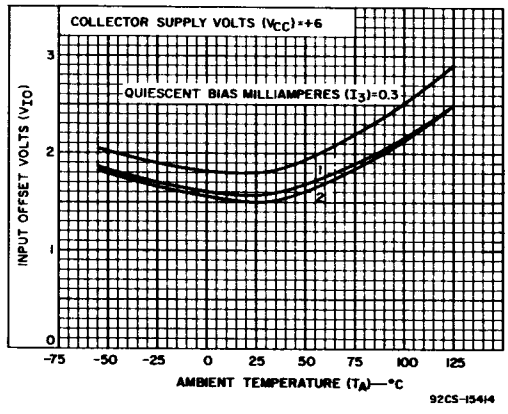


Fig.2(b) - Typical input offset voltage vs ambient temperature.

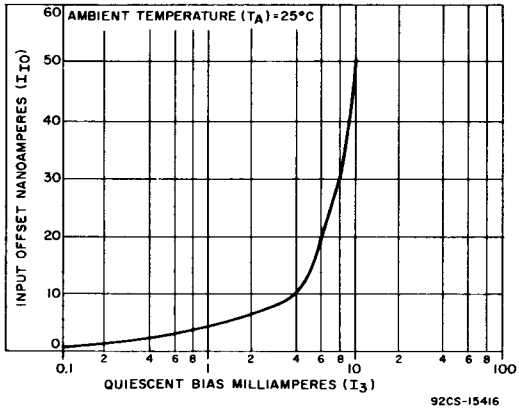


Fig.3(a) - Typical input offset current vs quiescent bias current.

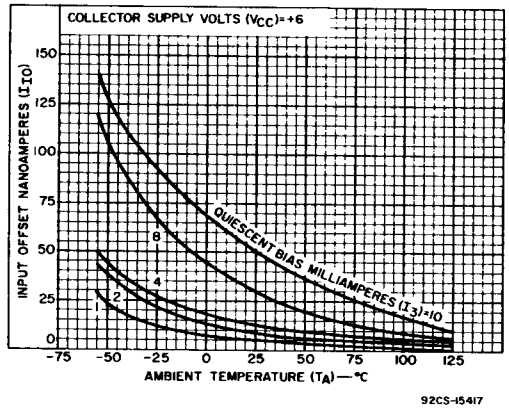


Fig.3(b) - Typical input offset current vs ambient temperature.

STATIC CHARACTERISTICS

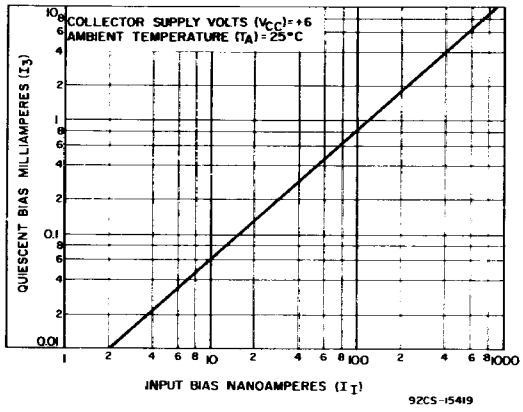


Fig.4(a) - Typical quiescent bias current vs input bias current.

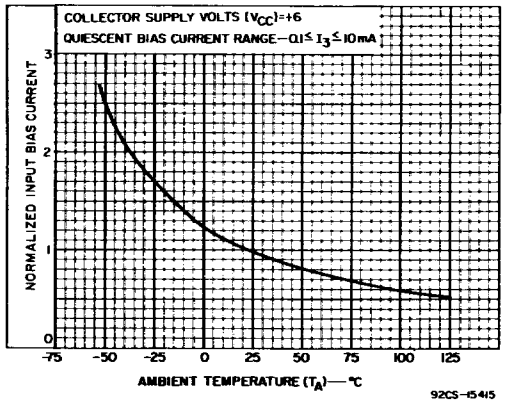


Fig.4(b) - Typical normalized input bias current vs ambient temperature.

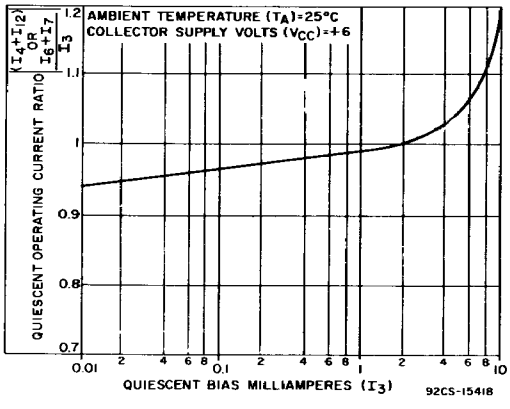


Fig.5(a) - Typical quiescent operating current ratio vs quiescent bias current.

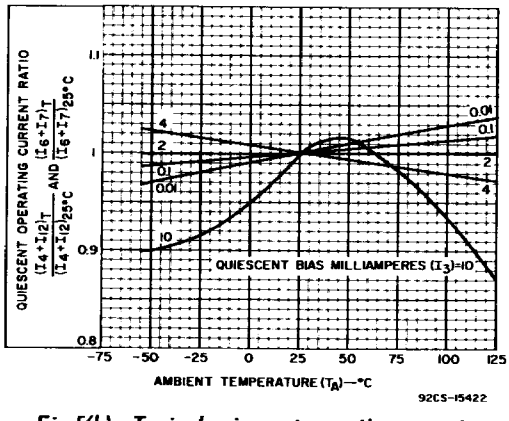


Fig.5(b) - Typical quiescent operating current ratio vs ambient temperature.

CA3050, CA3051

STATIC CHARACTERISTICS

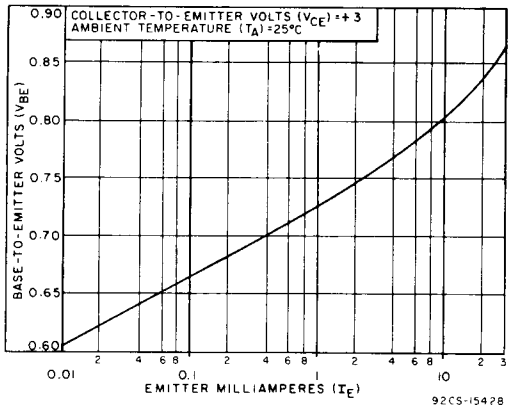


Fig.6 - Typical static base-to-emitter voltage characteristic vs emitter current for all transistors and forward diode voltage drops.

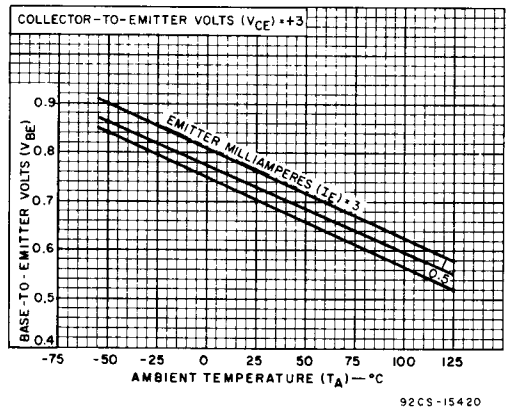


Fig.7 - Typical base-to-emitter voltage characteristic vs ambient temperature for each transistor.

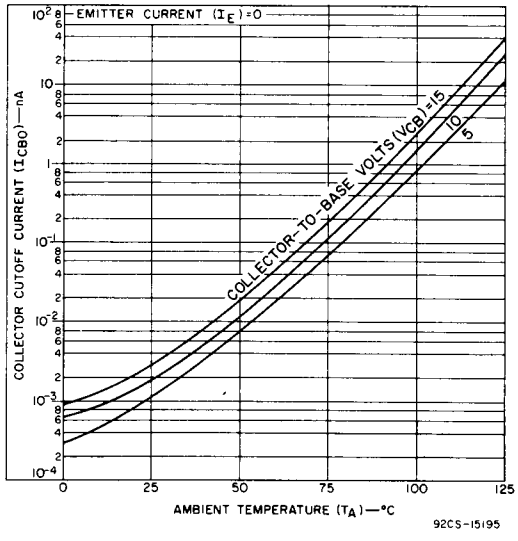


Fig.8 - Typical collector-to-base cutoff current vs ambient temperature for each transistor.

DYNAMIC CHARACTERISTICS FOR EACH TRANSISTOR

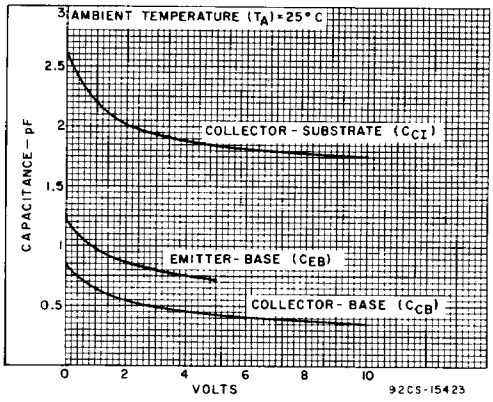


Fig.9 - Typical capacitance for each transistor.

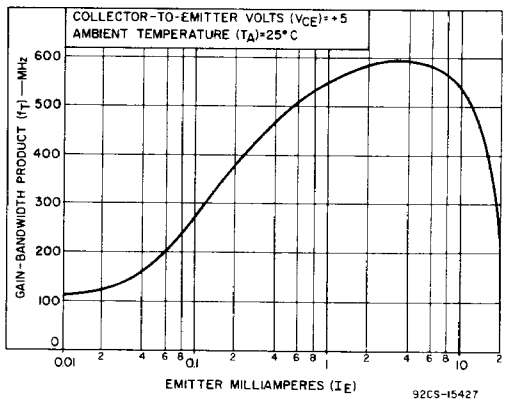
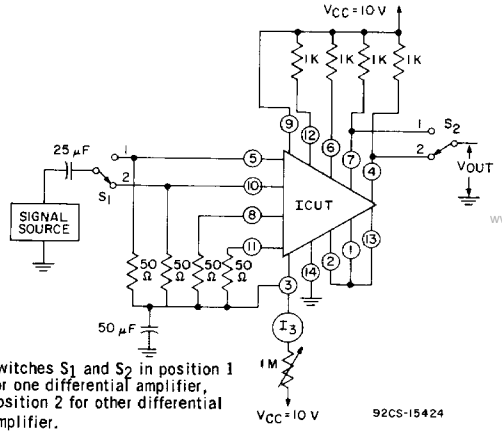


Fig.10 - Typical gain-bandwidth product (f_T) for each transistor vs emitter current.



Switches S_1 and S_2 in position 1 for one differential amplifier, position 2 for other differential amplifier.

Fig.11(a) - Test circuit for forward transadmittance, -3 dB bandwidth, and AGC range.

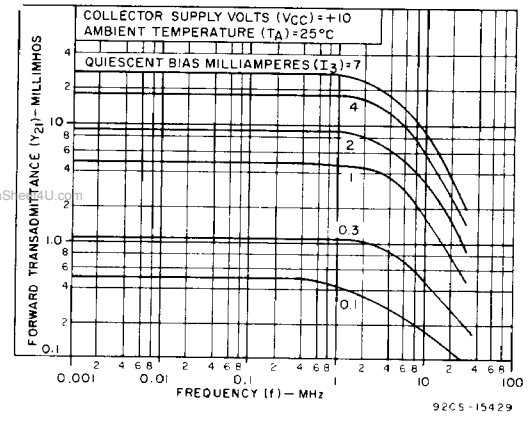


Fig.11(b) - Typical differential amplifier forward transadmittance with single-ended output vs frequency.

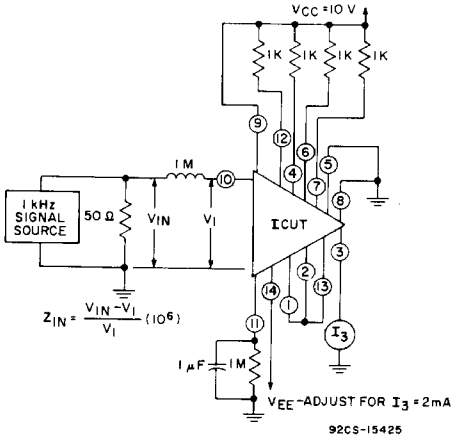


Fig.12(a) - Test circuit for input impedance.

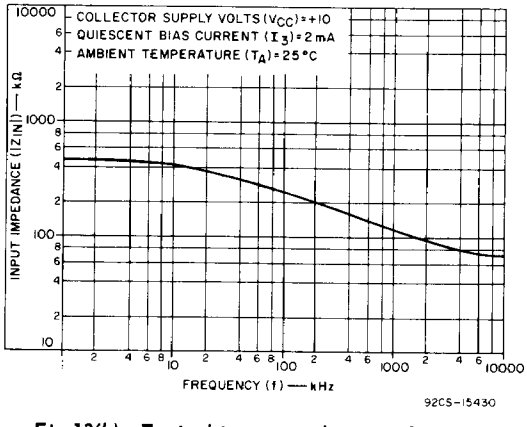
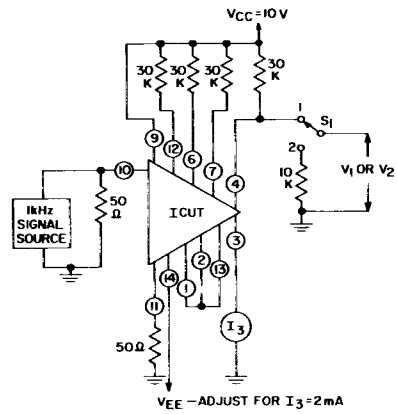


Fig.12(b) - Typical input impedance vs frequency with output short-circuited.

CA3050, CA3051

DYNAMIC CHARACTERISTICS FOR EACH TRANSISTOR



$$Z_{OUT} = \frac{(30K \times 10K)\frac{V_2}{V_1}}{\frac{V_2}{V_1}(30K+10K)-10K}$$

Fig.13(a) - Test circuit for output impedance.

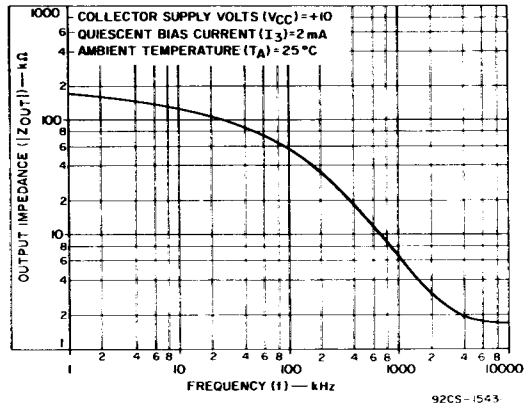


Fig.13(b) - Typical output impedance vs frequency with input short-circuited.