



12N50

Preliminary

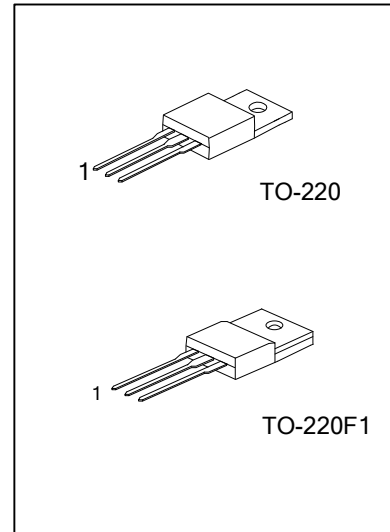
Power MOSFET

12 Amps, 500 Volts N-CHANNEL POWER MOSFET

DESCRIPTION

The UTC **12N50** is an N-channel mode power MOSFET using UTC's advanced technology to provide customers with planar stripe and DMOS technology. This technology allows a minimum on-state resistance and superior switching performance. It also can withstand high energy pulse in the avalanche and commutation mode.

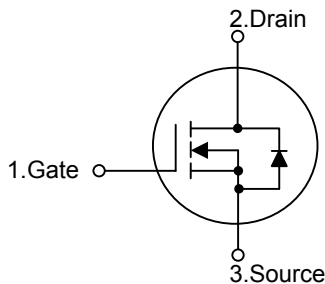
The UTC **12N50** is generally applied in high efficiency switch mode power supplies, active power factor correction and electronic lamp ballasts based on half bridge topology.



FEATURES

- * 12A, 500V, $R_{DS(ON)}=0.54\Omega @ V_{GS}=10V$
- * High Switching Speed
- * 100% Avalanche Tested

SYMBOL



ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
12N50L-TA3-T	12N50G-TA3-T	TO-220	G	D	S	Tube
12N50L-TF1-T	12N50G-TF1-T	TO-220F1	G	D	S	Tube

Note: Pin Assignment: G: Gate D: Drain S: Source

12N50L-TA3-T	(1)Packing Type	(1) T: Tube
	(2)Package Type	(2) TA3: TO-220 ,TF1: TO-220F1
	(3)Lead Free	(3) G: Halogen Free, L: Lead Free

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■ ABSOLUTE MAXIMUM RATINGS ($T_C=25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	500	V
Gate-Source Voltage		V_{GSS}	± 30	V
Drain Current	Continuous ($T_C=25^\circ\text{C}$)	I_D	12 *	A
	Pulsed (Note 1)	I_{DM}	48 *	A
Avalanche Current (Note 1)		I_{AR}	12	A
Avalanche Energy	Single Pulsed (Note 2)	E_{AS}	684	mJ
	Repetitive (Note 3)	E_{AR}	19.5	mJ
Peak Diode Recovery dv/dt (Note 3)		dv/dt	4.5	V/ns
Power Dissipation	$T_C=25^\circ\text{C}$	TO-220	192	W
		TO-220F1	42	
	Derate above 25°C	TO-220	1.53	W/ $^\circ\text{C}$
		TO-220F1	0.33	
Junction Temperature		T_J	+150	$^\circ\text{C}$
Storage Temperature		T_{STG}	-55~+150	$^\circ\text{C}$

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

* Drain current limited by maximum junction temperature

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	TO-220	θ_{JA}	62.5	$^\circ\text{C/W}$
	TO-220F1		62.5	
Junction to Case	TO-220	θ_{JC}	0.65	$^\circ\text{C/W}$
	TO-220F1		3.0	

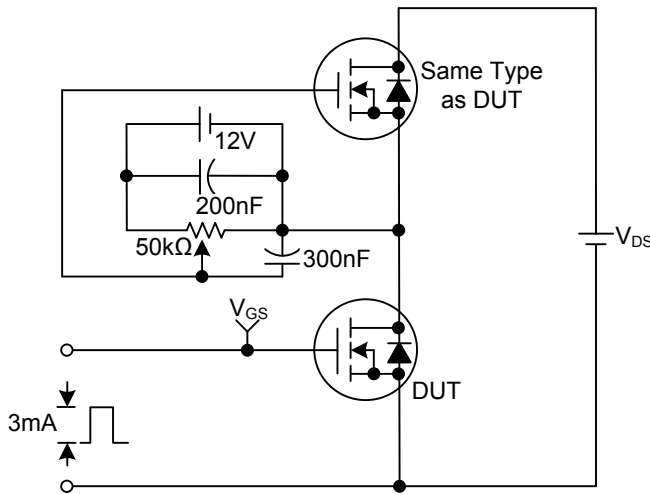
■ ELECTRICAL CHARACTERISTICS ($T_c=25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	500			V
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=500\text{V}$, $V_{GS}=0\text{V}$			1	μA
Gate- Source Leakage Current	Forward	$V_{GS}=+30\text{V}$, $V_{DS}=0\text{V}$			+100	nA
	Reverse	$V_{GS}=-30\text{V}$, $V_{DS}=0\text{V}$			-100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	2.0		4.0	V
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10\text{V}$, $I_D=6\text{A}$		0.42	0.54	Ω
DYNAMIC PARAMETERS						
Input Capacitance	C_{ISS}	$V_{GS}=0\text{V}$, $V_{DS}=25\text{V}$, $f=1.0\text{MHz}$		1450	1930	pF
Output Capacitance	C_{OSS}			198	265	pF
Reverse Transfer Capacitance	C_{RSS}			14.5	22	pF
SWITCHING PARAMETERS						
Total Gate Charge	Q_G	$V_{GS}=10\text{V}$, $V_{DS}=400\text{V}$, $I_D=12\text{A}$ (Note 4, 5)		30	39	nC
Gate to Source Charge	Q_{GS}			8		nC
Gate to Drain Charge	Q_{GD}			12		nC
Turn-ON Delay Time	$t_{D(ON)}$	$V_{DD}=250\text{V}$, $I_D=12\text{A}$, $R_G=25\Omega$ (Note 4, 5)		28	65	ns
Rise Time	t_R			54	120	ns
Turn-OFF Delay Time	$t_{D(OFF)}$			75	160	ns
Fall-Time	t_F			47	105	ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Maximum Body-Diode Continuous Current	I_S				12	A
Maximum Body-Diode Pulsed Current	I_{SM}				48	A
Drain-Source Diode Forward Voltage	V_{SD}	$I_S=12\text{A}$, $V_{GS}=0\text{V}$			1.5	V
Body Diode Reverse Recovery Time	t_{RR}	$I_S=12\text{A}$, $V_{GS}=0\text{V}$, $di/dt=100\text{A}/\mu\text{s}$ (Note 4)		154		ns
Body Diode Reverse Recovery Charge	Q_{RR}			0.45		μC

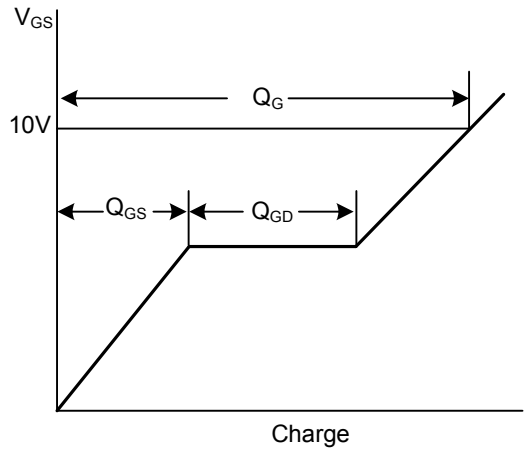
- Notes: 1. Repetitive Rating: Pulse width limited by maximum junction temperature
 2. $L=9.5\text{mH}$, $I_{AS}=12\text{A}$, $V_{DD}=50\text{V}$, $R_G=25\Omega$, Starting $T_J=25^\circ\text{C}$
 3. $I_{SD}\leq 12\text{A}$, $di/dt\leq 200\text{A}/\mu\text{s}$, $V_{DD}\leq BV_{DSS}$, Starting $T_J=25^\circ\text{C}$
 4. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$
 5. Essentially independent of operating temperature

■ TEST CIRCUITS AND WAVEFORMS

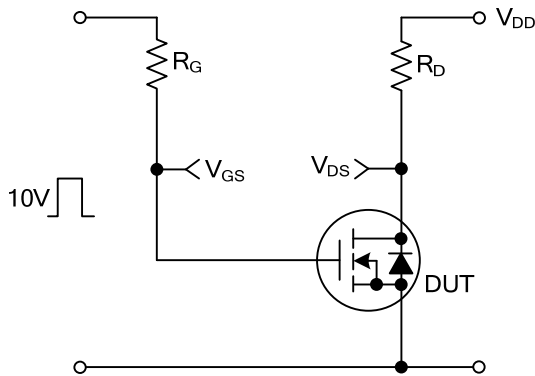
Gate Charge Test Circuit



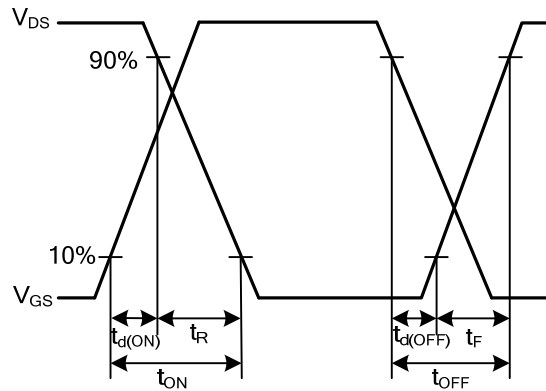
Gate Charge Waveforms



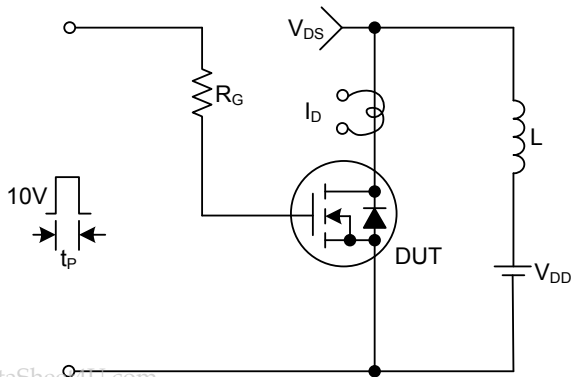
Resistive Switching Test Circuit



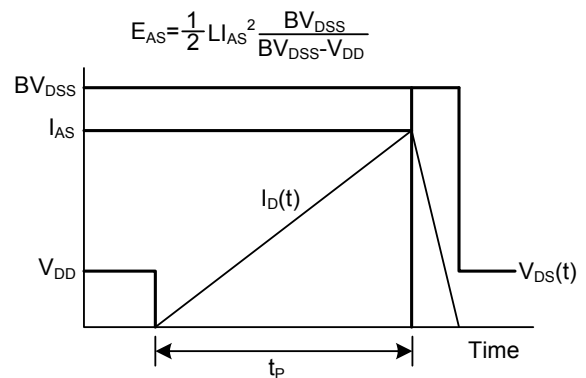
Resistive Switching Waveforms



Unclamped Inductive Switching Test Circuit

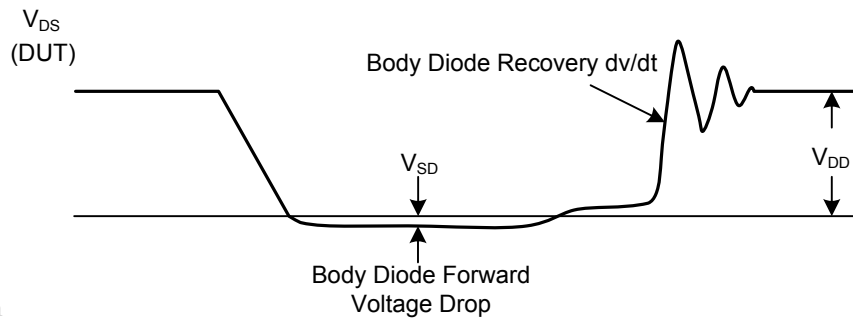
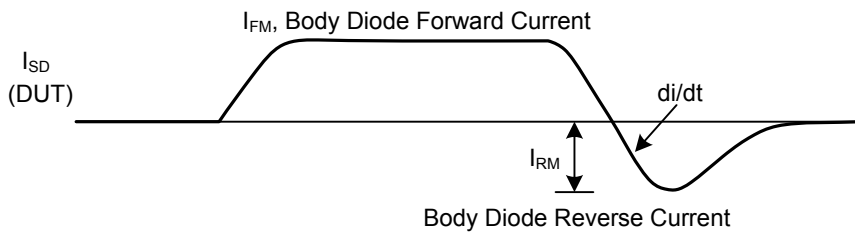
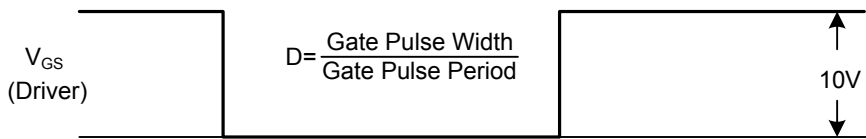
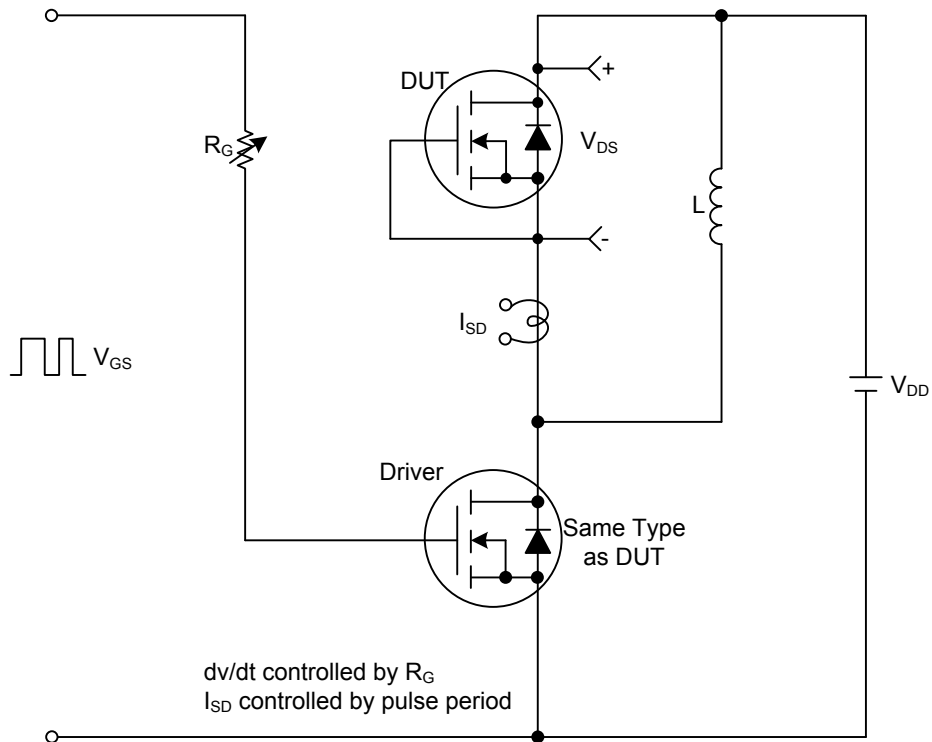


Unclamped Inductive Switching Waveforms



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Peak Diode Recovery dv/dt Test Circuit & Waveforms



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