MICRO NETWORKS

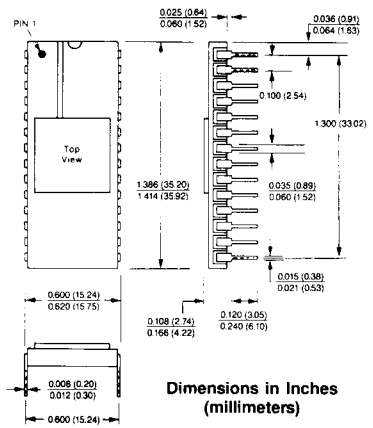
MN674A

μP-COMPATIBLE
15μsec, 12-Bit
A/D CONVERTER

FEATURES

- **Complete, 15μsec, 12-Bit A/D Converter with Internal:**
  - **Clock**
  - **Reference**
  - **Control Logic**
- **HI-674A and AD674A Pin and Function Compatible**
- **Full 8 or 16-Bit μP Interface:**
  - **Three-State Output Buffer**
  - **Chip Select, Address Decode**
  - **Read/Write Control**
- **±½LSB Linearity Guaranteed −55°C to +125°C (U Model)**
- **No Missing Codes Guaranteed Over Temperature**
- **Operation with ±12V or ±15V Supplies**
- **28-Pin DIP, 450mW Max Power**
- **Full Mil Operation −55°C to +125°C**

28-PIN CERAMIC DIP



Dimensions in Inches (millimeters)

DESCRIPTION

MN674A is a faster version (15μsec max conversion time) of the industry-standard MN574A microprocessor-interfaced, 12-bit A/D converter. It is a complete, successive-approximation A/D with internal buried-zener reference (+10V), clock, and control logic. MN674A is packaged in a 28-pin DIP and contains all the interface logic necessary to directly mate to most popular 8 and 16-bit microprocessors. The 3-state output buffer connects directly to the μP's data bus and can be read either as one 12-bit word or as two 8-bit bytes. Chip select, chip enable, address decode (short cycle), and read/write (read/convert) control inputs enable MN674A to connect directly to system address bus and control lines and operate totally under processor control.

MN674A's combination of bipolar and CMOS technologies represents the latest advances in 574A/674A evolution, and all problems associated with previous models from other manufacturers have been solved. These devices are truly TTL compatible over all temperature ranges, and they are not prone to CMOS latch-up at power-on. Their internal clock has minimal drift, and conversion time is guaranteed over all temperature ranges. Bus access time is guaranteed not to exceed 150nsec, and the A_0 line may be toggled freely with no fear of output-data overlap thanks to break-before-make action on the output buffer. At 450mW max, power consumption is almost half that of competing devices.

MN674A is ideal for most military/aerospace and industrial, general-purpose, data-acquisition applications. The device is available in 5 different electrical grades fully specified for either 0°C to +70°C or −55°C to +125°C operation. Each device guarantees integral linearity and no missing codes as summarized below. Add "/B" to either the S or T grade units for environmental stress screening.

Model	Temperature Range	Linearity Error Max (T_{min} to T_{max})	No Missing Codes (T_{min} to T_{max})
MN674AJ	0°C to +70°C	±1LSB	11 Bits
MN674AK	0°C to +70°C	±½LSB	12 Bits
MN674AL	0°C to +70°C	±½LSB	12 Bits
MN674AS	−55°C to +125°C	±1LSB	11 Bits
MN674AS/B*	−55°C to +125°C	±1LSB	11 Bits
MN674AT	−55°C to +125°C	±1LSB	12 Bits
MN674AT/B*	−55°C to +125°C	±1LSB	12 Bits

*Includes environmental stress screening.

MN674A

MICRO NETWORKS
324 Clark St., Worcester, MA 01606 (508) 852-5400

MN674A μP-COMPATIBLE 15μsec 12-Bit A/D CONVERTERS

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	−55°C to +125°C
Specified Temperature Range:	
MN674AJ, K, L	0°C to +70°C
MN674AS, S/B, T, T/B	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Positive Supply (+Vcc, Pin 7)	0 to +16.5 Volts
Negative Supply (−Vcc, Pin 11)	0 to −16.5 Volts
Logic Supply (+Vdd, Pin 1)	0 to +7 Volts
Digital Inputs (Pins 2-6)	−0.5 to (+Vdd + 0.5) Volts
Analog Inputs: Pins 10, 12 and 13	±16.5 Volts
Pin 14	±24 Volts
Analog Ground (Pin 9) to Digital Ground (Pin 15)	±1 Volt
Ref. Out (Pin 8) Short Circuit Duration	Continuous to Ground Momentary to ±Vcc

ORDERING INFORMATION

PART NUMBER — **MN674AX/B**

Select suffix J, K, L, S or T for desired performance and specified temperature range.

Add "/B" suffix to S or T models for environmental stress screening.

DESIGN SPECIFICATIONS ALL UNITS (T_A = +25°C, ±Vcc = ±12V or ±15V, +Vdd = +5V unless otherwise indicated) (Note 1)

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage Ranges: Unipolar		0 to +10, 0 to +20		Volts
Bipolar		±5, ±10		Volts
Input Impedance: 0 to +10V, ±5V	4.7	5	5.3	kΩ
0 to +20V, ±10V	9.4	10	10.6	kΩ
DIGITAL INPUTS CE, CS, R/C, A_0, 12/8 (Note 2)				
Logic Levels: Logic "1"	+2.0		+5.5	Volts
Logic "0"	−0.5		+0.8	Volts
Loading: Logic Currents	−5	±0.1	+5	μA
Input Capacitance		5		pF
DIGITAL OUTPUTS DB0-DB11, STS (Note 2)				
Output Coding (Note 3): Unipolar Ranges		Straight Binary		
Bipolar Ranges		Offset Binary		
Logic Levels: Logic "1" ($I_{source} \leq 500\mu A$)	+2.4			Volts
Logic "0" ($I_{sink} \leq 1.6mA$)			+0.4	Volts
Leakage (DB0-DB11) in High-Z State	−5	±0.1	+5	μA
Output Capacitance		5		pF
INTERNAL REFERENCE				
Reference Output (Pin 8): Voltage	+9.9	+10.0	+10.1	Volts
Drift		±10		ppm/°C
Output Source Current (Note 4)	2.0			mA
POWER SUPPLY REQUIREMENTS				
Power Supply Range: ±Vcc	±11.4		±16.5	Volts
+Vdd	+4.5	+5	+5.5	Volts
Power Supply Rejection (See Performance Specifications)				
Current Drains: +Vcc Supply		+3.5	+5	mA
−Vcc Supply		−15	−20	mA
+Vdd Supply		+9	+15	mA
Power Consumption (±Vcc = ±15V)		325	450	mW
DYNAMIC CHARACTERISTICS				
Conversion Time (Notes 1, 2, 5): 8-Bit Cycle	6	8	10	μsec
12-Bit Cycle	9	12	15	μsec

SPECIFICATION NOTES:

1. Detailed timing specifications appear in the Timing sections of this data sheet.
2. Listed specifications guaranteed over each device's full operating temperature range as determined by part number suffix.
3. See table of transition voltages in section labeled Output Coding.
4. The internal reference can be used to drive an external load, and it is capable of supplying up to 2mA over and above the requirements of the reference-in and bipolar-offset resistors. The external load should not vary during a conversion. The reference output does not require a buffer when operating with ±12V supplies.
5. If a conversion is started with A_0 (pin 4) low, a full 12-bit conversion cycle is initiated. If A_0 is high, a shorter 8-bit conversion is initiated. Conversion time is defined as the width of the Status Output pulse. See the Timing sections for more details.
6. MN674AJ, AK, AL are fully specified for 0°C to +70°C operation. MN674AS, AT are fully specified for −55°C to +125°C operation.
7. Adjustable to zero with external potentiometer.
8. Unipolar offset error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 0000 0000 0000 to 0000 0000 0001 when operating the MN674A on a unipolar range. The ideal value at which this transition should occur is +½LSB. See Digital Output Coding.
9. Listed maximum change specifications (temperature coefficients) for unipolar offset, bipolar offset and full scale calibration error correspond to the maximum change from the initial value (+25°C) to the value at T_{min} or T_{max}.
10. Bipolar offset error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 0111 1111 1111 to 1000 0000 0000 when operating the MN674A on a bipolar range. The ideal value at which this transition should occur is −½LSB. See Digital Output Coding.
11. Listed specs assume a fixed 50Ω resistor between Ref Out (pin 8) and Ref In (pin 10). Full scale calibration error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 1111 1111 1110 to 1111 1111 1111. Ideally, this digital output transition should occur at an analog voltage 1½LSB's below the nominal full scale voltage. See Digital Output Coding.
12. Listed spec is the max change in full scale calibration accuracy as supplies are varied over the range indicated.

Specifications subject to change without notice as Micro Networks reserves the right to make improvements and changes in its products.

PERFORMANCE SPECIFICATIONS (Typical at T_A = +25°C, ±Vcc = ±12V or ±15V, +Vdd = +5V unless otherwise indicated)

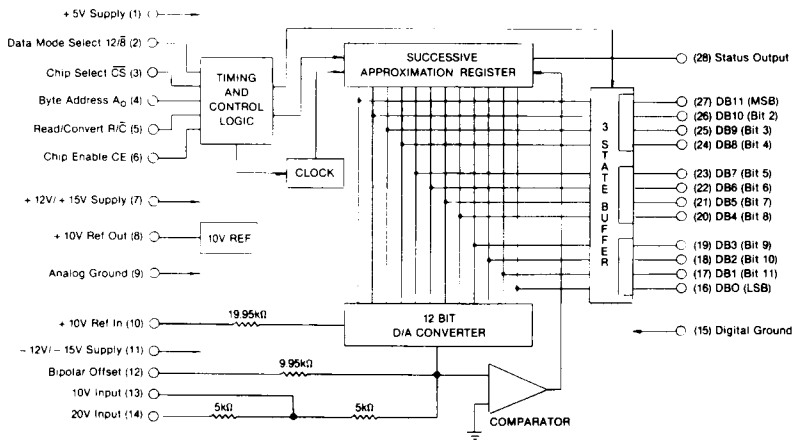
MODEL	674AJ	674AK	674AL	674AS	674AT	UNITS
Integral Linearity Error: Initial (+25°C) (Max)	±1	±½	±½	±1	±½	LSB
T_{min} to T_{max} (Max, Note 6)	±1	±½	±½	±1	±1	LSB
Resolution for Which No Missing Codes is Guaranteed: Initial (+25°C)	11	12	12	11	12	Bits
T_{min} to T_{max} (Note 6)	11	12	12	11	12	Bits
Unipolar Offset Error (Notes 7, 8):						
Initial (+25°C) (Max)	±2	±2	±2	±2	±2	LSB
Drift (Max)	±10	±5	±5	±5	±2.5	ppm of FSR/°C
Max Change to T_{min} or T_{max} (Note 9)	±2	±1	±1	±2	±1	LSB
Bipolar Offset Error (Notes 7, 10):						
Initial (+25°C) (Max)	±10	±4	±4	±10	±4	LSB
Drift (Max)	±10	±5	±5	±10	±5	ppm of FSR/°C
Max Change to T_{min} or T_{max} (Note 9)	±2	±1	±1	±4	±2	LSB
Full Scale Calibration Error (Notes 7, 11):						
Initial (+25°C) (Max)	±0.25	±0.25	±0.25	±0.25	±0.25	%FSR
T_{min} to T_{max} Without Initial Adjustment	±0.47	±0.37	±0.3	±0.75	±0.5	%FSR
T_{min} to T_{max} With Initial Adjustment	±0.22	±0.12	±0.05	±0.5	±0.25	%FSR
Drift (Max)	±50	±27	±10	±50	±25	ppm of FSR/°C
Max Change to T_{min} or T_{max} (Note 9)	±9	±5	±2	±20	±10	LSB
Power Supply Rejection (Note 12)						
+13.5V ≤ +Vcc ≤ +16.5V or +11.4V ≤ +Vcc ≤ +12.6V	±2	±1	±1	±2	±1	LSB
−16.5V ≤ −Vcc ≤ −13.5V or −12.6V ≤ −Vcc ≤ −11.4V	±2	±1	±1	±2	±1	LSB
+4.5V ≤ +Vdd ≤ +5.5V	±½	±½	±½	±½	±½	LSB

ORDERING INFORMATION

Part Number	Specified Temperature Range	Integral Linearity (1) +25°C	Integral Linearity (1) Temp.	No Missing Codes Over Temp.	Max. Offset Drift (2)	Max. Full Scale Drift (2)	Max. Power (mW)
MN674AJ	0°C to +70°C	±1	±1	11 Bits	±10	±50	450
MN674AK	0°C to +70°C	±½	±½	12 Bits	±5	±27	450
MN674AL	0°C to +70°C	±½	±½	12 Bits	±5	±10	450
MN674AS	−55°C to +125°C	±1	±1	11 Bits	±5	±50	450
MN674AS/B (3)	−55°C to +125°C	±1	±1	11 Bits	±5	±50	450
MN674AT	−55°C to +125°C	±½	±1	12 Bits	±2.5	±25	450
MN674AT/B (3)	−55°C to +125°C	±½	±1	12 Bits	±2.5	±25	450

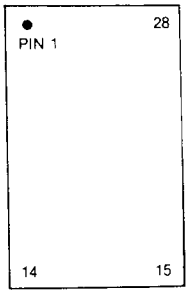
1. Maximum error expressed in LSB's for 12 bits.
2. Expressed in ppm of FSR/°C.
3. Includes environmental stress screening.

BLOCK DIAGRAM



CAUTION: These devices are sensitive to electronic discharge. Proper I.C. handling procedures should be followed.

PIN DESIGNATIONS



(1) +5V Supply (+ V_{dd})
(2) Data Mode Select 12/$\overline{8}$
(3) Chip Select $\overline{CS}$
(4) Byte Address A_0
(5) Read/Convert R/$\overline{C}$
(6) Chip Enable CE
(7) + 12V/+ 15V Supply (+ V_{cc})
(8) + 10V Ref Out
(9) Analog Ground
(10) + 10V Ref In
(11) – 12V/– 15V Supply (– V_{cc})
(12) Bipolar Offset
(13) 10V Input
(14) 20V Input
(28) Status Output
(27) DB11 (MSB)
(26) DB10 (Bit 2)
(25) DB9 (Bit 3)
(24) DB8 (Bit 4)
(23) DB7 (Bit 5)
(22) DB6 (Bit 6)
(21) DB5 (Bit 7)
(20) DB4 (Bit 8)
(19) DB3 (Bit 9)
(18) DB2 (Bit 10)
(17) DB1 (Bit 11)
(16) DB0 (LSB)
(15) Digital Ground

DESCRIPTION OF OPERATION

The MN674A is a complete 12-bit A/D converter. It utilizes the successive approximation conversion technique and contains all required function blocks — successive approximation register (SAR), D/A converter, comparator, clock and reference — internal to its package. The MN674A mates directly to most popular 8, 16 and 32-bit microprocessors and contains all the necessary address decoding logic, control logic and 3-state output buffering to operate completely under processor control. In most applications, the MN674A will require only power supplies, bypass capacitors, and two fixed resistors to provide the complete A/D conversion function. The completeness of this device makes it most convenient to think of the MN674A as a function block with specific input/output and transfer characteristics, and it is quite unnecessary to concern oneself with its inner workings.

Operating the MN674A under microprocessor control (it also functions as a stand-alone A/D) consists, in most applications, of a series of read and write instructions. Initiating a conversion requires sending a command from the processor to the A/D and involves a write operation. Retrieving digital output data is accomplished with read operations. Once the proper signals have been received and a conversion has begun, it cannot be stopped or restarted, and digital output data is not available until the conversion has been completed. Immediately following the initiation of a conversion cycle, the MN674A's Status Output (also called Busy Line or End of Conversion (E.O.C.) Line) rises to a logic "1" indicating that a conversion is in progress. At the end of a conversion, the internal control logic will drop the Status Output to a "0" and enable internal circuitry to permit output data to be read by external command. By sensing the state of the Status Output or by waiting an appropriate amount of time, the microprocessor will know when the conversion is complete and that output data is valid and can be read.

If the MN674A is operated with 12-bit or wider microprocessors, all 12 output bits can be 3-state enabled simultaneously, permitting data collection with a single read operation. If the MN674A is operated with an 8-bit μP, output data can be formatted to be read in two 8-bit bytes. The first will contain the 8 most significant bits (MSB's). The second will contain the remaining 4 least significant bits (LSB's), in a left justified format, with 4 trailing "0's".

APPLICATIONS INFORMATION

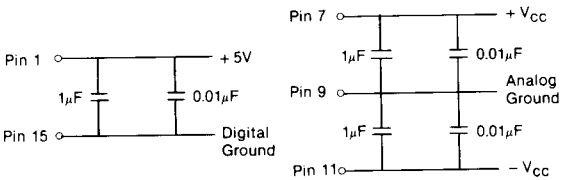
LAYOUT CONSIDERATIONS AND GROUNDING — Proper attention to layout and decoupling is necessary to obtain specified accuracy from the MN674A. It is critically important that the MN674A's power supplies be filtered, well regulated, and free from high-frequency noise. Use of noisy supplies may cause unstable output codes to be generated. Switching power supplies are not recommended for circuits attempting to achieve 12-bit accuracy unless great care is used in filtering any switching spikes present in the output.

Decoupling capacitors should be used on all power supply pins; the +5V supply decoupling capacitors should be connected directly from pin 1 to pin 15 (Digital Ground), and the +V_{CC} and –V_{CC} supplies should be decoupled directly to pin 9 (Analog Ground). A suitable decoupling capacitor pair is usually a relatively large tantalum (1 – 10μF) in parallel with a smaller (0.01 – 1.0μF) ceramic disc.

Coupling between analog inputs and digital signals should be minimized to avoid noise pickup. Pins 10 (Reference In), 12 (Bipolar Offset), and 13 and 14 (Analog Inputs) are particularly noise susceptible. Circuit layout should attempt to locate the MN674A and associated analog input circuitry as far as possible from high-speed digital circuitry. The use of wire-wrap circuit construction is not recommended. Careful printed-circuit construction is preferred. If external offset and gain adjust potentiometers are used, the pots and associated series resistors should be located as close to the MN674A as possible. If no trim adjusting is required and fixed resistors are used, they likewise should be as close as possible.

Analog (pin 9) and Digital (pin 15) Ground pins are not connected to each other internal to the MN674A. They must be tied together as close to the unit as possible and both connected to system analog ground, preferably through a large analog ground plane beneath the package. If these commons must be run separately, a non-polarized 0.01μF ceramic bypass capacitor should be connected between pins 9 and 15 as close to the unit as possible and wide conductor runs employed. Pin 9 (Analog Ground) is the ground reference point for the MN674A's internal reference. It should be connected as close as possible to the analog input signal reference point.

POWER SUPPLY DECOUPLING



CONTROL FUNCTIONS — Operating the MN674A under microprocessor control is most easily understood by examining the assorted control-line functions in a truth table. Table 1 below is a summary of MN674A control-line functions. Table 2 is the MN674A Truth Table.

Unless Chip Enable (CE, pin 6, logic "1" = active) and Chip Select ($\overline{CS}$, pin 3, logic "0" = active) are both asserted, various combinations of logic signals applied to other control lines (R/$\overline{C}$, 12/$\overline{8}$ and A_0) will have no effect on MN674[illegible] operation. When CE and $\overline{CS}$ are

Table 1: MN674A Control Line Functions

Pin Designation	Definition	Function
CE (Pin 6)	Chip Enable (active high)	Must be high ("1") to either initiate a conversion or read output data. 0→1 edge may be used to initiate a conversion.
$\overline{CS}$ (Pin 3)	Chip Select (active low)	Must be low ("0") to either initiate a conversion or read output data. 1→0 edge may be used to initiate a conversion
R/$\overline{C}$ (Pin 5)	Read/Convert ("1" = read) ("0" = convert)	Must be low ("0") to initiate either 8 or 12-bit conversions. 1→0 edge may be used to initiate a conversion. Must be high ("1") to read output data. 0→1 edge may be used to initiate a read operation
A_0 (Pin 4)	Byte Address Short Cycle	In the start-convert mode, A_0 selects 8-bit (A_0 = "1") or 12-bit (A_0 = "0") conversion mode. When reading output data in 2 8-bit bytes, A_0 = "0" accesses 8 MSB's (high byte) and A_0 = "1" accesses 4 LSB's and trailing "0's" (low byte).
12/$\overline{8}$ (Pin 2)	Data Mode Select ("1" = 12 bits) ("0" = 8 bits) (Note 5)	When reading output data, 12/$\overline{8}$ = "1" enables all 12 output bits simultaneously. 12/$\overline{8}$ = "0" will enable the MSB's or LSB's as determined by the A_0 line.

both asserted, the signal applied to R/$\overline{C}$ (Read/Convert, pin 5) determines whether a data read (R/$\overline{C}$="1") or a convert operation (R/$\overline{C}$="0") is initiated.

When initiating a conversion, the signal applied to A_0 (Byte Address/Short Cycle, pin 4) determines whether a 12-bit conversion is initiated (A_0="0") or an 8-bit conversion is initiated (A_0="1"). It is the combination of CE="1", $\overline{CS}$="0", R/$\overline{C}$="0" and A_0="1" or "0" that initiates a convert operation. The actual conversion can be initiated by the rising edge of CE, the falling edge of $\overline{CS}$ or the falling edge of R/$\overline{C}$ as shown in the Truth Table and as described in the section labeled Timing — Initiating Conversions. When initiating conversions, the 12/$\overline{8}$ line is a "don't care".

When reading digital output data from the MN674A, CE and $\overline{CS}$ must be asserted, and the signals applied to 12/$\overline{8}$ and A_0 will determine the format of output data. Logic "1" applied to the R/$\overline{C}$ line will initiate actual output data access. If the 12/$\overline{8}$ line is a "1", all 12 output data bits will be accessed simultaneously when the R/$\overline{C}$ line goes from a "0" to a "1".

If the 12/$\overline{8}$ line is a "0", output data will be accessible as two 8-bit bytes as detailed in the section labeled Timing — Reading Output Data. In this situation, A_0="0" will result in the 8 MSB's being accessed, and A_0="1" will result in the 4 LSB's and 4 trailing zeros being accessed. In this mode, only the 8 upper bits or the 4 lower bits can be enabled at one time, as addressed by A_0. For these applications, the 4 LSB's (pins 16-19) should be hardwired to the 4 MSB's (pins 24-27). Thus, during a read, when A_0 is low, the upper 8 bits are enabled and present data on pins 20 through 27. When A_0 goes high, the upper 8 data bits are disabled. The 4 LSB's then effectively present data to pins 24 to 27, and the 4 middle bits are overridden so that zeros are presented to pins 20 through 23. See the section labeled Hardwiring to 8-Bit Data Buses.

Table 2: MN674A Truth Table

CONTROL INPUTS					MN674A OPERATION
CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A_0	
0	X	X	X	X	No Operation
X	1	X	X	X	No Operation
1	0	1→0	X	0	Initiates 12-Bit Conversion
1	0	1→0	X	1	Initiates 8-Bit Conversion
0→1	0	0	X	0	Initiates 12-Bit Conversion
0→1	0	0	X	1	Initiates 8-Bit Conversion
1	1→0	0	X	0	Initiates 12-Bit Conversion
1	1→0	0	X	1	Initiates 8-Bit Conversion
1	0	1	1	X	Enables 12-Bit Parallel Output
1	0	1	0	0	Enables 8 MSB's
1	0	1	0	1	Enables 4 LSB's and 4 Trailing Zeros

TABLE 1, TABLE 2 NOTES:

1. "1" indicates TTL logic high (+2.0V minimum).
2. "0" indicates TTL logic zero (+0.8V maximum).
3. X indicates "don't care".
4. 0→1, 1→0 indicate logic transitions (edges).
5. Some vendors 674's required the 12/$\overline{8}$ line to be hard wired to either +5V (pin 1) or 0V (pin 15). The MN674A may be hard wired as such or driven with normal TTL signals.
6. Output data format is as follows:

MSB	XXXX	XXXX	XXXX	LSB
	High Bits	Middle Bits	Low Bits	
	8 MSB's		4 LSB's	

TIMING — INITIATING CONVERSIONS — It is the combination of CE="1", $\overline{CS}$="0", R/$\overline{C}$="0" and A_0="1" (initiate 8-bit conversion) or A_0="0" (initiate 12-bit conversion) that initiates a convert operation. As stated earlier, the actual conversion can be initiated by the rising edge of CE, the falling edge of $\overline{CS}$ or the falling edge of R/$\overline{C}$. Whichever occurs last will control the conversion; however, all three may change simultaneously. The nominal delay time from either input transition to the beginning of the conversion (rising edge of Status) is the same for all three inputs (60nsec). If it is desired that a particular one of these three inputs be responsible for starting the conversion, the other two should be stable a minimum of 50nsec prior to the transition of that input.

Because the MN674A's control logic latches the A_0 signal upon conversion initiation, the A_0 line should be stable immediately prior to whichever of the above transitions is used to initiate the conversion. The R/$\overline{C}$ transition is normally used to initiate conversions in stand-alone operation; however, it is not recommended to use this line to initiate conversions in μP applications. If R/$\overline{C}$ is high just prior to a conversion, there will be a momentary enabling of output data as if a read operation were occurring, and the result could be system

bus contention. In most applications, A_0 should be stable and R/$\overline{C}$ low before either CE or $\overline{CS}$ is used to initiate a conversion.

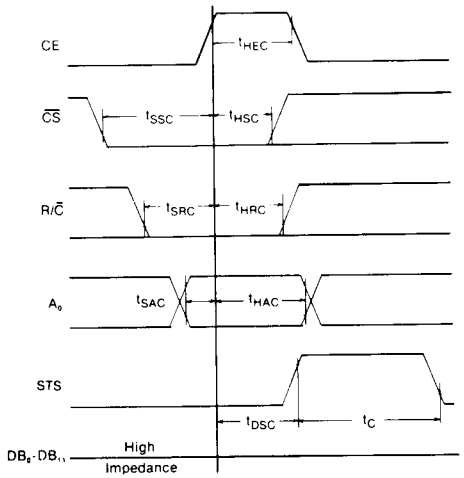
Timing for a typical application is shown below. In this application, $\overline{CS}$ is brought low, R/$\overline{C}$ is brought low, and A_0 is set to its chosen value prior to CE becoming a "1". This sequence can be accomplished in a number of ways including connecting $\overline{CS}$ and A_0 to address bus lines, connecting R/$\overline{C}$ to a read/write line (or its equivalent) and generating a CE 0→1 transition using the system clock. In this example, $\overline{CS}$ should be a "0" 50nsec prior to the CE transition (t_{SSC} =50nsec min), R/$\overline{C}$ should be a "0" 50nsec prior to the CE transition (t_{SRC} =50nsec min), and A_0 should be stable 0nsec prior to the CE transition (t_{SAC} =0nsec min). The minimum pulse width for CE="1" is 50nsec (t_{HEC} =50nsec min) and both $\overline{CS}$ and R/$\overline{C}$ must be valid for at least 50nsec while CE="1" (t_{HSC} and t_{HRC} =50nsec min) to effectively initiate the conversion. Similarly, A_0 must be valid for at least 50nsec (t_{HAC} =50nsec min) while CE is high to effectively initiate the conversion. The Status Line rises to a "1" no later than 200nsec after the rising edge of CE (t_{DSC} =200nsec max). Once Status="1", additional convert commands will be ignored until ongoing conversion is complete.

TIMING — RETRIEVING DATA — When a conversion is in progress (Status Output="1"), the MN674A's 3-state output buffer is in its high-impedance state. After the falling edge of Status indicates that the conversion is done, the combination of CE="1", $\overline{CS}$="0", and R/$\overline{C}$="1" is used to activate the buffer and read the digital output data. If the above combination of control signals is met and the 12/$\overline{8}$ line has a "1" applied, all twelve output bits will become valid simultaneously. If the 12/$\overline{8}$ line has a "0" applied, output data will be formatted for an 8-bit data bus. The 8 MSB's will become valid when the above conditions are met with A_0="0"; while the 8 LSB's (4 data bits and 4 trailing "0's") will become valid whenever A_0="1". If 12/$\overline{8}$="1", A_0 is a "don't care". If an 8-bit conversion is performed and all 12 output data bits are read, bit 9 (DB3) will be a "1", and bits 10-12 (DB2-DB0) will be "0's". Data access can be initiated by either the rising edge of CE or the falling edge of $\overline{CS}$.

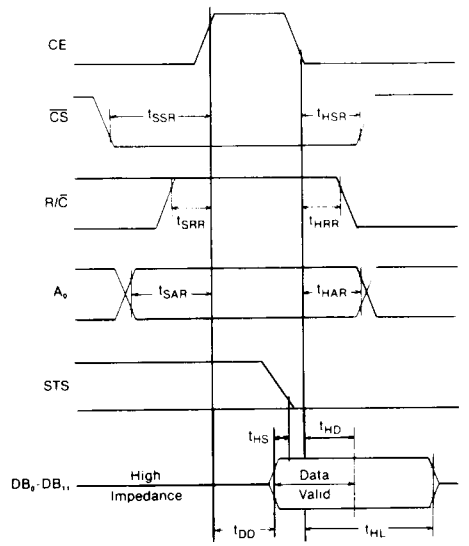
Timing for a typical application is shown below. In this application, $\overline{CS}$ is brought low, A_0 is set to its final state, and R/$\overline{C}$ is brought high all before the rising edge of CE. $\overline{CS}$ and A_0 should be valid 50nsec prior to CE (t_{SSR} =50nsec min, t_{SAR} =50nsec min). R/$\overline{C}$ can become valid the same time as CE (t_{SRR} =0nsec min).

A_0 may be toggled at any time without damage to the converter. Break-before-make action is guaranteed between the two data bytes, which assures that the outputs strapped together in 8-bit bus applications will never be enabled at the same time.

Access time is measured from the point at which CE and R/$\overline{C}$ are both high (assuming $\overline{CS}$ is already low). Data actually becomes valid typically 300nsec before the falling edge of Status as indicated by t_{HS}. In most applications, the 12/$\overline{8}$ input will be hard-wired high or low; although it is fully TLL/CMOS compatible and may be actively driven.



Convert Start Timing



Read Cycle Timing

MN674A TIMING SPECIFICATIONS:

CONVERT MODE

Symbol	Parameter	Min	Typ	Max	Units
t_{DSC}	STS Delay from CE		60	200	ns
t_{HEC}	CE Pulse Width	50	30		ns
t_{SSC}	$\overline{CS}$ to CE Setup	50	20		ns
t_{HSC}	$\overline{CS}$ Low During CE High	50	20		ns
t_{SRC}	R/$\overline{C}$ to CE Setup	50	0		ns
t_{HRC}	R/$\overline{C}$ Low During CE High	50	20		ns
t_{SAC}	A_0 to CE Setup	0			ns
t_{HAC}	A_0 Valid During CE High	50	20		ns
t_C	Conversion Time (Over Temp.)				
	8-Bit Cycle	6	8	10	μs
	12-Bit Cycle	9	12	15	μs

MN674A TIMING SPECIFICATIONS:

READ MODE

Symbol	Parameter	Min	Typ	Max	Units
t_{DD}	Access Time (from CE)		75	150	ns
t_{HD}	Data Valid after CE Low	25	35		ns
t_{HL}	Output Float Delay		100	150	ns
t_{SSR}	$\overline{CS}$ to CE Setup	50	0		ns
t_{SRR}	R/$\overline{C}$ to CE Setup	0			ns
t_{SAR}	A_0 to CE Setup	50	25		ns
t_{HSR}	$\overline{CS}$ Valid After CE Low	0			ns
t_{HRR}	R/$\overline{C}$ High After CE Low	0			ns
t_{HAR}	A_0 Valid After CE Low	50			ns
t_{HS}	STS Delay After Data Valid	100	300	600	ns

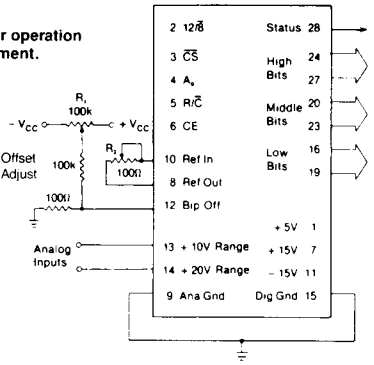
UNIPOLAR OPERATION AND CALIBRATION — Analog input connections and calibration circuits for the unipolar operating modes are shown below. If the 0 to +10V input range is to be used, apply the analog input to pin 13. If the 0 to +20V range is used, apply the analog input to pin 14. If gain adjustment is not used, replace trim pot R_2 with a fixed, 50Ω ± 1%, metal-film resistor to meet all published specifications. If unipolar offset adjustment is not used, connect pin 12 (Bipolar Offset) directly to pin 9 (Analog Ground).

Unipolar offset error refers to the accuracy of the 0000 0000 0000 to 0000 0000 0001 digital output transition (see Digital Output Coding). If offset adjustment is not used, the actual transition will occur within ±2 LSB's of its ideal value (+½ LSB). For the 10V range, 1 LSB=2.44mV. For the 20V range, 1 LSB=4.88mV. To offset adjust, apply an analog input equal to +½ LSB and, with the MN674A continuously converting, adjust the offset potentiometer "down" until the digital output is all "0's" and then adjust "up" until the LSB "flickers" between "0" and "1".

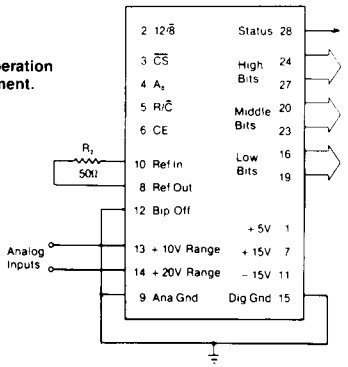
Unipolar gain error can be defined as the accuracy of the 1111 1111 1110 to 1111 1111 1111 digital output transition after unipolar offset adjustment has been accomplished. Ideally, this transition should occur 1½ LSB's below the nominal full scale of the selected input range. This corresponds to +9.9963V and +19.9927V respectively for the 10V and 20V unipolar input ranges. Gain trimming is accomplished by applying either of these voltages and adjusting the gain potentiometer "up" until the digital outputs are all "1's" and then adjusting down until the LSB "flickers" between "1" and "0".

If a 10.24V (1 LSB=2.5mV) or a 20.48V (1 LSB=5mV) input range is required, the gain trim pot (R_2) should be replaced with a fixed 50Ω resistor and a 200Ω trim pot (500Ω for 20.48V) inserted in series with the analog input to pin 13 (pin 14 for 20.48V). Offset trimming proceeds as described above. Gain trimming is now accomplished with the new pots. If one is not gain trimming and wishes to use fixed-value resistors, the values are 120Ω and 240Ω, respectively. MN674A's input impedance is laser trimmed to a typical accuracy of ±2%.

MN674A unipolar operation with trim adjustment.



MN674A unipolar operation without trim adjustment.

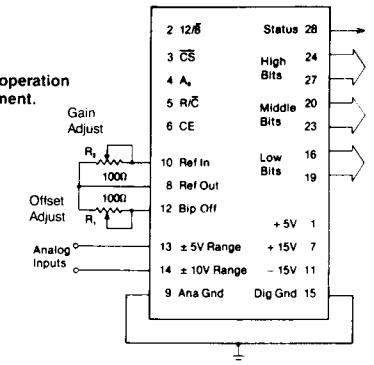


BIPOLAR OPERATION AND CALIBRATION — Analog input connections and calibration circuits for the bipolar operating modes are shown below. If the ±5V input range is to be used, apply the analog input to pin 13. If the ±10V range is used, apply the analog input to pin 14. If either bipolar offset or bipolar gain adjustments are not to be used, the trim pots R_1 and R_2 should be replaced with fixed, 50Ω ± 1%, metal-film resistors to meet all published specifications.

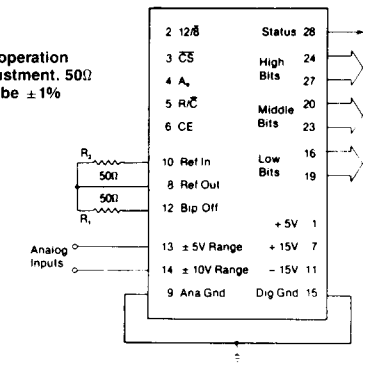
Bipolar offset error refers to the accuracy of the 0111 1111 1111 to 1000 0000 0000 digital output transition (see Digital Output Coding). Ideally, this transition should occur ½ LSB below zero volts, and if bipolar offset adjustment is not used, the actual transition will occur within the specified limit of its ideal value. Offset adjusting on the bipolar device is performed not at the zero crossing point but at the minus full scale point. The procedure is to apply an analog input equal to −FS+½ LSB (−4.9988V for the ±5V range, −9.9976V for the ±10V range) and adjust the bipolar offset trim pot "down" until the digital output is all "0's". Then adjust "up" until the LSB "flickers" between "0" and "1".

Bipolar gain error can be defined as the accuracy of the 1111 1111 1110 to 1111 1111 1111 digital output transition after bipolar offset adjustment has been accomplished. Ideally, this transition should occur 1½ LSB's below the nominal positive full scale value of the selected input range. This corresponds to +4.9963V and +9.9927V respectively for the ±5V and ±10V bipolar input ranges. Gain trimming is accomplished by applying either of these voltages and adjusting the gain trim pot "up" until the digital outputs are all "1's" and then adjusting "down" until the LSB "flickers" between "1" and "0".

MN674A bipolar operation with trim adjustment.

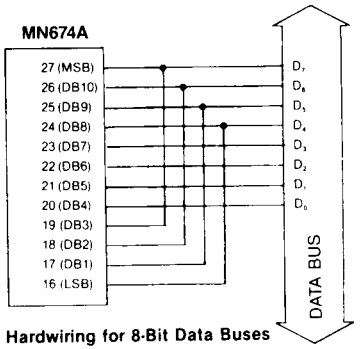


MN674A bipolar operation without trim adjustment. 50Ω resistors should be ±1% metal film.



HARDWIRING TO 8-BIT DATA BUSES — For applications with 8-bit data buses, output lines DB4-DB11 (pins 20-27) should be connected directly to data bus lines D_0-D_7. In addition, output lines DB0-DB3 (pins 16-19) should be connected to data bus lines D_4-D_7 or to MN674A output lines DB8-DB11. Thus, if A_0 is low during a read operation, the upper 8 bits are enabled and become valid on output pins 20-27. When A_0 is high during a read operation, the 4 LSB's are enabled on output pins 16-19 and the 4 middle bits (pins 20-23) are overridden with "0's".

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
High Byte ($A_0 = 0$)	MSB	DB10	DB9	DB8	DB7	DB6	DB5	DB4
Low Byte ($A_0 = 1$)	DB3	DB2	DB1	DB0	0	0	0	0

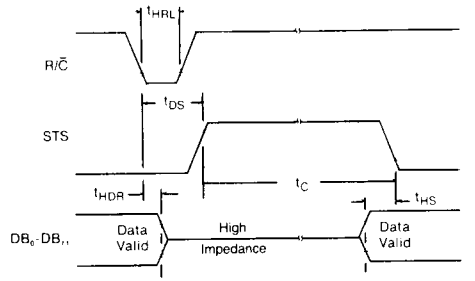


Hardwiring for 8-Bit Data Buses

STAND-ALONE OPERATION

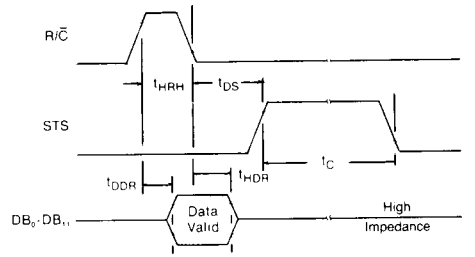
The MN674A can be used in a "stand-alone" mode in systems having dedicated input ports and not requiring full bus interface capability. In this mode, $\overline{CE}$ and 12/$\overline{8}$ are tied to logic "1" (they may be hard-wired to +5V), $\overline{CS}$ and A_0 are tied to logic "0" (they may be grounded), and the conversion is controlled by R/$\overline{C}$. A conversion is initiated whenever R/$\overline{C}$ is brought low (assuming a conversion is not already in progress), and all 12 bits of the three-state output buffers are enabled whenever R/$\overline{C}$ is brought high (assuming Status has already gone low indicating conversion complete).

This gives rise to two possible modes of operation; conversions can be initiated with either positive or negative R/$\overline{C}$ pulses. The timing diagram below details operation with a negative start pulse. In this case, the outputs are forced into the high-impedance state in response to the falling edge of R/$\overline{C}$ and return to valid logic levels after the conversion cycle is completed. The Status Output goes high 200ns after R/$\overline{C}$ goes low (t_{DS}) and returns low no longer than 1000nsec after data is valid (t_{HS}). In this mode, output data is available "most of the time" and becomes invalid only during a conversion.



Low Pulse for R/$\overline{C}$—Outputs Enabled After Conversion

The timing diagram below details operation with a positive start pulse. Output data lines are enabled during the time R/$\overline{C}$ is high. The falling edge of R/$\overline{C}$ starts the next conversion, and the data lines return to three-state (and remain three-state) until the next rising edge of R/$\overline{C}$. In this mode, output data is inaccessible "most of the time" and becomes valid only when R/$\overline{C}$ is brought high.



High Pulse for R/$\overline{C}$—Outputs Enabled While R/$\overline{C}$ High, Otherwise High-Z

STAND-ALONE MODE TIMING

Symbol	Parameter	Min	Typ	Max	Units
t_{HRL}	Low R/$\overline{C}$ Pulse Width	50			ns
t_{DS}	STS Delay from R/$\overline{C}$			200	ns
t_{HDR}	Data Valid After R/$\overline{C}$ Low	25			ns
t_{HS}	STS Delay After Data Valid	300	400	1000	ns
t_{HRH}	High R/$\overline{C}$ Pulse Width	150			ns
t_{DDR}	Data Access Time			150	ns

DIGITAL OUTPUT CODING

ANALOG INPUT VOLTAGE (Volts)				DIGITAL OUTPUT
0 to + 10V	0 to + 20V	± 5V	± 10V	MSB LSB
+ 10.0000	+ 20.0000	+ 5.0000	+ 10.0000	1111 1111 1111
+ 9.9963	+ 19.9927	+ 4.9963	+ 9.9927	1111 1111 111Ø*
+ 5.0012	+ 10.0024	+ 0.0012	+ 0.0024	1000 0000 000Ø*
+ 4.9988	+ 9.9976	− 0.0012	− 0.0024	ØØØØ ØØØØ ØØØØ*
+ 4.9963	+ 9.9927	− 0.0037	− 0.0073	0111 1111 111Ø*
+ 0.0012	+ 0.0024	− 4.9988	− 9.9976	0000 0000 000Ø*
0.0000	0.0000	− 5.0000	− 10.0000	0000 0000 0000

DIGITAL OUTPUT CODING NOTES:

1. For unipolar input ranges, output coding is straight binary.
2. For bipolar input ranges, output coding is offset binary.
3. For 0 to + 10V or ± 5V input ranges, 1LSB for 12 bits = 2.44mV. 1LSB for 11 bits = 4.88mV.
4. For 0 to + 20V or ± 10V input ranges, 1LSB for 12 bits = 4.88mV. 1LSB for 11 bits = 9.77mV.

*Voltages given are the theoretical values for the transitions indicated. Ideally, with the converter continuously converting, the output bits indicated as Ø will change from "1" to "0" or vice versa as the input voltage passes through the level indicated.

EXAMPLE: For an MN674A operating on its ± 10V input range, the transition from digital output 0000 0000 0000 to 0000 0000 0001 (or vice versa) will ideally occur at an input voltage of − 9.9976 volts. Subsequently, any input voltage more negative than − 9.9976 volts will give a digital output of all "0's". The transition from digital output 1000 0000 0000 to 0111 1111 1111 will ideally occur at an input of − 0.0024 volts, and the 1111 1111 1111 to 1111 1111 1110 transition should occur at + 9.9927 volts. An input more positive than + 9.9927 volts will give all "1's".