



# SPP9517

## P-Channel Enhancement Mode MOSFET

### DESCRIPTION

The SPP9517 is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application , notebook computer power management and other battery powered circuits where high-side switching .

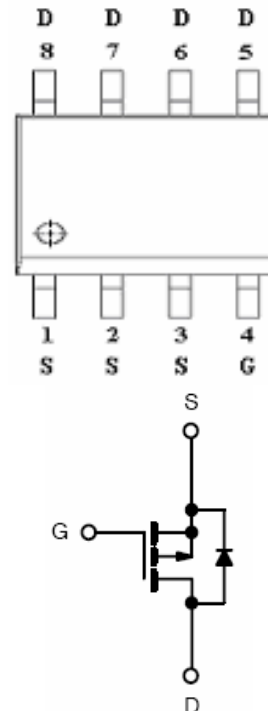
### FEATURES

- ◆ -40V/-10A,  $R_{DS(ON)} = 16m\Omega @ V_{GS} = -10V$
- ◆ -40V/- 8A,  $R_{DS(ON)} = 22m\Omega @ V_{GS} = -4.5V$
- ◆ Super high density cell design for extremely low  $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ SOP – 8P package design

### APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

### PIN CONFIGURATION(SOP – 8P)



### PART MARKING





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### PIN DESCRIPTION

Pin	Symbol	Description
1	S	Source
2	S	Source
3	S	Source
4	G	Gate
5	D	Drain
6	D	Drain
7	D	Drain
8	D	Drain

### ORDERING INFORMATION

Part Number	Package	Part Marking
SPP9517S8RGB	SOP- 8P	SPP9517

※ SPP9517S8RGB 13" Tape Reel ; Pb – Free ; Halogen – Free

### ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit	
Drain-Source Voltage	V <sub>DSS</sub>	-40	V	
Gate –Source Voltage	V <sub>GSS</sub>	±20	V	
Continuous Drain Current(T <sub>J</sub> =150°C)	I <sub>D</sub>	TA=25°C	-10	A
		TA=70°C	-8	
Pulsed Drain Current	I <sub>DM</sub>	-30	A	
Continuous Source Current(Diode Conduction)	I <sub>S</sub>	-2.3	A	
Power Dissipation	P <sub>D</sub>	TA=25°C	2.8	W
		TA=70°C	1.8	
Operating Junction Temperature	T <sub>J</sub>	-55/150	°C	
Storage Temperature Range	T <sub>STG</sub>	-55/150	°C	
Thermal Resistance-Junction to Ambient	R <sub>θJA</sub>	70	°C/W	



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### ELECTRICAL CHARACTERISTICS

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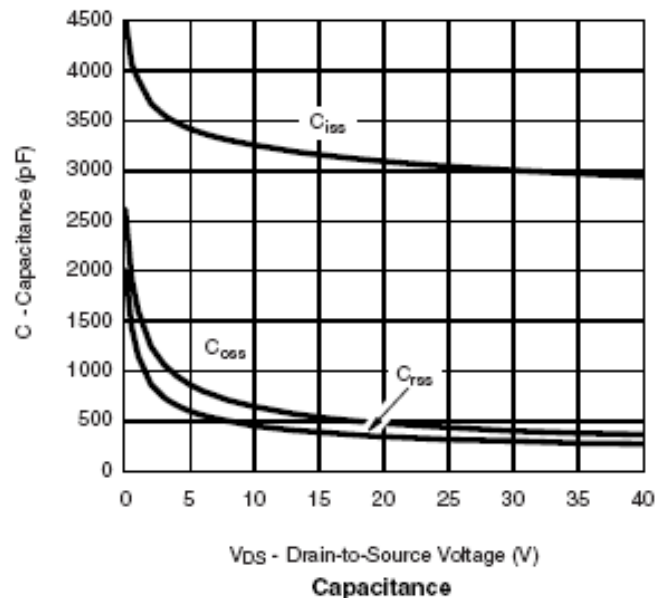
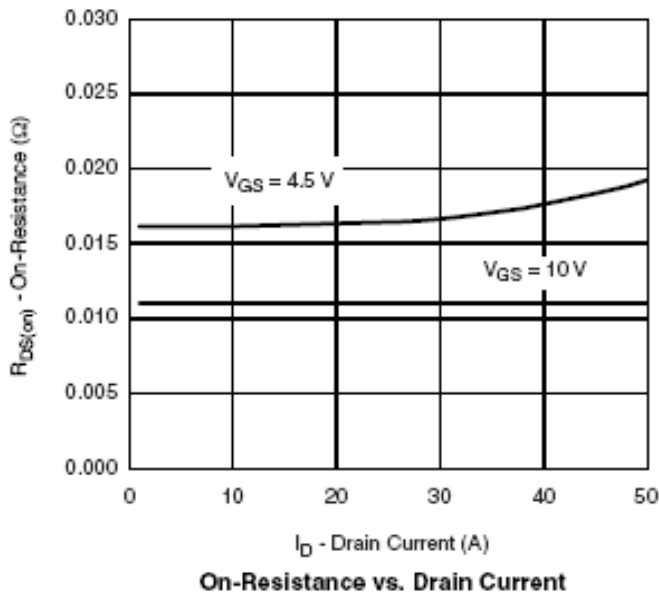
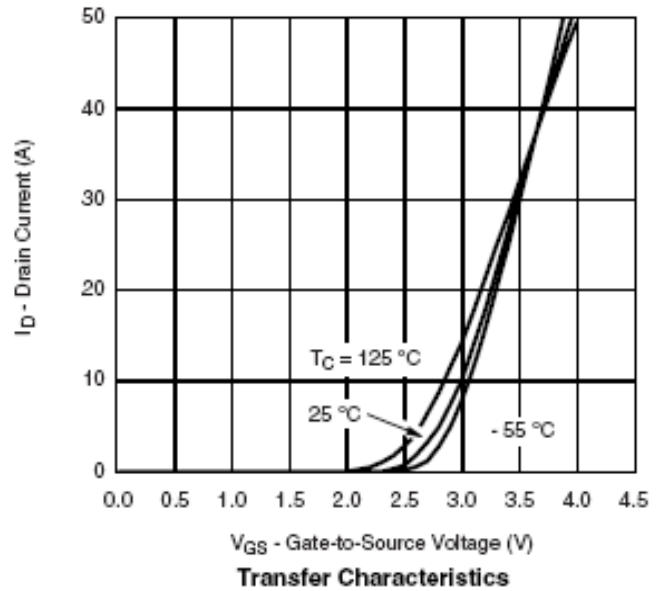
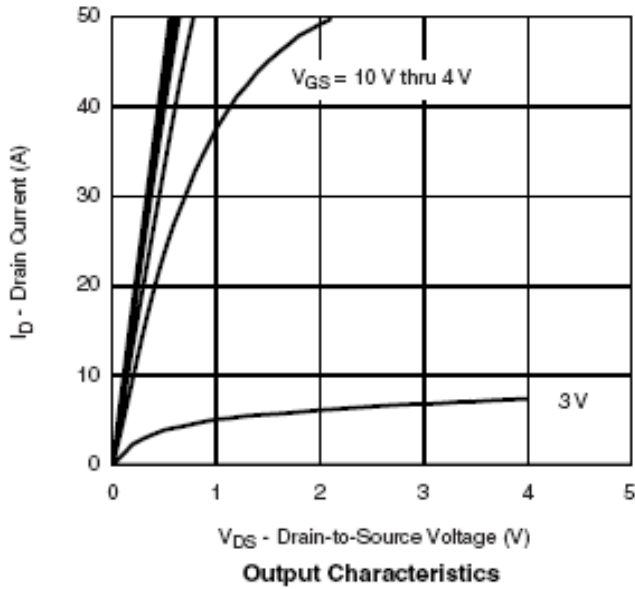
Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=-250\mu A$	-40			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-0.8		-2.5	
Gate Leakage Current	$I_{GSS}$	$V_{DS}=0V, V_{GS}=\pm 20V$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=-36V, V_{GS}=0V$			-1	uA
		$V_{DS}=-36V, V_{GS}=0V$ $T_J=85^\circ C$			-10	
On-State Drain Current	$I_{D(on)}$	$V_{DS}=-5V, V_{GS}=-4.5V$	-10			A
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=-10V, I_D=-10A$		0.012	0.016	$\Omega$
		$V_{GS}=-4.5V, I_D=-8A$		0.017	0.022	
Forward Transconductance	$g_{fs}$	$V_{DS}=-15V, I_D=-5.7A$		13		S
Diode Forward Voltage	$V_{SD}$	$I_S=-2.3A, V_{GS}=0V$		-0.8	-1.2	V
<b>Dynamic</b>						
Total Gate Charge	$Q_g$	$V_{DS}=-15V, V_{GS}=-5.0V$ $I_D=-10.0A$		40	55	nC
Gate-Source Charge	$Q_{gs}$			10		
Gate-Drain Charge	$Q_{gd}$			14		
Input Capacitance	$C_{iss}$	$V_{DS}=-20V, V_{GS}=0V$ $f=1MHz$		2300		pF
Output Capacitance	$C_{oss}$			280		
Reverse Transfer Capacitance	$C_{rss}$			240		
Turn-On Time	$t_{d(on)}$	$V_{DD}=-15V, R_L=15\Omega$ $I_D=-1.0A, V_{GEN}=-10.0V$ $R_G=6\Omega$		20	25	nS
	$t_r$			15	25	
Turn-Off Time	$t_{d(off)}$			60	90	
	$t_f$			40	60	



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### TYPICAL CHARACTERISTICS

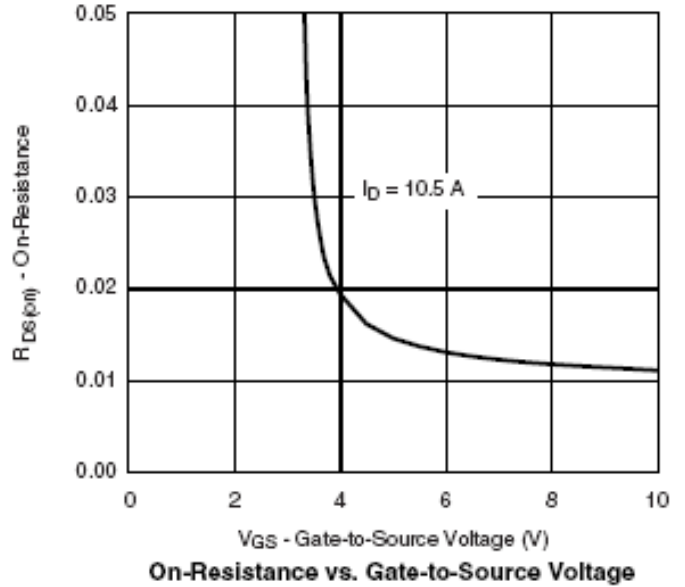
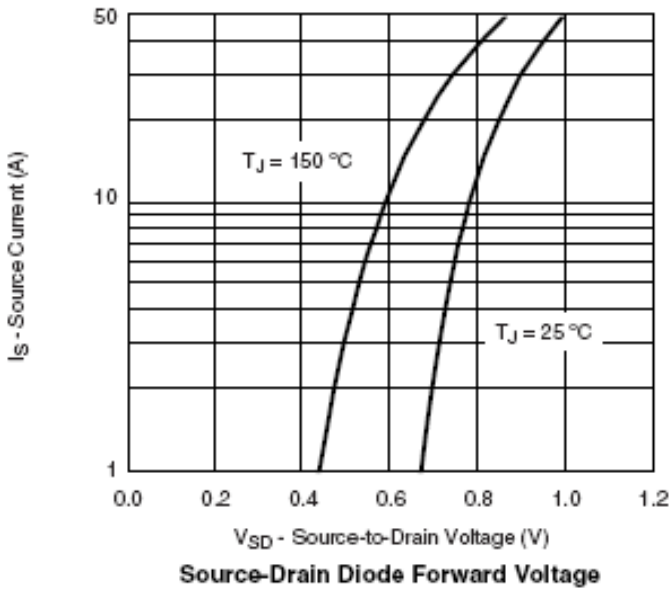
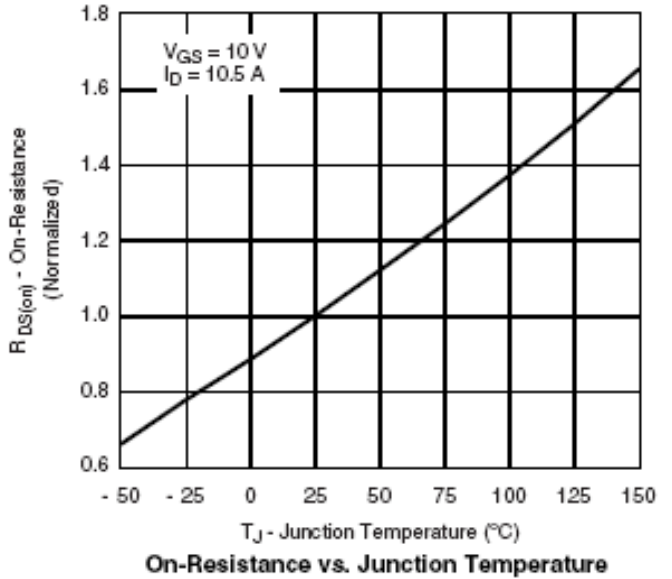
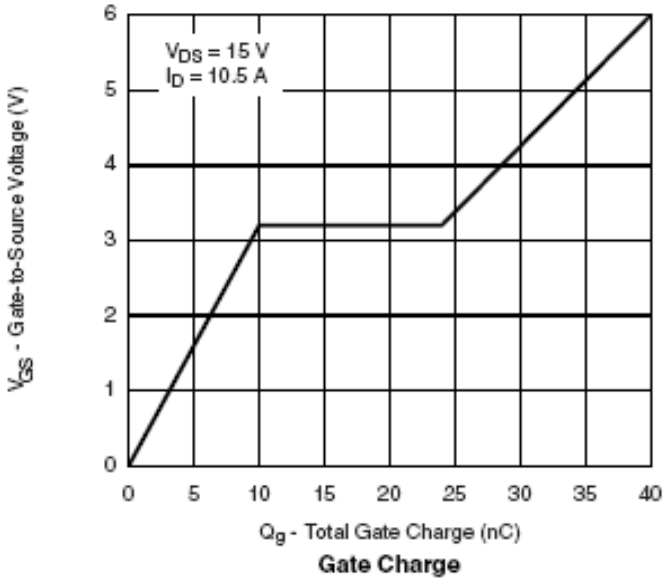




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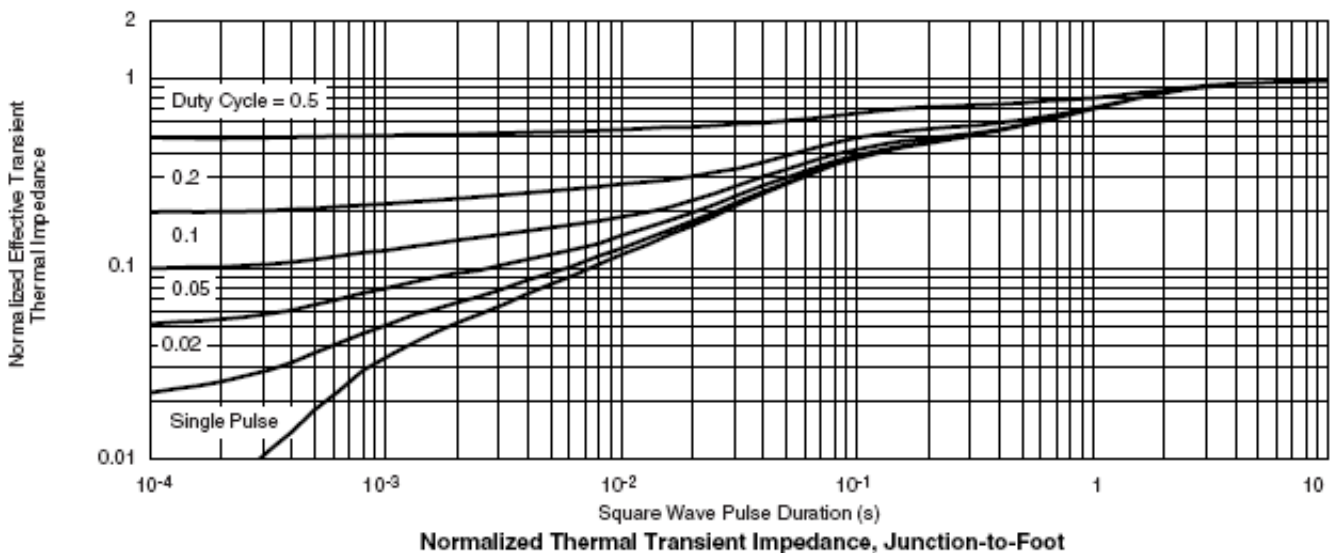
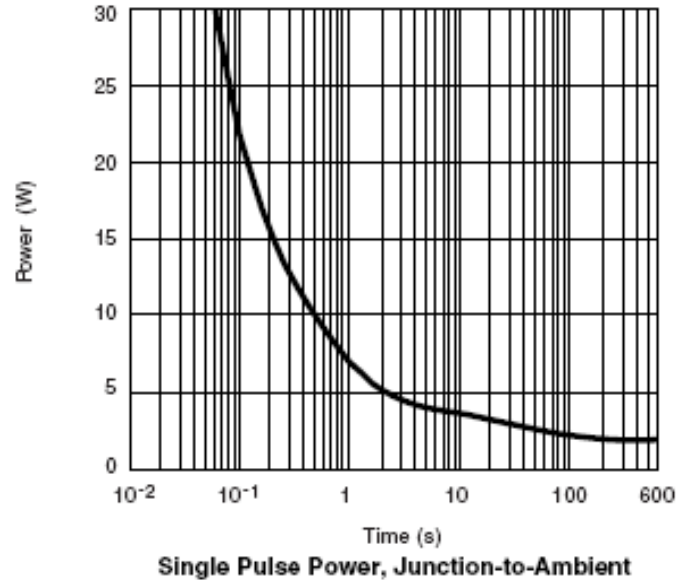
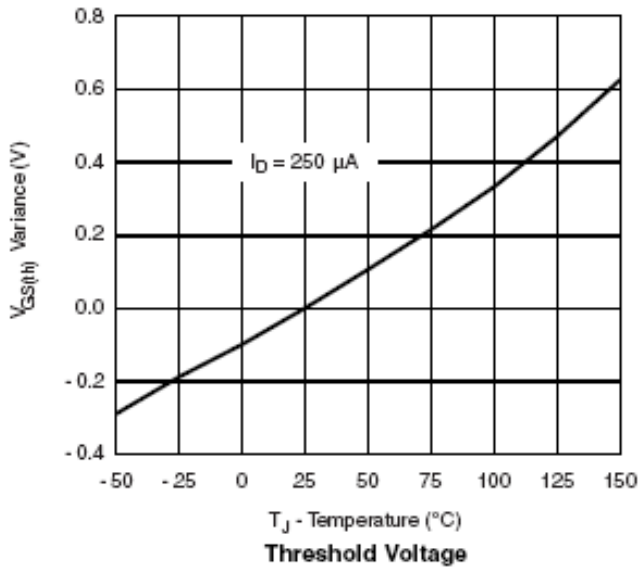




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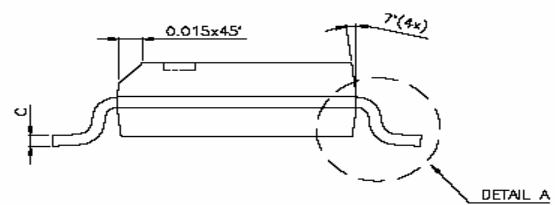
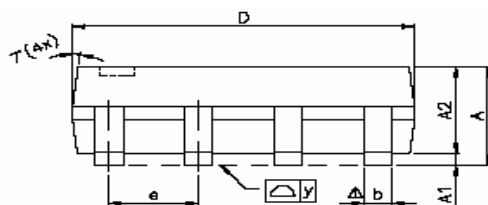
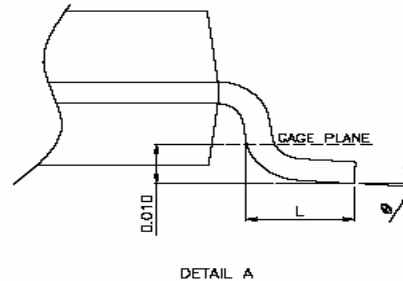
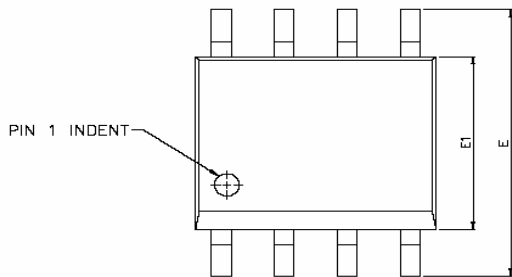




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### SOP- 8 PACKAGE OUTLINE



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.47	1.60	1.73	0.058	0.063	0.068
A1	0.10	—	0.25	0.004	—	0.010
A2	—	1.45	—	—	0.057	—
b	0.33	0.41	0.51	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.0098
D	4.80	4.85	4.95	0.189	0.191	0.195
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e	—	1.27	—	—	0.050	—
L	0.38	0.71	1.27	0.015	0.028	0.050
$\Delta y$	—	—	0.076	—	—	0.003
$\varnothing$	0°	—	8°	0°	—	8°



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