TDK SEMICONDUCTOR CORP.

AVPro® 5002B
Dual SCART A/V Switch

August 2000

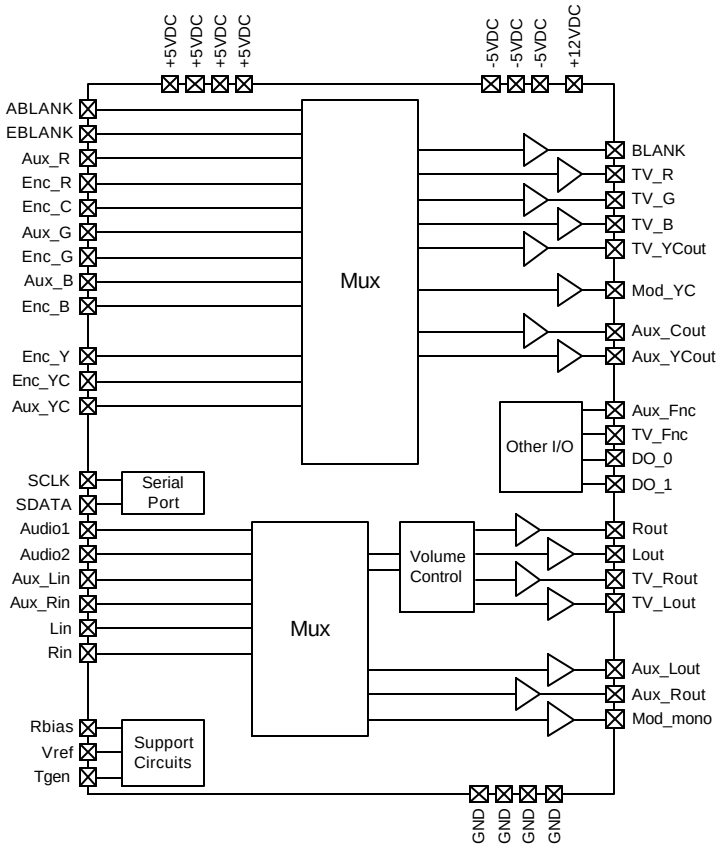
DESCRIPTION

The AVPro® 5002B device is an audio/video switching IC that supports an input/output port, an input only port, and an output only port. The device includes multiplexers that allow the inputs to be routed to the outputs in various configurations. Additional outputs are provided to drive an external RF modulator. The video outputs of the multiplexers are buffered to drive 137ohm loads. The audio outputs are buffered to provide 2 Vrms output into 600 ohms. The 5002B has features optimized for BSkyB satellite receiver applications, but it can also be used in other applications that require control of multiple audio and video sources.

FEATURES

- Two SCART connections (Auxiliary, TV)
- Video section
  - Integrated output drivers
  - RGB, SVHS, composite outputs
  - Programmable RGB gain
- Audio section
  - 5-bit audio attenuation, 0 to -31 dB
  - Auxiliary tone inputs to support BSkyB
  - Ground based outputs (no AC coupling caps)
- Serial port control of switching I^2C bus
- 64-lead LQFP package

BLOCK DIAGRAM



AVPro® 5002B
Dual SCART A/V Switch

FUNCTIONAL DESCRIPTION

The 5002B is an audio/video switching device. The device integrates both audio and video drivers so that it can directly drive the SCART interface. The use of a -5 volt supply eliminates the need for AC coupling capacitors on the audio outputs. All programmable functions of the device are controlled through a standard I^2C serial interface and a set of internal registers. This device will interface to an external video encoder that provides six video outputs. In addition, the 5002B includes two programmable digital outputs and inputs for the TV SCART audio /video.

SCART VIDEO SWITCHING

The device is designed to accept video signals from an auxiliary SCART connector, TV SCART connector, and an external video encoder/DAC device. The device includes a set of analog multiplexers that receive video signals from these sources and allows routing of the signals to the various video outputs. The video output drivers have a nominal gain of 1.83 V/V to allow for a series resistance of 62 ohms prior to the 75 ohm termination. A block diagram of the video switching function is provided in Figure 1. Details of the register settings are provided in the section titled “Serial Port Register Tables”.

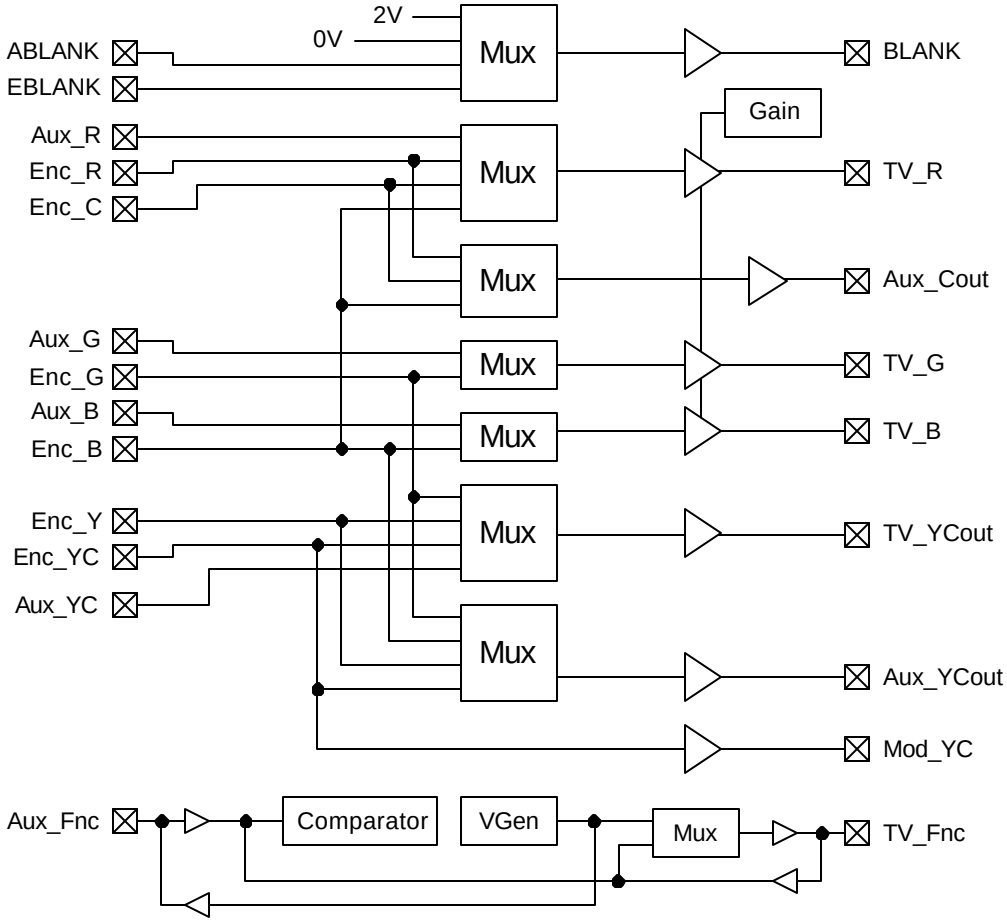


Figure 1: 5002B Video switching block diagram

TV RGB OUTPUTS

The device accepts RGB video signals from two sources. The *Aux_R*, *Aux_G*, *Aux_B* input pins are typically connected to the auxiliary SCART connector. The *Enc_R*, *Enc_G*, *Enc_B* input pins are connected to the RGB outputs of an external video encoder device. These outputs are used as a video source for the TV SCART pins *TV_R*, *TV_G*, and *TV_B*. The RGB video source is selected by setting the lower three (3) bits of serial port Register 1. When these bits are set to xxxxxx00, the RGB source will be the encoder. When these bits are set to xxxxxx01, the source will be the auxiliary port.

RGB Gain: The gain of the RGB outputs can be adjusted to one of four different levels. Bits 4 and 5 in Register 2 set the gain of the RGB output amplifiers according to the following table:

Bit 5	Bit 4	RGB Amplifier Gain
0	**0**	**Gain = 1.83V/V = A_0**
0	1	Gain = A_0 - 10%
1	0	Gain = A_0 - 20%
1	1	Gain = A_0 - 30%

DC Restore: The device will generate a DC restore level on each video output based on timing referenced to a horizontal sync pulse. When the sync pulse is detected, the DC restore circuit will act to position the blank level to 0.6 V at the respective video output load. The device can be programmed to look for the horizontal sync pulse on all of the RGB input pins or on the associated composite video input pin (*Aux_YC* for the auxiliary port or *Enc_YC* for the external encoder). Bit 7 of Register 1 determines the horizontal sync source. At power-up, this bit defaults to a low (0) state which programs the device to look for a sync detect on the RGB input signals. In this mode, the device can detect a horizontal sync on any of the three RGB input signals. When Bit 7 is set to a high (1) state, the device will look for a sync detect from the signal on either the *Aux_YC* or *Enc_YC* pin depending on which source is selected.

Blanking: The signal on the *Blank* output pin is determined by the state of two MSBs in Register 2 according to the following table:

Bit 7	Bit 6	*Blank* source
0	**0**	**BLANK = ABLANK**
0	1	BLANK = EBLANK
1	0	BLANK = 0V
1	1	BLANK = 4V @ IC output pin

The user must insure that the source of the *Blank* output is the same as the source for the RGB outputs, i.e.*ABLANK* is selected when the auxiliary RGB is active and *EBLANK* is selected when the encoder RGB is active.

TV COMPOSITE OUTPUT

The device provides inputs for two composite video sources that can be switched to the TV SCART composite video pin, *TV_YCout*. The *AUX_YC* input pin is typically connected to the “Video In” pin on the auxiliary SCART connector. The *Enc_YC* input pin is typically connected to the “YC” or “CVBS” output from the external video encoder device. Selection of the video source for the TV composite output is accomplished when the RGB video source is selected (see the register tables).

TV SVHS OUTPUT MODE

The device supports SVHS video format. The SVHS mode is selected for the TV SCART using the lower three (3) bits of Register 1. When the SVHS mode is selected, the *TV_YCout* pin will provide the luminance signal output from the selected source. The chroma output will be provided on the *TV_R* pin. The video source for SVHS mode can be either the auxiliary port or the encoder port. When the auxiliary port is selected as the video source, the video on *Aux_R* will be provided at the *TV_R* output pin and the *Aux_YC* video will be provided at the *TV_YCout* pin.

The device will support SVHS mode for three encoder interface formats. The first encoder interface format accepts chroma signals on the *Enc_C* pin and luma signals on the *Enc_Y* pin for the "SVHS, Enc 1" mode. The second format will receive chroma information on the *Enc_B* pin and luma information on *Enc_G*. This format is designated "SVHS, Enc 2". The third format will receive chroma information from the *Enc_R* pin and luma information from the *Enc_G* pin. This mode is designated “SVHS, Enc 3”.

When the SVHS mode is selected, the DC restore on the *TV_R* pin will average to approximately 1.68 VDC at the output pin. The DC restore circuit will act to position the blank level to 0.6 V at the *TV_YCout* video output load. The *TV_G* and *TV_B* outputs will be set to 0 VDC when the SVHS mode is active.

RF MODULATOR OUTPUT

The device provides an output, *Mod_YC*, to drive an external RF modulator. This output is driven by the *Enc_YC* input at all times.

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TV VIDEO MUTE

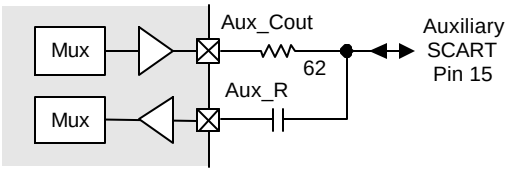
All TV video outputs can be simultaneously disabled by programming the lower three (3) bits in Register 1. The power-up default condition is xxxxx111, which sets all TV video outputs to 0 VDC and switches the TV audio outputs to *Aux_Lin/Aux_Rin*. Setting these bits to xxxxx110 will also mute the TV video outputs and switch the TV audio outputs to *Lin/Rin*.

AUXILIARY COMPOSITE OUTPUT

The auxiliary port includes a composite video output pin (*AUX_YCout*) that is typically connected to the "Video Out" pin on an auxiliary SCART connector. Bits 3-5 in Register 1 determine the source for the *AUX_YCout* pin. When these bits are set to xx000xxx, the video source will be the *Enc_B* input. When these bits are set to xx001xxx, the video source will be the *Enc_YC* input.

AUXILIARY SVHS OUTPUT MODE

The device also includes an output pin (*Aux_Cout*) that provides a chroma output to Pin 15 (RED) on the auxiliary SCART connector. When connected with the Aux_R pin, this forms a bi-directional port as shown in the following diagram:



Using this configuration, the device will support SVHS mode for three encoder interface formats. The first encoder interface format will receive chroma information from the *Enc_C* pin and luma information from the *Enc_Y* pin. This format is designated "SVHS, Enc 1". The second format will receive chroma information on the *Enc_B* input and luma information on *Enc_G*. This format is designated "SVHS, Enc 2". The third format will receive chroma information from the *Enc_R* pin and luma information from the *Enc_G* pin. This mode is designated "SVHS, Enc 3" on the serial port register table.

When the SVHS mode is selected, the DC restore on the *Aux_Cout* pin will average to approximately 0.9 VDC at the video output load. The DC restore on the *Aux_YCout* pin will set the blank level to 0.6 V at the video output load.

AUXILIARY VIDEO MUTE

All auxiliary video outputs can be simultaneously disabled by programming Bits 3-5 in Register 1. The power-up default condition is xx111xxx, which sets all auxiliary video outputs to 0 VDC and switches the auxiliary audio outputs to *Lin/Rin*. Setting these bits to xx110xxx will also mute the auxiliary video outputs.

FUNCTION SWITCHING

The device provides functions switching pins for both the auxiliary (*Aux_Fnc*) and TV (*TV_Fnc*) SCART ports. Both of these pins are bi-directional. The direction of the pins is determined by setting bits in Register 2 according to the following table:

Bits	*Aux_Fnc*	*TV_Fnc*
xxxx**00**xx	**output**	**output**
xxxx01xx	output	input
xxxx10xx	input	output
xxxx11xx	Passthru I/O	Passthru O/I

For the case where Register 2 is set to xxxx11xx, the input signal on the *Aux_Fnc* pin is passed directly through to the *TV_Fnc* pin as an output, or vice versa. This mode is useful for supporting a system power down mode where all signals from the auxiliary port are passed directly through to the TV port.

When a function pin is set as an input, the voltage on that pin is applied to an internal comparitor. The comparitor sense the voltage on the input pin and sets the two (2) LSBs in the read register according to the following table:

Input voltage	Bits	Function
< 4.0 V	xxxxxx00	Normal TV
4.0 to 8.0V	xxxxxx01	16:9 aspect
>8.0 V	xxxxxx10	Peritelevision

When a function pin is set as an output, the output level for the pin is determined by the state of the two LSBs Register 2, according to the following table:

Bits	Output voltage	Function
xxxxxx**00**	**~0 V**	**Normal TV**
xxxxxx01	~6 V	16:9 aspect
xxxxxx10	~ 11 V	Peritelevision
xxxxxx11	~ 11 V	Peritelevision

The function output circuit includes short circuit protection. When a function pin is in the 6V or 11V output mode, if the SCART connection is shorted to ground, then the output is disabled. Likewise, when a function pin is in the 0V output mode, if the SCART connection is connected to a voltage source, then the output is disabled. The load for the function outputs is designed to be 10k or higher.

Note that both the *Aux_Fnc* pin and the *TV_Fnc* pin can be set as outputs simultaneously, however they will have the same output voltage.

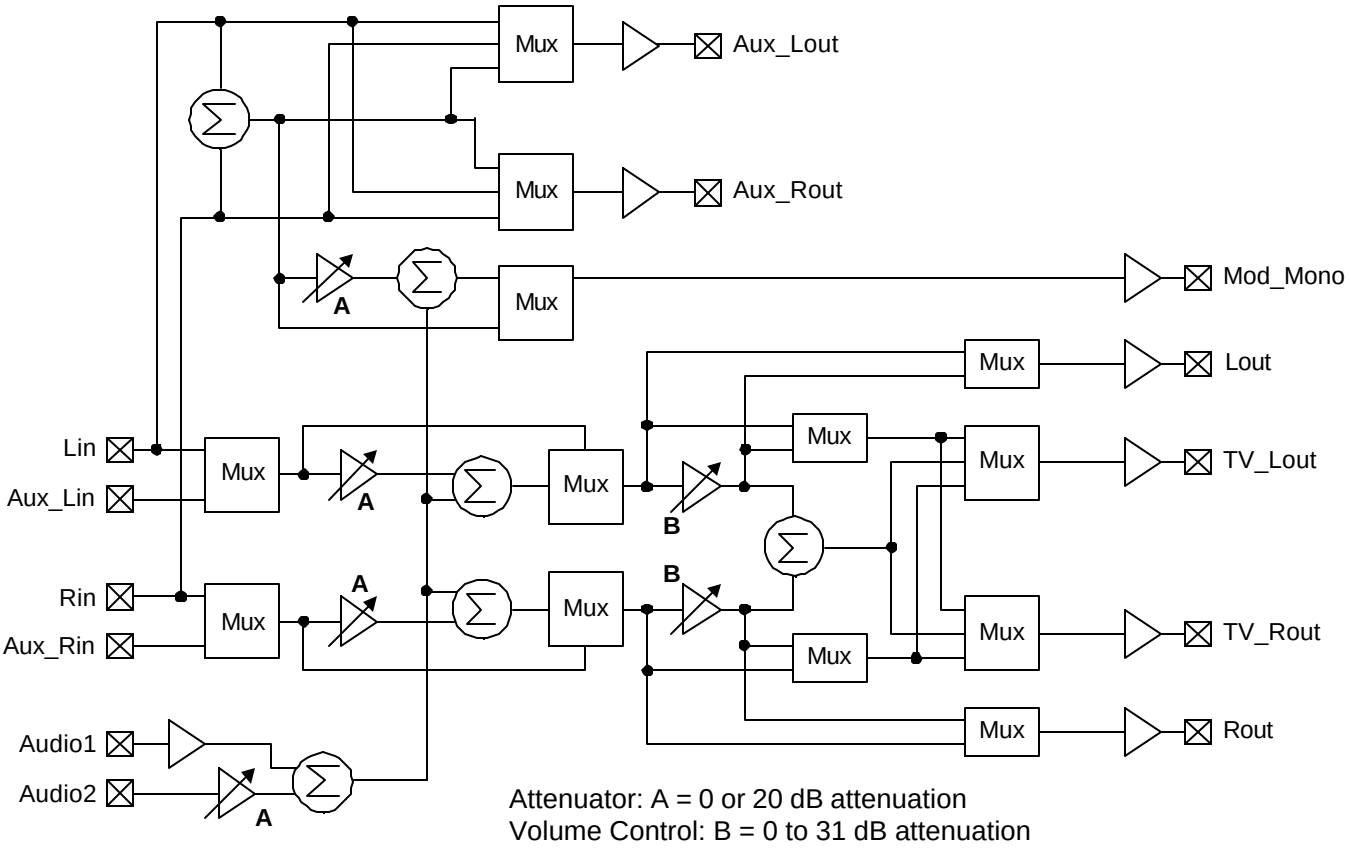


Figure 2: 5002B Audio Switching Block Diagram

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SCART AUDIO SWITCHING

The audio inputs are considered to be associated with the respective video inputs. As a result, the video selection determines which audio signals will be switched to a given SCART output. Refer to the serial port register table for more information. Also see the audio switching block diagram shown in Figure 2.

The 5002B provides inputs for the auxiliary audio source (*Aux_Lin*/*Aux_Rin*) and the stereo DAC associated with the video encoder inputs (*Lin*/*Rin*).

TV AUDIO OPERATION

The audio source for the TV port is selected in concert with the video source using the three (3) LSBs of Register 1. The selected audio signals are input to internal multiplexers that allow the user to select between mono and stereo output options. Bits 4 and 5 of Register 3 control the stereo/mono selection according to the following table:

Bit 5	Bit 4	*TV_Lout source*	*TV_Rout source*
0	**0**	**left input**	**right input**
0	1	left + right	left + right
1	0	left input	left input
1	1	right input	right input

At power-up, these bits default to 00 putting the device in the stereo mode. The outputs of these multiplexers are then passed through a pair of programmable attenuators that are controlled by the two (2) MSBs of Register 4. These register bits provide the following control of the left and right audio channels:

Bit 7	Bit 6	*Left and right channel levels*
0	**0**	**attenuation = 0 dB**
0	1	attenuation = 20 dB
1	x	Both channels disabled

The output of these attenuators are then summed with an audio signal created by summing two additional audio inputs. These additional audio inputs are labeled *Audio1* and *Audio2* on the block diagram. The purpose of these pins is to allow externally generated tones to be mixed with the TV audio signal source.

The state of these two inputs is controlled by Bits 3-5 of Register 4. At power-up reset, Bit 3 is set to a high level (1) which disables the *Audio1* input. Setting this bit low (0) enables the input. The *Audio2* input passes through a programmable attenuator prior to being summed with the *Audio1* input. Bits 4 and 5 of Register 4 control the level of *Audio2* according to the following table:

Bit 5	Bit 4	*Audio2* Mode
0	0	Audio 2 level = 0 dB attenuation
0	1	Audio 2 level = 20 dB attenuation
1	**x**	**Audio 2 input disabled**

At power-up, Bits 4 and 5 are set high (11) so that the input is disabled. The sum of the *Audio1* and *Audio2* signals is then internally summed with each of the left and right TV audio signals.

Volume Control: The resulting left and right TV audio channels are then passed through a volume control circuit. The lower 6-bits in serial port Register 0 set a programmable attenuation level. The attenuation is linear at 1 dB per step with a setting of xx000000 producing 0 dB attenuation and a setting of xx011111 producing 31 dB of attenuation.

TV SCART Audio Outputs: The first pair of signals is labeled *TV_Lout* and *TV_Rout* on the block diagram. *TV_Lout* and *TV_Rout* are typically used to drive the TV SCART audio pins. These outputs also have an internal multiplexer that allows the user to select TV audio either before or after the internal volume control function. When Bit 0 in Register 4 is set low (0), the volume control is used. When this bit is set high (1), the volume control is bypassed. The power-up default state is volume control active.

TV Audio Line Outputs: The second pair of signals is labeled *Lout* and *Rout* on the block diagram. *Lout* and *Rout* are standard line outputs. The *Lout*/*Rout* outputs have an internal multiplexer that allows the user to select TV audio either before or after the internal volume control function. When Bit 1 in Register 4 is set low (0), the volume control is used. When this bit is set high (1), the volume control is bypassed. The power-up default state is volume control active.

RF Mono Output: The *Lin* and *Rin* input signals are summed internally to generate a mono audio signal for an external RF modulator. This output is labeled *Mod_mono*. This mono signal can also be mixed with the *Audio1* and *Audio2*. The switching of the *Audio1* and *Audio2* signals on this pin is controlled by the same bits that control the TV audio outputs. The internal summing circuit is before the volume control mux so the *Mod_mono* output level cannot be adjusted.

TV Audio Mute: A mute function is provided for all *TV* audio outputs. The mute function is controlled by setting Bit 6 in Register 0. When this bit is set to a high state(1), all *TV* audio outputs are attenuated to at least -60 dB. This will be the default condition at power-up. When the bit is set to a low state(0), the audio path will be in normal operating mode. This bit can be set independent of the volume control such that the outputs can be muted before any change in volume, or any switching of audio sources.

AUXILIARY AUDIO OPERATION

The auxiliary port includes stereo audio outputs for a SCART connector (*Aux_Lout*, *Aux_Rout*). The audio inputs *Lin* and *Rin* are the only sources that can be switched to the auxiliary audio outputs for the 5002B device. The audio inputs are switched in concert with the associated video inputs according to Bits 3-5 in Register 1.

Internal multiplexers allow the *Aux_Lout* and *Aux_Rout* outputs to be configured into either stereo or mono audio outputs. The two MSBs of Register 3 control the stereo/mono selection according to the following table:

Bit 7	Bit 6	*Aux_Lout source*	*Aux_Rout source*
0	**0**	**Lin**	**Rin**
0	1	Lin+Rin	Lin+Rin
1	0	Lin	Lin
1	1	Rin	Rin

At power-up, these bits default to 00 putting the device in the stereo mode.

The auxiliary audio outputs can be muted by setting the MSB in Register 0. This bit is set high(1) at power-up causing the outputs to be muted. Setting this bit low(0) enables all auxiliary audio outputs.

DIGITAL OUTPUTS

The 5002B provides two programmable digital outputs, *DO_0* and *DO_1*. These pins are general purpose outputs programmed by setting Bit 0 and 1 in Register 3. Setting the register bits to 0 puts these outputs in the logic low state. Setting the register bits to 1 puts the outputs in the logic high state. Internal pull-up resistors (approximately 30k) are included on these pins.

SERIAL PORT DEFINITION

Internal functions of the device are monitored and controlled by a standard inter-IC (I^2C)bus. The serial port operates in a slave mode only and can be written to or read from. The default address of the device is 1001000x.

DATA TRANSFERS

A data transfer starts when the *SDATA* pin is driven from HIGH to LOW by the bus master while the *SCLK* pin is HIGH. On the following eight clock cycles, the device receives the data on the *SDATA* pin and decodes that data to determine if a valid address has been received. The first seven bits of information are the address with the eighth bit indicating whether the cycle is a read (bit is HIGH) or a write (bit is LOW). If the address is valid for this device, on the falling *SCLK* edge of the eighth bit of data, the device will drive the *SDATA* pin low and hold it LOW until the next rising edge of the *SCLK* pin to acknowledge the address transfer. The device will continue to transmit or receive data until the bus master has issued a stop by driving the *SDATA* pin from LOW to HIGH while the *SCLK* pin is held HIGH

Write Operation: When the read/write bit (bit 8) is LOW and a valid address is decoded, the device will receive data from the *SDATA* pin. The device will continue to latch data into the registers until a stop condition is detected. The device generates an acknowledge after each byte of data written.

Read Operation: When the read/write bit (bit 8) is HIGH and a valid address is decoded, the device will transmit the data from the internal register on the following eight *SCLK* cycles. Following the transfer of the register data and the acknowledge from the master, the device will release the data bus.

Reset: At power-up the serial port defaults to the states indicated in boldface type. The device also responds to the system level reset that is transmitted through the serial port. When the master sends the address 00000000 followed by the data 00000110, the device resets to the default condition. The device also generates an acknowledge.

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Serial Port Register Tables
Read register Device Address = 10010001

FUNCTION	BITS	DESCRIPTION
Function Control Input	xxxxxx00 xxxxxx01 xxxxxx10	TV_Fnc or AUX_Fnc pin level = Level 0 (~0V) TV_Fnc or AUX_Fnc pin level = Level 1A (~6.0V) TV_Fnc or AUX_Fnc pin level = Level 1B (~12V)
TV_YCout video sync	xxxxx0xx xxxxx1xx	TV ycout: no sync pulse present TV ycout: sync pulse present
AUX_YCout video sync	xxxx0xxx xxxx1xxx	AUX ycout: no sync pulse present AUX ycout: sync pulse present
Device ID code	0010xxxx	This code identifies the device type as the 5002B

Write Registers: Device Address = 10010000 (**Bold** indicates default setting)
Register 0: Audio Control Register A

FUNCTION	BITS	DESCRIPTION
TV Volume Control	xx**000000** xx011111	**TV audio volume = normal (0 dB attenuation)** TV audio volume = minimum (31 dB attenuation)
TV audio mute	x0xxxxxx x**1**xxxxxx	TV audio (*TV_Lout/TV_Rout, Lout/Rout, Mod_mono*) output = normal audio output **TV audio (*TV_Lout/TV_Rout, Lout/Rout, Mod_mono*) output = Muted by 60 dB**
AUX audio mute	0xxxxxxx **1**xxxxxxx	AUX audio (*AUX_Lout/AUX_Rout*) output = normal audio output **AUX audio (*AUX_Lout/AUX_Rout*) output = Muted by 60 dB**

Register 1: Audio/Video Control Register; audio/video source select bits

TV A/V source	**Bits**	***TV_R***	***TV_G***	***TV_B***	***TV_YC***	***Mod_YC***	***L,Rout***
RGB/YC, Encoder	xxxxx000	Enc_R	Enc_G	Enc_B	Enc_YC	Enc_YC	Lin, Rin
RGB/YC, Auxiliary	xxxxx001	Aux_R	Aux_G	Aux_B	Aux_YC	Enc_YC	AuxLin,Rin
SVHS, Enc 1	xxxxx010	Enc_C	0V	0V	Enc_Y	Enc_YC	Lin, Rin
SVHS, Enc 2	xxxxx011	Enc_B	0V	0V	Enc_G	Enc_YC	Lin, Rin
SVHS, Enc 3	xxxxx100	Enc_R	0V	0V	Enc_G	Enc_YC	Lin, Rin
SVHS, Aux 1	xxxxx101	Aux_R	0V	0V	Aux_YC	Enc_YC	AuxL,Rin
TV mute	xxxxx110	0V	0V	0V	0V	0V	Lin, Rin
TV mute	xxxxx**111**	**0V**	**0V**	**0V**	**0V**	**0V**	AuxL,Rin

Aux A/V source	**Bits**	***Aux_Cout***	***Aux_YCout***	***Aux_Lout, Rout***
Composite, Enc 1	xx000xxx	off	Enc_B	Lin, Rin
Composite, Enc 2	xx001xxx	off	Enc_YC	Lin, Rin
Composite, Enc 2	xx010xxx	off	Enc_YC	Lin, Rin
SVHS, Enc 1	xx011xxx	Enc_C	Enc_Y	Lin, Rin
SVHS, Enc 2	xx100xxx	Enc_B	Enc_G	Lin, Rin
SVHS, Enc 3	xx101xxx	Enc_R	Enc_G	Lin, Rin
Aux mute	xx110xxx	0V	0V	Lin, Rin
Aux mute	xx**111**xxx	**0V**	**0V**	Lin, Rin

Function	**Bits**	**Description**
Not used	x**0**xxxxxx	Reserved, set to 0 for normal operation
RGB Sync Source	**0**xxxxxxx	**RGB sync /DC restore source = RGB**
	1xxxxxxx	RGB sync /DC restore source = TV_YC

Register 2: Video Control Register; video function bits

Function	Bits	Description
Function Control Output Voltage	xxxxxx**00**	**Level 0; normal TV output (Function Voltage = 0V)**
	xxxxxx01	Level 1A; 16:9 aspect ratio (Function Voltage = 6V)
	xxxxxx10	Level 1B; Peritelevision output mode (Function Voltage = 11V)
	xxxxxx11	Level 1B; Peritelevision output mode (Function Voltage = 11V)
Function Pins Control*	**xxxx00xx**	**Aux_Fnc pin = output, TV_Fnc pin = output**
	xxxx01xx	Aux_Fnc pin = output, TV_Fnc pin = input
	xxxx10xx	Aux_Fnc pin = input, TV_Fnc pin = output
	xxxx11xx	Signals will pass through from Aux_Fnc to TV_Fnc or vice versa.
RGB Gain Control	xx**00**xxxx	**RGB output amplifier gain = normal**
	xx01xxxx	RGB output amplifiers attenuated by 10%
	xx10xxxx	RGB output amplifiers attenuated by 20%
	xx11xxxx	RGB output amplifiers attenuated by 30%
BLANK output selection	**00**xxxxxx	**BLANK = ABLANK**
	01xxxxxx	BLANK = EBLANK
	10xxxxxx	BLANK = 0V
	11xxxxxx	BLANK = 4V @ IC output pin

* Function pin voltages: (I) in output mode are defined by the two LSB of register 2, (II) in input mode set the state of the two LSB of the read register.
Digital read is not meaningful in the pass-through mode(xxxx11xx).

Register 3: Audio control register B

Function	Bits	Description
D0 output control	xxxxxxx**0**	**D0 output = 0 (low)**
	xxxxxxx1	D0 output = 1 (high)
D1 output control	xxxxxx**0**x	**D1 output = 0 (low)**
	xxxxxx1x	D1 output = 1 (high)
Not used	xxxx**00**xx	Reserved, set to 0 for normal operation
TV Stereo/mono control	xx**00**xxxx	**TV audio mode: stereo**
	xx01xxxx	TV audio mode: mono (sum L+R) on both TV_Lout/TV_Rout
	xx10xxxx	TV audio mode: L channel on both TV_Lout/TV_Rout
	xx11xxxx	TV audio mode: R channel on both TV_Lout/TV_Rout
Aux Stereo/mono control	**00**xxxxxx	**Aux audio mode: stereo**
	01xxxxxx	Aux audio mode: mono (sum L+R) on both Aux_Lout/Aux_Rout
	10xxxxxx	Aux audio mode: L channel on both Aux_Lout/Aux_Rout
	11xxxxxx	Aux audio mode: R channel on both Aux_Lout/Aux_Rout

Register 4: Audio control register C

Function	Bits	Description
TV volume control select 1	xxxxxxx**0** xxxxxxx1	**Volume control on TV_Lout, TV_Rout** TV_Lout, TV_Rout bypass the volume control
TV volume control select 2	xxxxxx**0**x xxxxxx1x	**Volume control on Lout, Rout** Lout, Rout bypass the volume control
Not used	xxxxx**0**xx	Reserved, set to 0 for normal operation
Audio1 control (Note 1)	xxxx0xxx xxxx**1**xxx	Audio1 input is active **Audio1 input disabled**
Audio2 control	xx00xxxx xx01xxxx **xx1xxxxx**	Audio2 level = 0 dB attenuation Audio2 level = 20 dB attenuation **Audio2 input disabled**
TV source mixer control (Note 2)	**00**xxxxxx 01xxxxxx 1xxxxxxx	**TV source = 0 dB attenuation** (bypass attenuator/summing node) TV source level = 20 dB attenuation TV source disabled

Note 1 Audio1 exhibits excessive DC offset in the disabled state(xxxx1xxx). This DC offset can propagate to audio outputs Lout, Rout, TV_Lout and TV_Rout if care is not taken. There are two ways to avoid excessive DC offset at the audio outputs:

1. Activate Audio1 with register setting xxxx0xxx. The input pin can be either left floating or actively driven, or
2. Bypass attenuator 'A' and the summing node with register code 00xxxxxx. By bypassing the summing node, the offset at Audio1 will be blocked from the audio path. In this case, the state of Audio1 control does not impact output DC offset.

Note 2 This effects both the TV audio outputs (TV_Lout, TV_Rout, Lout, Rout) and the Mod_mono audio output.

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SCART Switching Table

INPUT PINS	OUTPUT PIN
Aux_R: Red input from Aux port Enc_R: Red input from Enc port Enc_B: Optional chroma input from Enc port Enc_C: Chroma input from Enc port	TV_R: Red video output to TV or SVHS chroma output to TV port
Aux_G: Green input from Aux port Enc_G: Green input from Enc port	TV_G: Green video output to TV port
Aux_B: Blue input from AUX SCART Enc_B: Blue input from Enc port	TV_B: Blue video output to TV port
ABLANK: Blanking input from Aux port EBLANK: Blanking input from Enc port	BLANK: TV blanking output for RGB (also can output 0V or 4V at this pin)
Aux_YC: Composite input from Aux port Enc_YC: Composite input from Enc port Enc_Y: Luma input from Enc port Enc_G: Optional luma input from Enc port	TV_YCout: Composite video, RGB sync, or Luma output to TV port
Enc_YC: Composite input from Enc port	Mod_YC: Composite output to RF modulator
Enc_C: Chroma input from Enc port Enc_R: Optional chroma input from Enc port Enc_B: Optional chroma input from Enc port	Aux_Cout: Chroma output to auxiliary port
Enc_YC: Composite input from Enc port Enc_B: Optional composite input from Enc port Enc_G: Optional luma input from Enc port Enc_Y: Luma input from Enc port	Aux_YCout: Composite video output to auxiliary port
Aux_Lin: Left audio input from Aux port Lin: Left audio input from audio DAC Audio1: External audio source Audio2: External audio source	Lout: Left audio output to RCA jack
Aux_Lin: Left audio input from Aux port Lin: Left audio input from audio DAC Audio1: External audio source Audio2: External audio source	TV_Lout: Left audio output to TV port
Lin: Left audio input from audio DAC	Aux_Lout: Left audio output to auxiliary port
Aux_Rin: Right audio input from Aux port Rin: Right audio input from audio DAC	Rout: Right audio output to RCA jack
Aux_Rin: Right audio input from Aux port Rin: Right audio input from audio DAC	TV_Rout: Right audio output to TV port
Rin: Right audio input from audio DAC	Aux_Rout: Right audio output to auxiliary port
Rin: Right audio input from audio DAC Lin: Left audio input from audio DAC Audio1: External audio source Audio2: External audio source	Mod_mono: Mono audio output to RF modulator.

PIN DESCRIPTIONS (Pins marked N/C should be left unconnected during normal use.)

NAME	TYPE	DESCRIPTION
Analog Pins		
ABLANK	I	Auxiliary Blanking Input: In a typical system, this pin is connected to the RGB status pin (pin 16) from the auxiliary SCART connector.
Aux_R	I	Auxiliary Red Input: In a typical system, this pin is connected to the RED input pin (pin 15) of the auxiliary SCART connector. This input can be selected as the signal source for the *TV_R* output pin.
Aux_G	I	Auxiliary Green Input: In a typical system, this pin is connected to the GREEN input pin (pin 11) of the auxiliary SCART connector. This input can be selected as the signal source for the *TV_G* output pin.
Aux_B	I	Auxiliary Blue Input: In a typical system, this pin is connected to the BLUE input pin (pin 7) of the auxiliary SCART connector. This input can be selected as the signal source for the *TV_B* output pin.
Aux_Fnc	I/O	Auxiliary Function Pin: This is a bi-directional pin. As an input, it digitizes the analog voltage on the auxiliary SCART function pin. As an output, it puts out one of three voltage levels to the auxiliary SCART function pin.
Aux_YC	I	Auxiliary Video Input: In a typical system, this pin is connected to the composite video input pin (pin 20) of the auxiliary SCART connector. This input can be selected as the signal source for the *TV_YCout*.
Aux_Lin	I	Auxiliary Left Audio Input: In a typical system, this pin is connected to the L Audio Output pin (pin 3) of the auxiliary SCART connector. This input can be selected as the signal source for the *TV_Lout*.
Aux_Rin	I	Auxiliary Right Audio Input: In a typical system, this pin is connected to the R Audio Output pin (pin 1) of the auxiliary SCART connector. This input can be selected as the signal source for the *TV_Rout*.
EBLANK	I	Encoder Blanking Input: In a typical system, this pin is connected to the blanking signal from the external video encoder device.
Enc_R	I	Encoder Red Input: In a typical system, this pin is connected to the RED output pin from the external video encoder device. This input can be selected as the signal source for the *TV_R* output pin.
Enc_G	I	Encoder Green Input: In a typical system, this pin is connected to the GREEN output pin from the external video encoder device. This input can be selected as the signal source for the *TV_G* output pin.
Enc_B	I	Encoder Blue Input: In a typical system, this pin is connected to the BLUE output pin from the external video encoder device. This input can be selected as the signal source for the *TV_B* output pin.

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PIN DESCRIPTIONS (continued)

NAME	TYPE	DESCRIPTION
Enc_YC	I	Encoder Video Input: In a typical system, this pin is connected to the composite video output pin from the external video encoder device. This input can be selected as the signal source for the *AUX_YCout*, *TV_YCout* and/or *Mod_YC* pins.
Enc_Y	I	Encoder Luma Input: In a typical system, this pin is connected to the composite video output pin from the external video encoder device. In SVHS mode, this input can be selected as the signal source for the *TV_YCout* pin and/or the *Aux_YCout* pin.
Enc_C	I	Encoder Chroma Input: In a typical system, this pin is connected to the *TV_R* output pin from the external video encoder device. In the SVHS mode, this input can be selected as the signal source for the *TV_R* pin and/or the *Aux_Cout* output pin.
Lin	I	Left Audio Input: In a typical system, this pin is connected to the left audio output pin of the external audio DAC. This input can be selected as the signal source for the *TV_Lout* and/or *Aux_Lout* pins.
Rin	I	Right Audio Input: In a typical system, this pin is connected to the right audio output pin of the external audio DAC. This input can be selected as the signal source for the *TV_Rout* and/or *Aux_Rout* pins.
Audio 1	I	External tone input: This pin accepts an external tone that can be output to the TV audio outputs.
Audio 2	I	External tone input: This pin accepts an external tone that can be output to the TV audio outputs.
Aux_YCout	O	Auxiliary Video Output: This pin is the composite video output to the auxiliary SCART connector (pin 19). In the SVHS mode, this pin is the luma output.
Aux_Lout	O	Auxiliary Left Audio Output: This pin is the output to the left channel audio (pin 3) of the auxiliary SCART connector.
Aux_Rout	O	Auxiliary Right Audio Output: This pin is the output to the right channel audio (pin1) of the auxiliary SCART connector.
BLANK	O	Blanking output: This output provides the blanking signal to the TV SCART connector (pin 16). This signal is either the blanking signal from the auxiliary SCART connector (*ABLANK*) or the external video encoder (*EBLANK*).
Lout	O	Left Audio Output: This pin is the output to the left channel audio RCA jack.
Rout	O	Right Audio Output: This pin is the output to the right channel audio RCA jack.
Mod_Mono	O	Mono Audio Output: This pin is sum of Lin & Rin audio inputs. It is typically used as the audio output to an external RF modulator.

PIN DESCRIPTIONS (continued)

NAME	TYPE	DESCRIPTION
Aux_Cout	O	Aux Chroma Output: This output provides a chroma signal to the auxiliary SCART connector to support SVHS operation. This pin is typically AC coupled to pin 15 of the auxiliary SCART connector. When the S-video mode is selected, a chroma signal from the video encoder is output to this pin.
Mod_YC	O	TV Modulator Video Output: This pin provides composite video for an external RF modulator. The signal on this pin is provided by the *Enc_YC* input pin.
TV_YCout	O	TV Video Output: This pin is the composite video output to the TV SCART connector (pin 19). In the SVHS mode, this pin provides luminance information.
TV_R	O	TV Red Output: This pin provides Red video to the TV SCART connector (pin 15). In SVHS mode, this pin provides the chroma information.
TV_G	O	TV Green Output: This pin provides Green video to the TV SCART connector (pin 11).
TV_B	O	TV Blue Output: This pin provides Blue video to the TV SCART connector (pin 7).
TV_Lout	O	TV Left Audio Output: This pin is the output to the left channel audio (pin 3) of the TV SCART connector.
TV_Rout	O	TV Right Audio Output: This pin is the output to the right channel audio (pin1) of the TV SCART connector.
TV_Fnc	I/O	TV Function Pin: This is a bi-directional pin. As an input, it digitizes the analog voltage on the TV SCART function pin. As an output, it puts out one of three voltage levels to the TV SCART function pin.
Digital Pins		
DO_0	O	Digital Output 0: This pin is a general purpose output that is controlled by serial port register.
DO_1	O	Digital Output 1: This pin is a general purpose output that is controlled by serial port register.
SCLK	I	Serial Clock Input: This pin accepts a serial port clock input signal.
SDATA	I/O	Serial Data Input: This is a tri-state pin that receives or transmits serial data.
Power/Ground Pins		
VCC	-	+5 VDC power inputs.
VEE	-	-5 VDC power inputs.
VDD	-	+12 VDC power input for function switching
Vref	-	Internal voltage reference, bypass pin. Add capacitor 0.01 µF to ground.
GND	-	Ground for all blocks.
Rbias	-	Bias point of internal current generator. Add resistor 10.0k to ground.
Tgen	-	Reference point for internal timing circuit. Add capacitor 470 pF to ground.

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Dual SCART A/V Switch

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS
Operation beyond the maximum ratings may damage the device

PARAMETER	RATING
Storage temperature	-55 to 150 °C
Junction operating temperature	+150 °C
Positive supply voltages	-0.3V < VCC < 6V; VCC – 0.3V < VDD < 13V
Negative supply voltages	-6 < VEE < +0.3V
Voltage applied to Digital Inputs	Gnd-0.3V to VCC+0.3 V
audio/video input pins	VEE-0.3V to VCC+0.3 V
function input pins (300 Ω source)	Gnd-0.3V to +15 V

SPECIFICATIONS: Unless otherwise specified: 0° < Ta < 70 °C; power supplies VCC = +5.0 V ±5%, VEE = -5.0 V ±5%, VDD = 12.0 V ±5%.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
OPERATING CHARACTERISTICS					
Power Supply Currents	All outputs loaded VCC (+5 VDC) VEE (-5 VDC) VDD (+12 VDC)	 -65	 130 –45 18	 150 28	 mA mA mA
PSRR	f_{in} = 100 Hz, 0.3 Vpp on VCC/ VEE	40			dB
Switch time	From serial data acknowledge		2.0		µsec
Serial Port Timing (set by I^2C controller)					
SCLK Input Frequency				400	kHz
SCLK LOW time (t_{CL})		1.3			µsec
SCLK HIGH time (t_{CH})		0.6			µsec
Rise time (t_{RT})	*SCLK* and *SDATA*			300	nsec
Fall time (t_{FT})	*SCLK* and *SDATA*			300	nsec
Data set-up time* (t_{DSU})	*SDATA* change to *SCLK* HIGH	100			nsec
Data hold time* (t_{DH})	*SCLK* LOW to *SDATA* change	0			nsec
Start set-up time (t_{SSU})		0.6			µsec
Start hold time (t_{SH})		0.6			µsec
Stop set-up time (t_{PSU})		0.6			µsec
Glitch rejection	maximum pulse on *SCLK* and/or *SDATA*			50	nsec
* These specifications also apply to an acknowledge generated by the device.					

SPECIFICATIONS (continued)

Digital I/O Characteristics (SCLK, SDATA)					
PARAMETER	**CONDITION**	**MIN**	**NOM**	**MAX**	**UNIT**
High level input voltage		0.7* VCC		VCC+0.3	V
Low level input voltage		GND-0.3		0.3* VCC	V
High level input current	Vin = Vcc - 1.0V	-10		10	µA
Low level input current	Vin = 1.0V	-10		10	µA
Low level output voltage (SDATA)	I_{OL} = 3 mA			0.4	V
Fall time (t_{FT})(SDATA) acknowledge or read	V_{IH} MIN to V_{IL} Max with CL = 400 pF			250	nsec
Digital I/O Characteristics (DO_0, DO_1, TV_Fnc, Aux_Fnc)					
Digital output sink current 4.5k pullup	DO_0, DO_1, Register bits read 0		1.0		mA
Digital output fall time	R_{pullup} = 10 kΩ, C_L = 15 pF		100		nsec
TV_Fnc or Aux_Fnc output level 10 k or open load	Register 2 = xxxxxx00 Register 2 = xxxxxx01 Register 2 = xxxxxx10 or 11	0.0 4.9 10.0	1.0 6.0 10.5	1.2 6.5 VDD	V V V
TV-Fnc or AUX_Fnc input levels	Read Register= xxxxxx00 Read Register= xxxxxx01 Read Register= xxxxxx10	0.0 4.5 9.5		2.0 7.0 VDD	V V V

Video Characteristics - Unless otherwise noted, typical output loading on all video outputs is 137Ω. All video outputs are capable of withstanding a sustained 62ohm load to ground without damage.

Input impedance	All video inputs	100			kΩ
Input dynamic range	f_{in} = 100 kHz, THD < 1.0%, at DC floor level of 0.3 V		1.5		Vpp
Gain	1.0 Vpp input, f_{in} = 100 kHz	1.73	1.83	1.93	V/V
RGB Gain control A_0 = nominal xx00xxxx gain	1.0 Vpp input, f_{in} = 100 kHz; Register 2 = xx00xxxx Register 2 = xx01xxxx Register 2 = xx10xxxx Register 2 = xx11xxxx	 1.73 A_0 –12% A_0 –22% A_0 –33%	 1.83 A_0 –10% A_0 –20% A_0 –30%	 1.93 A_0 –8% A_0 –18% A_0 –27%	 V/V V/V V/V V/V
Output gain inequality	RGB or SVHS output channel to channel	-2.5		2.5	%
Video Output DC level					V
Blank level clamp voltage	RGB, CVBS or luma outputs		1.2		V
Average level	chroma outputs		1.9		V
Signal to noise ratio	1 Vpp input	58	65		dB
Cross talk	f_{in} = 4.43 MHz, 1 Vpp		-55		dB
Output to output differential delay	RGB signals, f_{in} = 100 kHz	-20		20	nsec
Blanking level (Rapid Switching)	Input or output, logical “0”	0.0		0.4	V
	Input or output, logical “1”	1.0		3.0	V
Blanking delay	BLANK to RGB signals	-50		50	nsec
Differential phase	All composite outputs	-2.5		2.5	Deg.
Differential gain	All composite outputs	-5.0		5.0	%

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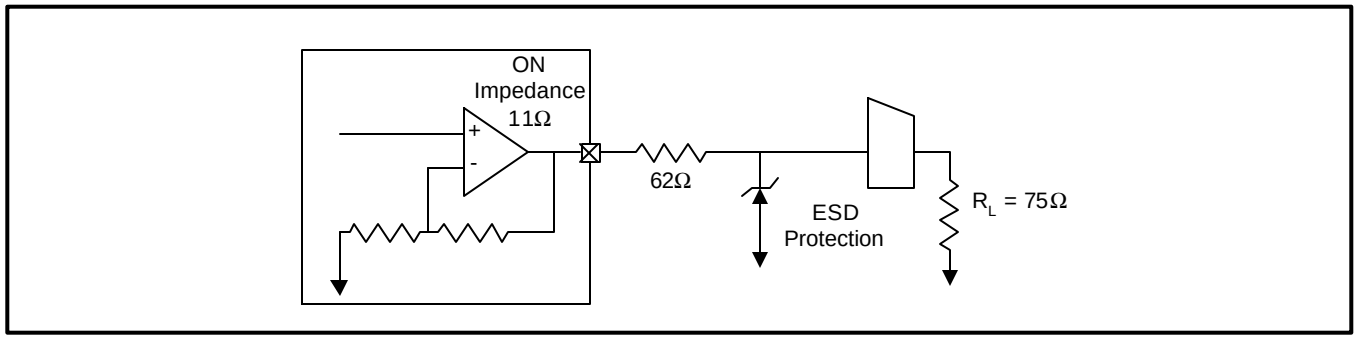
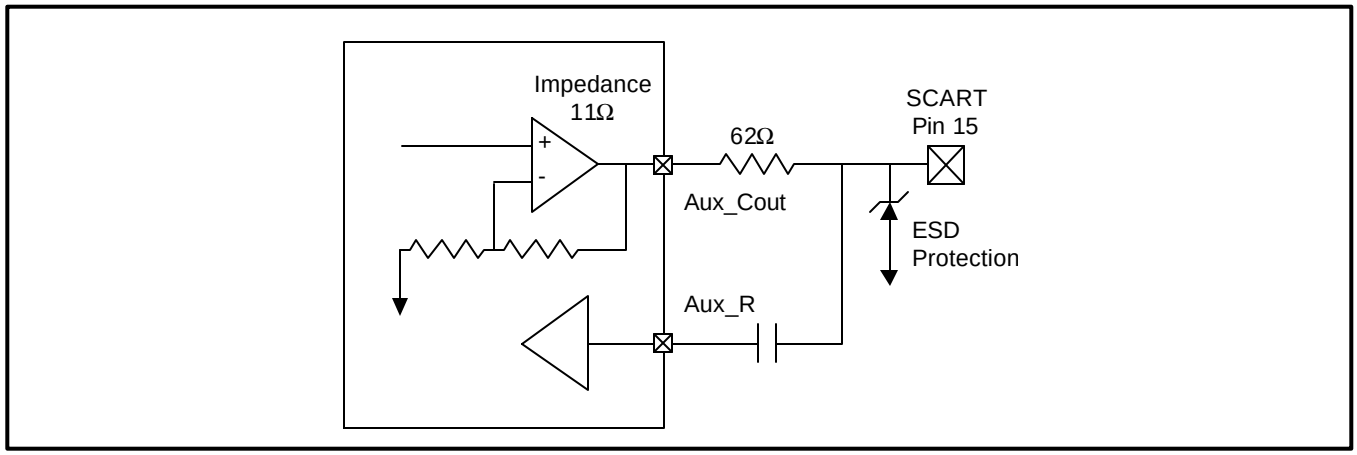
Audio Characteristics - Unless otherwise noted, all audio outputs shall drive a load of 10 kΩ. All audio outputs will withstand a sustained short to ground without damage.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Input impedance			75		kΩ
Gain	f_{in}=1.0 kHz, 0.5 Vrms,0dB attenuation	0.95	1.0	1.05	V/V
Frequency response	0.5 Vrms input, Flat within ± 0.3 dB	20			kHz
	Measured -3 dB point	100			kHz
Signal to Noise ratio A weighting	f_{in} = 1.0 kHz, 2.0 Vrms; Register 4 = 00111011	90			dB
Distortion (THD)	f_{in} = 1.0 kHz, 0.5 Vrms; Register 4 = 00111011			0.05	%
	f_{in} = 1.0 kHz, 2 Vrms; Register 4 = 00111011			0.10	%
Output impedance			10		Ω
Output DC Offset at Aux_Lout and Aux_Rout		-40		30	mV
Output DC Offset at Mod_Mono		-75		30	mV
Output DC Offset at Lout, Rout, TV_Lout and TV_Rout	TV Source Attenuator = 0 dB (Bypassed) With Volume Control	-65		30	mV
	TV Source Attenuator = 0 dB (Bypass) Bypass Volume Control	-50		30	mV
	TV Source Attenuator = -20 dB Or Disabled, Audio1 active With Volume Control	-90		30	mV
	TV Source Attenuator = -20 dB Or Disabled, Audio1 active Bypass Volume Control	-75		30	mV
Output phase matching	f_{in} = 1.0 kHz, 0.5 Vrms; any stereo pair		0.5		Deg.
Channel separation	f_{in} = 1.0 kHz, 2.0 Vrms, 0 dB attenuation	90			dB
Output attenuation (volume control)	TV_Lout/TV_Rout; Lout/Rout				
	Register 0 = x0000000; Register 4 = 00111000		0		dB
	Register 0 = x0011111; Register 4 = 00111000		-31		dB
	Register 0 = x1xxxxxx (MUTE) ; Register 4 = 00111000		-60		dB
Attenuation accuracy		-5		5	%
Audio to video path skew	Video input = 1.0 Vpp @ 100 kHz Audio input = 1.0 kHz, 0.5 Vrms		1.5		µsec

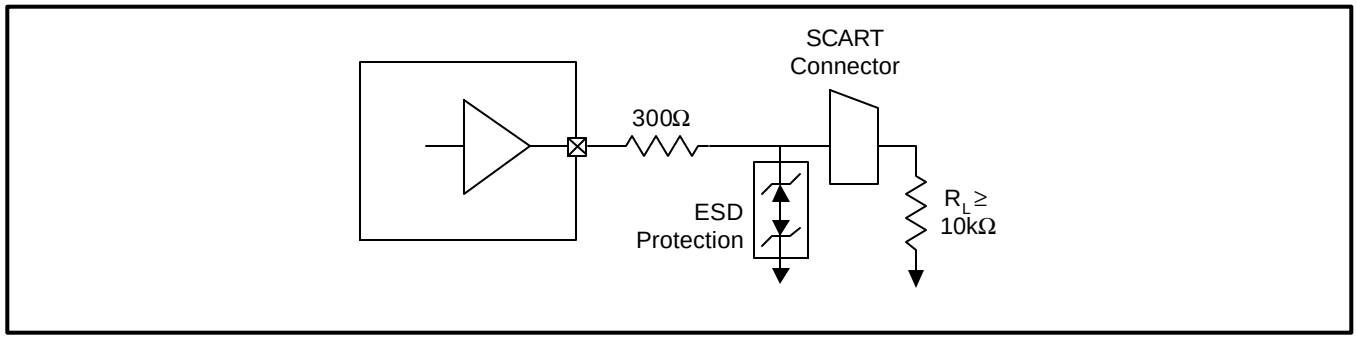
Equivalent Circuits:



Video Output Circuit



Auxiliary SCART pin 15 Circuit



Audio Output Circuit

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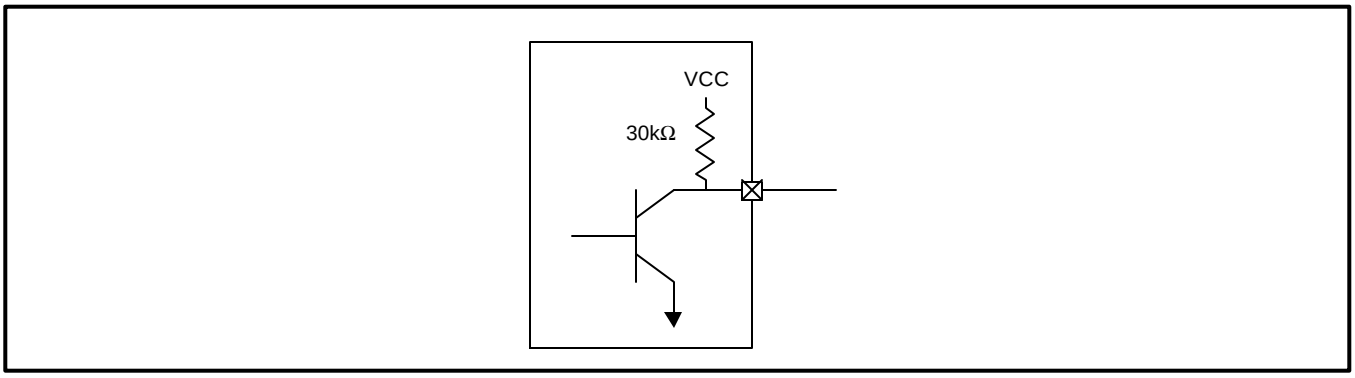
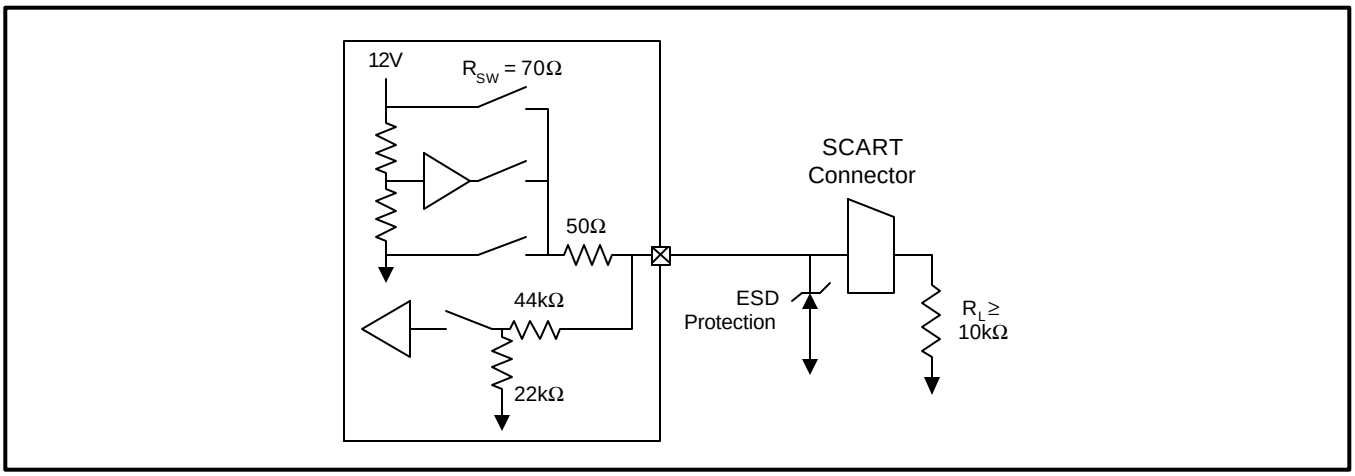
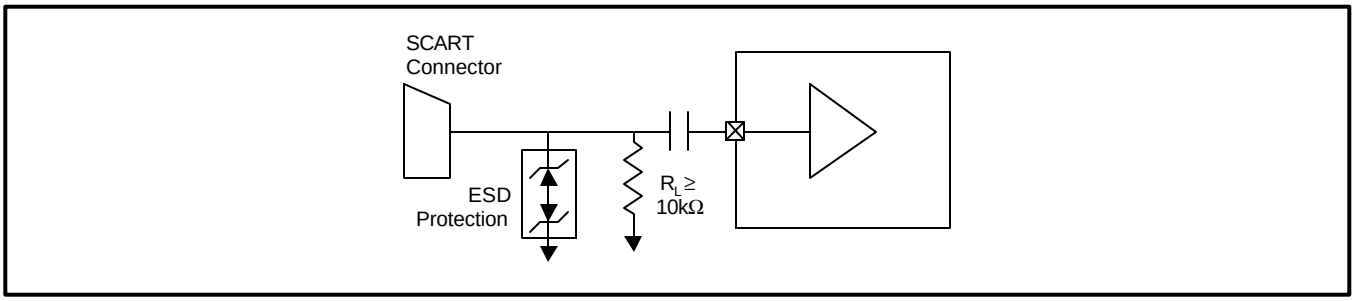


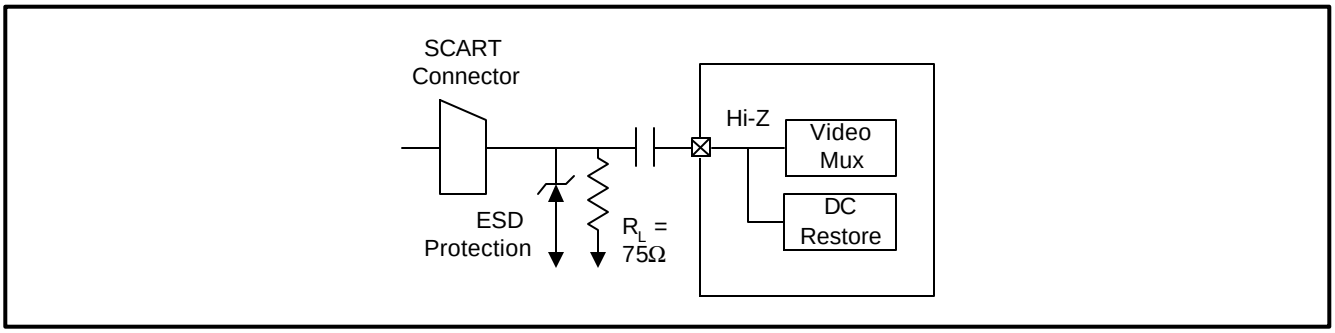
Digital Output Circuit



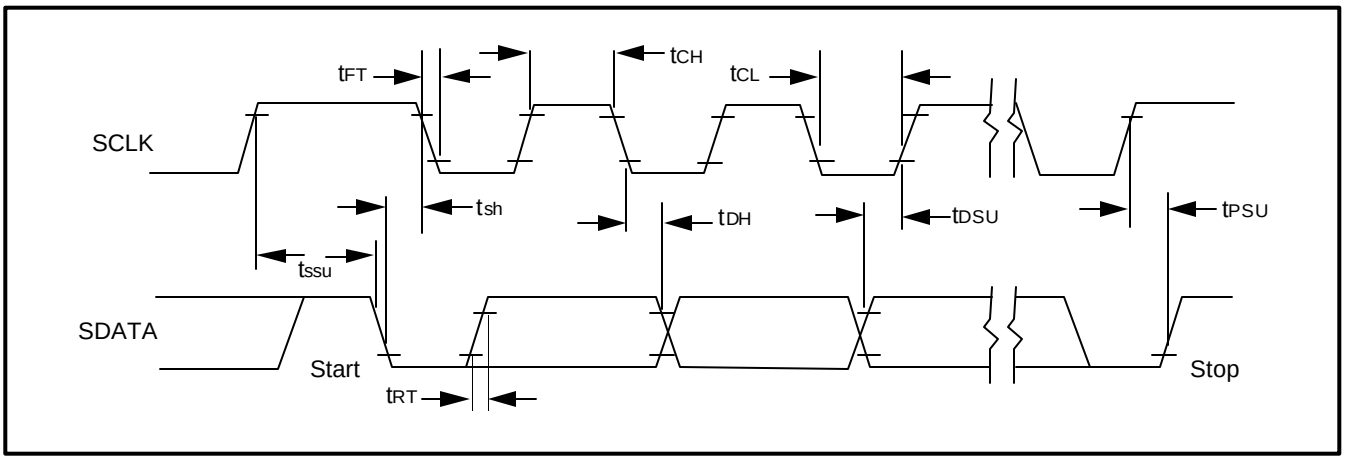
AUX and TV Function Switching Circuit



Audio Input Circuit



Video Input (Typical)



Serial Port Timing (Typical)

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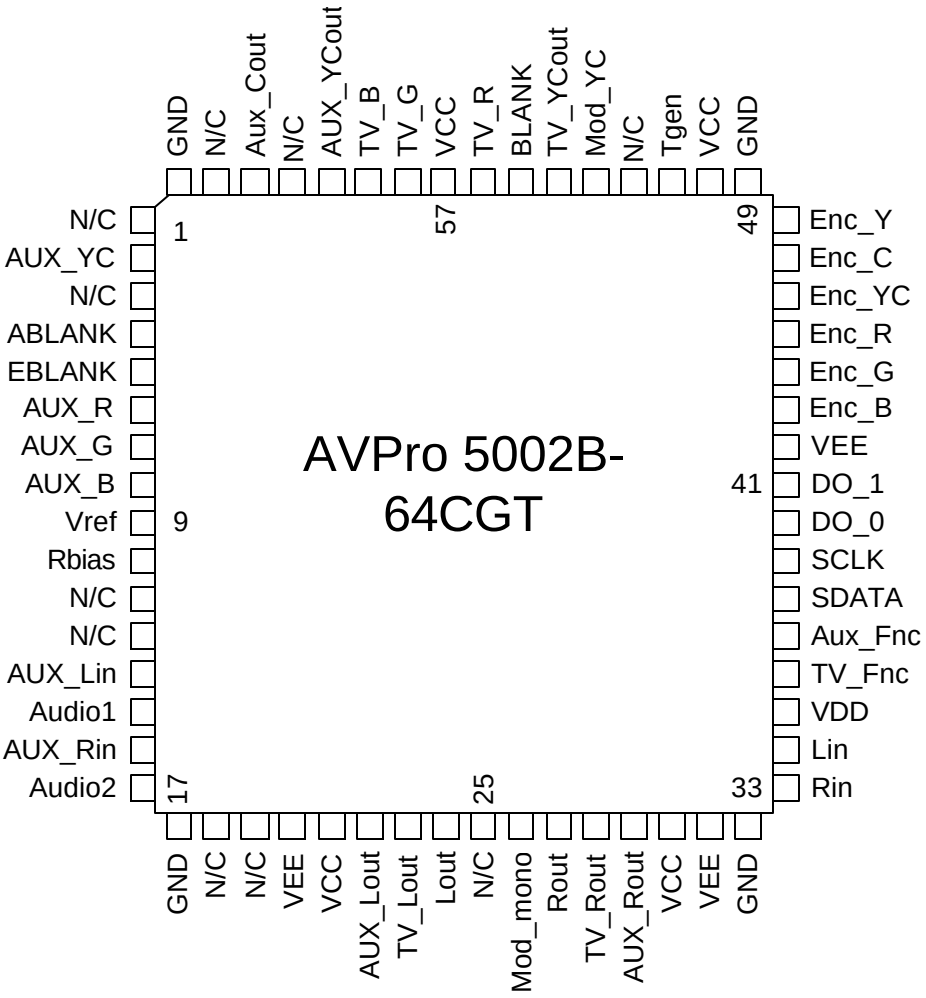
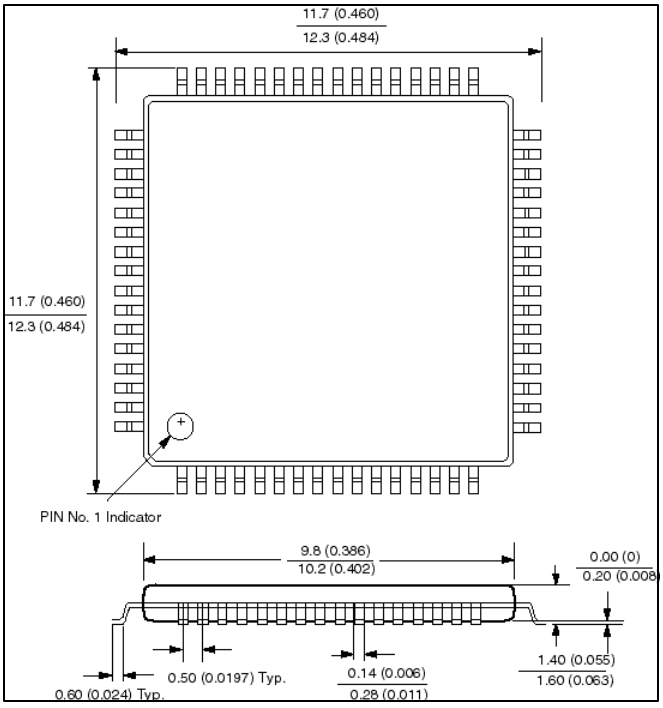
PACKAGE PIN DESIGNATIONS
(Top View)



AVPro® 5002B-CGT (64 LQFP)

MECHANICAL DRAWING



64-Lead Low Profile Plastic Quad Flatpack Package(JEDEC LQFP)

Note: Controlling dimensions are in mm.

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PACKAGE MARK
AVPro® 5002B Dual SCART A/V Switch	5002BXXA64CGT	AVPro® 5002B-CGT

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 8/07/00 Rev. D