



## EVALUATION BOARD FOR Si53x XOs AND Si55x VCXOs

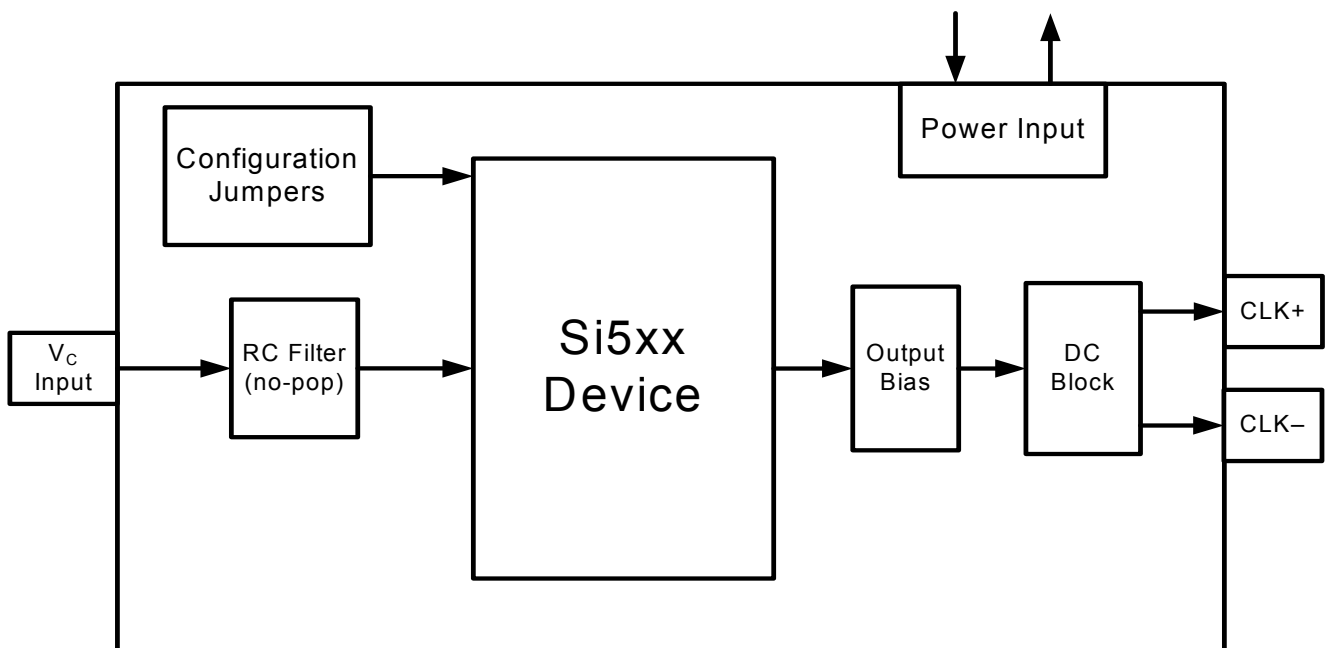
### Description

This document describes the operation of the Silicon Laboratories Si5xx-EVB evaluation board to evaluate both Silicon Laboratories' Si55x VCXOs and Si53x XOs. The Si55x and Si53x devices use Silicon Laboratories' advanced DSPLL<sup>®</sup> circuitry to provide a low-jitter clock at high frequencies. The Si55x/Si53x IC-based device is factory configurable for a wide variety of user specifications including frequency, supply voltage, output, and tuning slope. Specific configurations are factory programmed into the Si55x/Si53x at time of shipment, thereby eliminating the long lead times associated with custom oscillators. Si55x/Si53x samples should be ordered at the same time as the Si5xx-EVB since the EVB does not come with the device. This allows end users maximum flexibility. Silicon Laboratories can solder down samples when ordering an EVB; please specify when ordering.

### Features

- Evaluation of Silicon Laboratories' Si55x/53x family
- AC-coupled differential output clocks
- Voltage control ( $V_C$ ) input port (for Si55x devices)
- Jumper selection for multi-frequency outputs
- Jumper selection for output enable

### Functional Block Diagram



# Si5xx-EVB

## 1. Functional Description

The Si5xx-EVB provides access to all signals for configuring and operating the device. This board allows evaluation of the Si55x VCXO device either by itself (open-loop) or within a prototype PLL (closed-loop). The performance of the Si53x XO device can also be evaluated on this board (the Vc port is not used for XO devices).

**Table 1. Jumper Control**

Part Type	JP1	JP2	JP3	JP4
Si530	N/A	N/A	OE	N/A
Si532	N/A	N/A	OE	Freq Sel
Si534	Freq Sel1	Freq Sel2	OE	N/A
Si550	N/A	N/A	OE	V <sub>C</sub>
Si552	N/A	N/A	Freq Sel	V <sub>C</sub>
Si554	Freq Sel1	Freq Sel2	OE	V <sub>C</sub>

**Notes:**

1. With jumper(s) installed, signal(s) are driven low.
2. With jumper(s) not installed, signal(s) are pulled high.

### 1.1. Power Supply

The Si55x/Si53x devices support operation from nominal voltages of 1.8, 2.5, and 3.3 V. Review the device data sheet and part number for allowed configurations of output buffer type and device power supply.

### 1.2. Voltage Control for VCXOs

The voltage control (V<sub>C</sub>) input of the Si55x device is conveniently accessible through an SMA jack (J3) but can also be driven (and observed) through 100 mil-centered posts (JP4). For prototyping purposes, two 0603 solder pads are located near the device V<sub>C</sub> input (R3 and C3). A traditional PLL might use these as a single-time-constant low-pass filter (RC filter). The EVB is shipped with a 0 Ω resistor soldered at R3; C3 is left open. The voltage control input is not used for XO devices.

### 1.3. Output Clock

Because the Si55x/Si53x devices can support an LVPECL buffer type (in addition to LVDS and CMOS), pulldown resistors (R1 and R2) are available for proper output biasing. For LVPECL buffers, biasing can be achieved through a variety of equivalent circuits; the Si5xx-EVB allows for 130 Ω pulldown resistors. After the output biasing, the high-speed outputs are dc-blocked for connection to differently biased inputs, such as standard test equipment or a phase detector EVB. Please review “1.4. Preparing the EVB” for non-LVPECL devices.

### 1.4. Preparing the EVB

By default, the evaluation board is set up to accept LVPECL configured devices. This configuration uses 130 Ω pull-down resistors to bias the LVPECL output stage. If an LVDS, CMOS, or CML based device is to be installed, the output biasing resistors, R1 and R2, should be removed.

2. Schematics

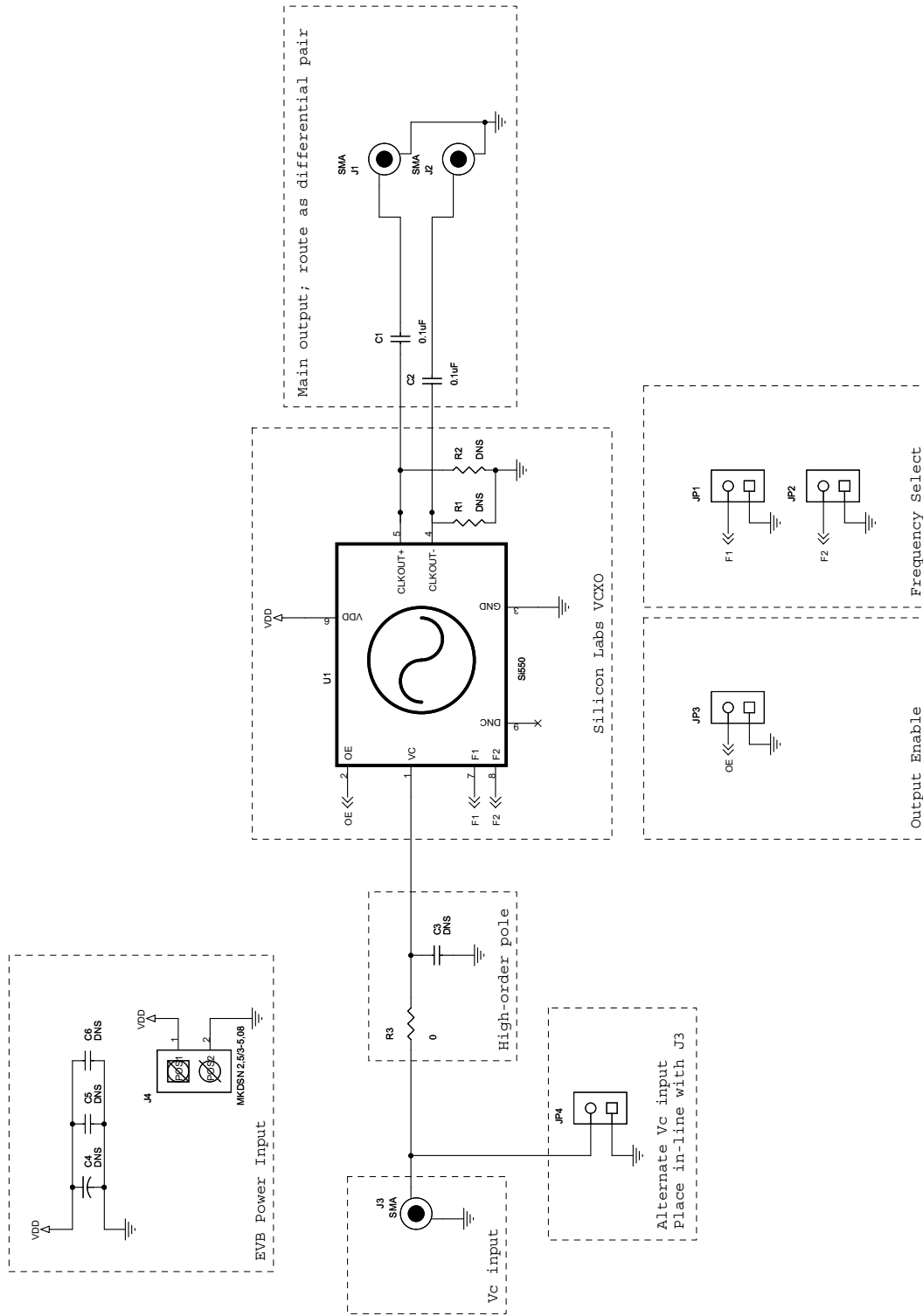


Figure 1. Si5xx-EVB Schematic

# Si5xx-EVB

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## 3. Bill of Materials

Item	Quantity	Reference	Description	Manufacturer's #	Manufacturer
1	2	C1,C2	CAP,SM,0.1UF,16V,20%,X7R,0402	C0402X7R160-104KNE	VENKEL
2	2	C5	CAP,SM,0.1UF,16V,20%,X7R,0603	C0603X7R160-104KNE	VENKEL
3	1	C4	CAP,SM,10UF,10V,10%,TANTALUM,3216	TA010TCM106KAR	VENKEL
4	1	C6	CAP,SM,100PF,50V,10%,C0G,0603	C0603C0G500-101KNE	VENKEL
5	4	JP1,JP2,JP3,JP4	CONN,HEADER,2X1	TSW-150-07-T-D or TSW-150-07-T-S	SAMTEC
6	3	J1,J2,J3	CONN,SMA SIDE MOUNT	901-10003	AMPHENOL
7	1	J4	CONN,POWER,2 POSITION	1729018	PHOENIX CONTACT
8	1	R3	RES,SM,0 OHM,0603	CR0603-16W-000T	VENKEL
9	2	R1,R2	RES,SM,150,1%,0603	CR0603-16W-1500FT	VENKEL
<b>No Load</b>					
11	1	C3	CAP,SM,0.1UF,16V,20%,X7R,0603	C0603X7R160-104KNE	VENKEL
10	1	U1	SI5XX	SI5XX	SILICON LABORATORIES

4. Layout

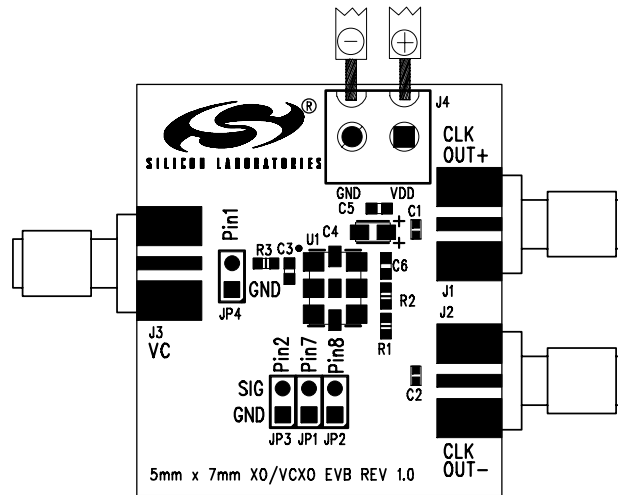


Figure 2. Assembly Drawing

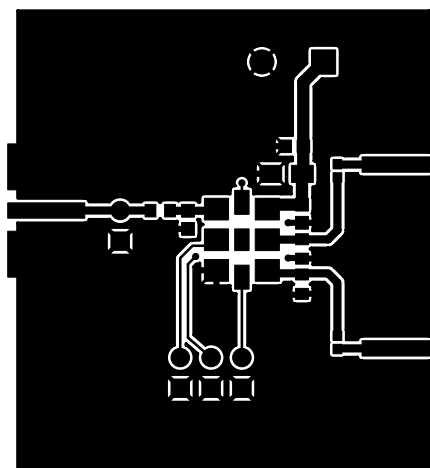


Figure 3. Layer 1 Primary

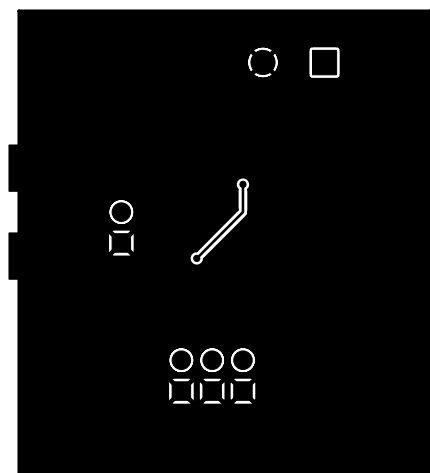


Figure 4. Layer 2 Secondary

# Si5xx-EVB

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## DOCUMENT CHANGE LIST

### Revision 0.13 to Revision 0.14

- Updated "Bill of Materials," on page 4.
- Updated Figure 2, "Assembly Drawing," on page 5.

**NOTES:**

# Si5xx-EVB

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## CONTACT INFORMATION

### Silicon Laboratories Inc.

4635 Boston Lane  
Austin, TX 78735  
Tel: 1+(512) 416-8500  
Fax: 1+(512) 416-9669  
Toll Free: 1+(877) 444-3032  
Email: VCXOinfo@silabs.com  
Internet: www.silabs.com

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