



RF Power Field Effect Transistors

N-Channel Enhancement-Mode Lateral MOSFETs

Designed for W-CDMA and LTE base station applications with frequencies from 2110 to 2170 MHz. Can be used in Class AB and Class C for all typical cellular base station modulation formats.

- Typical Doherty Single-Carrier W-CDMA Performance: $V_{DD} = 28$ Volts, $I_{DQB} = 360$ mA, $V_{GSA} = 0.4$ Vdc, $P_{out} = 28$ Watts Avg., IQ Magnitude Clipping, Channel Bandwidth = 3.84 MHz, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)
2110 MHz	14.2	46.4	7.9	-35.4
2140 MHz	14.1	45.7	7.7	-35.3
2170 MHz	14.0	45.1	7.6	-34.8

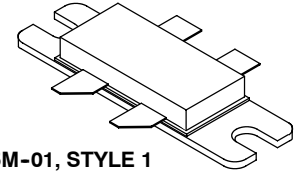
- Capable of Handling 10:1 VSWR, @ 32 Vdc, 2140 MHz, 157 Watts CW ⁽¹⁾ Output Power (3 dB Input Overdrive from Rated P_{out})
- Typical P_{out} @ 3 dB Compression Point ≈ 166 Watts CW ⁽¹⁾

Features

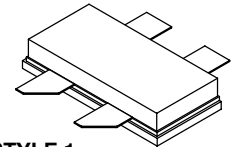
- Advanced High Performance In-Package Doherty
- Production Tested in a Doherty Configuration
- 100% PAR Tested for Guaranteed Output Power Capability
- Characterized with Large-Signal Load-Pull Parameters and Common Source S-Parameters
- Internally Matched for Ease of Use
- Integrated ESD Protection
- Greater Negative Gate-Source Voltage Range for Improved Class C Operation
- Designed for Digital Predistortion Error Correction Systems
- RoHS Compliant
- NI-780-4 in Tape and Reel. R3 Suffix = 250 Units, 56 mm Tape Width, 13 inch Reel. For R5 Tape and Reel option, see p. 8.
- NI-780S-4 in Tape and Reel. R3 Suffix = 250 Units, 32 mm Tape Width, 13 inch Reel. For R5 Tape and Reel option, see p. 8.

MRF8HP21130HR3
MRF8HP21130HSR3

2110-2170 MHz, 28 W AVG., 28 V
W-CDMA, LTE
LATERAL N-CHANNEL
RF POWER MOSFETs



CASE 465M-01, STYLE 1
NI-780-4
MRF8HP21130HR3



CASE 465H-02, STYLE 1
NI-780S-4
MRF8HP21130HSR3

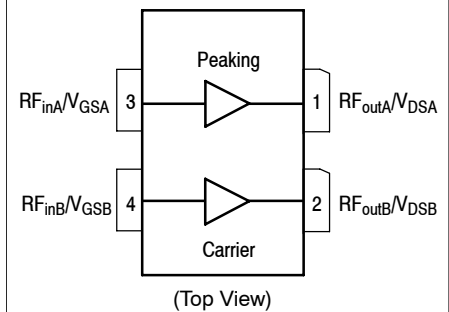


Figure 1. Pin Connections

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	-6.0, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_C	150	°C
Operating Junction Temperature ^(2,3)	T_J	225	°C
CW Operation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	CW	118 0.28	W W/°C

1. Exceeds recommended operating conditions. See CW operation data in Maximum Ratings table.
2. Continuous use at maximum temperature will affect MTTF.
3. MTTF calculator available at <http://www.freescale.com/rf>. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (1,2)	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$		°C/W
Case Temperature 81°C, 28 W CW, 28 Vdc, $I_{DQB} = 360$ mA, $V_{GSA} = 0.4$ Vdc, 2170 MHz		0.60	
Case Temperature 105°C, 110 W CW ⁽³⁾ , 28 Vdc, $I_{DQB} = 360$ mA, $V_{GSA} = 0.4$ Vdc, 2170 MHz		0.50	

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	1C (Minimum)
Machine Model (per EIA/JESD22-A115)	B (Minimum)
Charge Device Model (per JESD22-C101)	IV (Minimum)

Table 4. Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

Off Characteristics ⁽⁴⁾

Zero Gate Voltage Drain Leakage Current ($V_{DS} = 65$ Vdc, $V_{GS} = 0$ Vdc)	I_{DSS}	—	—	10	μA_{dc}
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 28$ Vdc, $V_{GS} = 0$ Vdc)	I_{DSS}	—	—	1	μA_{dc}
Gate-Source Leakage Current ($V_{GS} = 5$ Vdc, $V_{DS} = 0$ Vdc)	I_{GSS}	—	—	1	μA_{dc}

On Characteristics - Side A ⁽⁴⁾

Gate Threshold Voltage ($V_{DS} = 10$ Vdc, $I_D = 102$ μA_{dc})	$V_{GS(th)}$	0.1	0.9	1.6	Vdc
Drain-Source On-Voltage ($V_{GS} = 10$ Vdc, $I_D = 1.02$ Adc)	$V_{DS(on)}$	0.1	0.2	0.3	Vdc

On Characteristics - Side B ⁽⁴⁾

Gate Threshold Voltage ($V_{DS} = 10$ Vdc, $I_D = 75$ μA_{dc})	$V_{GS(th)}$	1.2	1.8	2.7	Vdc
Gate Quiescent Voltage ($V_{DD} = 28$ Vdc, $I_{DB} = 360$ mA, Measured in Functional Test)	$V_{GS(Q)}$	1.9	2.6	3.4	Vdc
Drain-Source On-Voltage ($V_{GS} = 10$ Vdc, $I_D = 0.75$ Adc)	$V_{DS(on)}$	0.1	0.2	0.3	Vdc

Functional Tests ^(5,6) (In Freescale Doherty Test Fixture, 50 ohm system) $V_{DD} = 28$ Vdc, $I_{DQB} = 360$ mA, $V_{GSA} = 0.4$ Vdc, $P_{out} = 28$ W Avg., $f = 2170$ MHz, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ± 5 MHz Offset.

Power Gain	G_{ps}	13.0	14.0	16.0	dB
Drain Efficiency	η_D	42.0	45.1	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	6.7	7.6	—	dB
Adjacent Channel Power Ratio	ACPR	—	-34.8	-30.0	dBc

Typical Broadband Performance ⁽⁶⁾ (In Freescale Doherty Test Fixture, 50 ohm system) $V_{DD} = 28$ Vdc, $I_{DQB} = 360$ mA, $V_{GSA} = 0.4$ Vdc, $P_{out} = 28$ W Avg., Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ± 5 MHz Offset.

Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)
2110 MHz	14.2	46.4	7.9	-35.4
2140 MHz	14.1	45.7	7.7	-35.3
2170 MHz	14.0	45.1	7.6	-34.8

1. MTTF calculator available at <http://www.freescale.com/rf>. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
2. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to <http://www.freescale.com/rf>. Select Documentation/Application Notes - AN1955.
3. Exceeds recommended operating conditions. See CW operation data in Maximum Ratings table.
4. Each side of device measured separately.
5. Part internally matched both on input and output.
6. Measurement made with device in a Doherty configuration.

(continued)

Table 4. Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted) (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
Typical Performances ⁽¹⁾ (In Freescale Doherty Test Fixture, 50 ohm system) $V_{DD} = 28\text{ Vdc}$, $I_{DQB} = 360\text{ mA}$, $V_{GSA} = 0.4\text{ Vdc}$, 2110–2170 MHz Bandwidth					
P_{out} @ 1 dB Compression Point, CW	P1dB	—	130 ⁽²⁾	—	W
P_{out} @ 3 dB Compression Point, CW	P3dB	—	166 ⁽²⁾	—	W
IMD Symmetry @ 52 W PEP, P_{out} where IMD Third Order Intermodulation $\cong 30\text{ dBc}$ (Delta IMD Third Order Intermodulation between Upper and Lower Sidebands $> 2\text{ dB}$)	IMD _{sym}	—	18	—	MHz
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW _{res}	—	50	—	MHz
Gain Flatness in 60 MHz Bandwidth @ $P_{out} = 28\text{ W Avg.}$	G_F	—	0.2	—	dB
Gain Variation over Temperature (-30°C to $+85^\circ\text{C}$)	ΔG	—	0.011	—	dB/ $^\circ\text{C}$
Output Power Variation over Temperature (-30°C to $+85^\circ\text{C}$) ⁽²⁾	ΔP_{1dB}	—	0.012	—	dB/ $^\circ\text{C}$

1. Measurement made with device in a Doherty configuration.

2. Exceeds recommended operating conditions. See CW operation data in Maximum Ratings table.

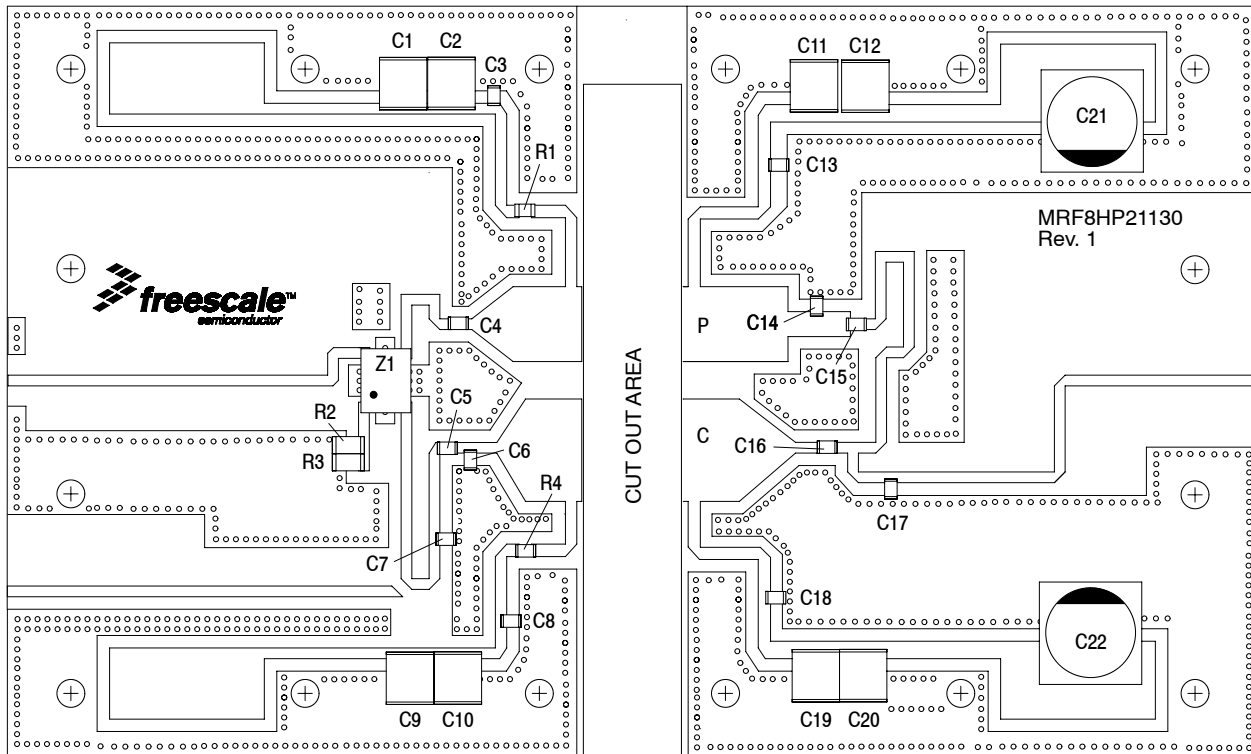


Figure 2. MRF8HP21130HR3(HSR3) Test Circuit Component Layout

Table 5. MRF8HP21130HR3(HSR3) Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C2, C9, C10, C11, C12, C19, C20	10 μ F Chip Capacitors	GRM55DR61H106KA88L	Murata
C3, C4, C5, C8, C13, C15, C16, C18	15 pF Chip Capacitors	ATC600F150JT250XT	ATC
C6	1.2 pF Chip Capacitor	ATC600F1R2BT250XT	ATC
C7	0.5 pF Chip Capacitor	ATC600F0R5BT250XT	ATC
C14	0.7 pF Chip Capacitor	ATC600F0R7BT250XT	ATC
C17	1 pF Chip Capacitor	ATC600F1R0BT250XT	ATC
C21, C22	220 μ F, 50 V Electrolytic Capacitors	EMVY500ADA221MJA0G	United Chemi-Con
R2, R3	100 Ω , 1/4 W Chip Resistors	CRCW1206100RFKEA	Vishay
R1, R4	10 Ω , 1/4 W Chip Resistors	CRCW120610R0JNEA	Vishay
Z1	2000–2300 MHz Band 90°, 3 dB Hybrid Coupler	X3C21P1-03S	Anaren
PCB	0.020", $\epsilon_r = 3.5$	R04350	Rogers

TYPICAL CHARACTERISTICS

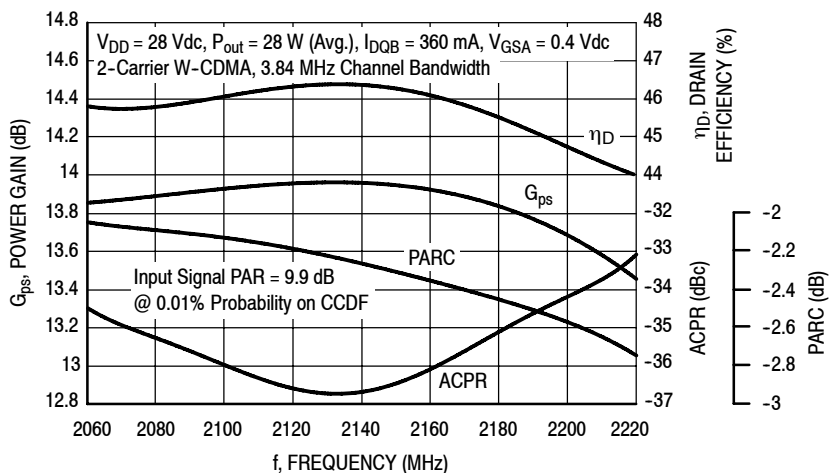


Figure 3. Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ $P_{out} = 28$ Watts Avg.

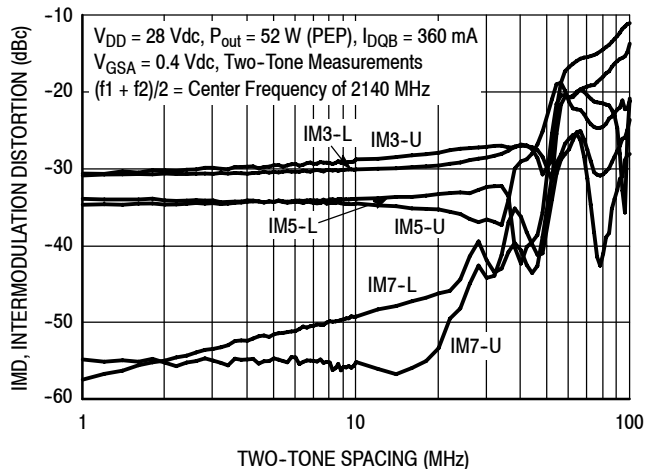


Figure 4. Intermodulation Distortion Products versus Two-Tone Spacing

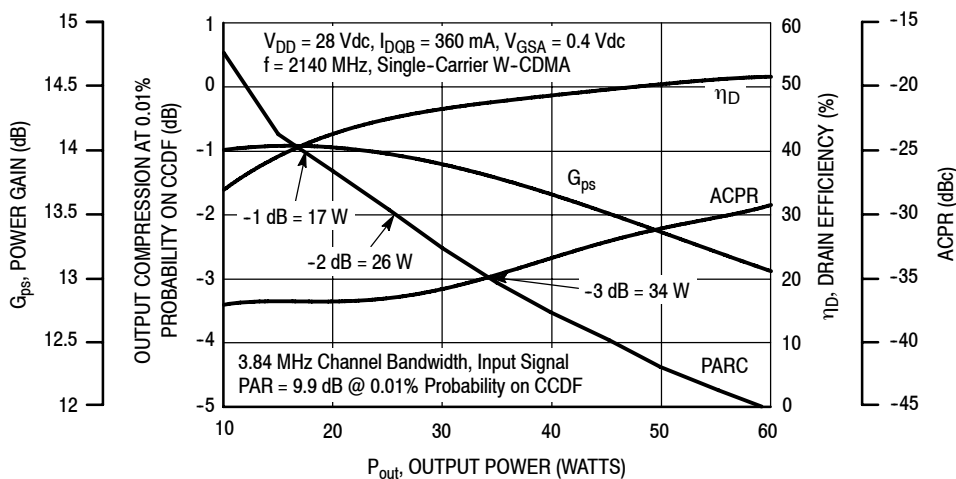


Figure 5. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

TYPICAL CHARACTERISTICS

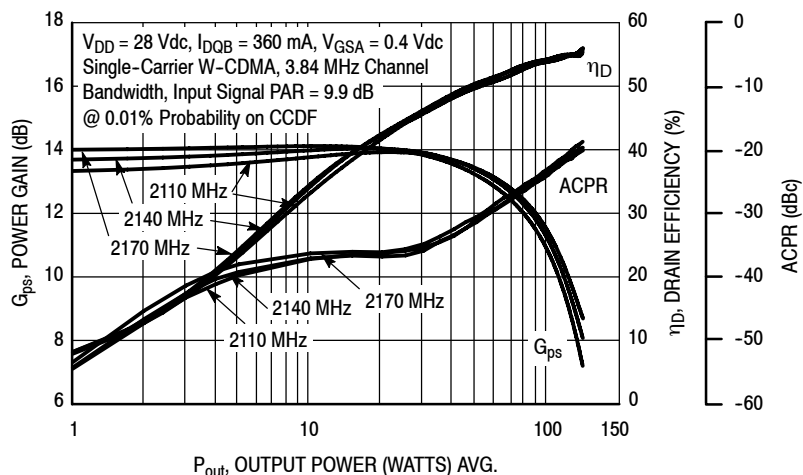


Figure 6. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

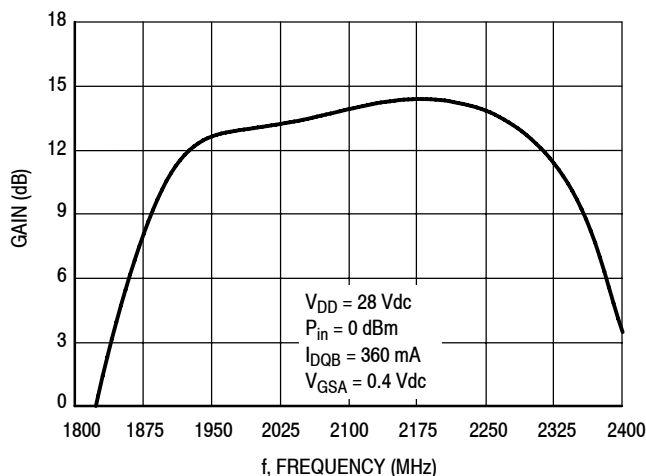


Figure 7. Broadband Frequency Response

W-CDMA TEST SIGNAL

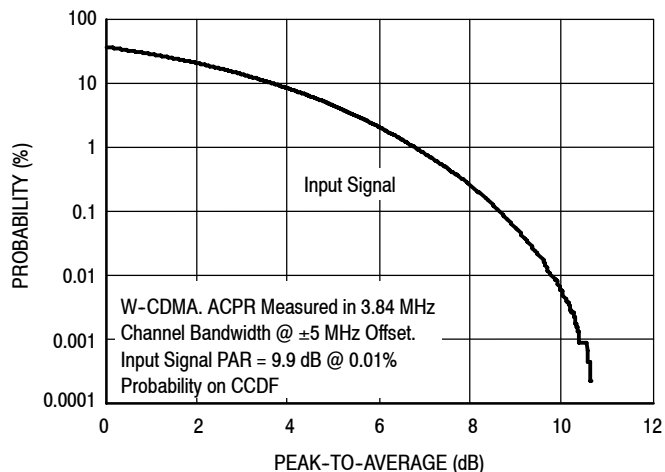


Figure 8. CCDF W-CDMA IQ Magnitude Clipping, Single-Carrier Test Signal

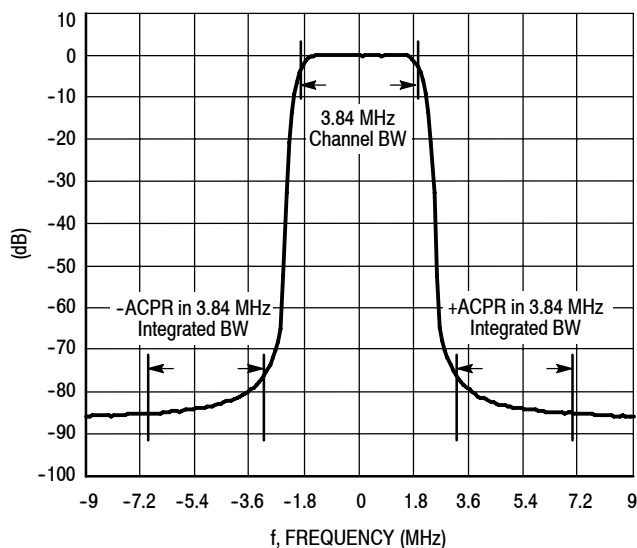


Figure 9. Single-Carrier W-CDMA Spectrum

$V_{DD} = 28 \text{ Vdc}$, $I_{DQB} = 360 \text{ mA}$, Pulsed CW, 10 $\mu\text{sec}(\text{on})$, 10% Duty Cycle

f (MHz)	$Z_{\text{source}} (\Omega)$	$Z_{\text{load}}^{(1)} (\Omega)$	Max Output Power					
			P1dB			P3dB		
			(dBm)	(W)	η_D (%)	(dBm)	(W)	η_D (%)
2110	6.20 - j10.7	3.40 - j6.70	48.4	69	55.3	49.2	83	56.1
2140	7.80 - j11.5	3.40 - j6.80	48.4	69	55.5	49.2	83	55.3
2170	9.20 - j12.2	3.00 - j7.24	48.4	69	52.5	49.2	83	53.3

(1) Load impedance for optimum P1dB power.

Z_{source} = Impedance as measured from gate contact to ground.

Z_{load} = Impedance as measured from drain contact to ground.

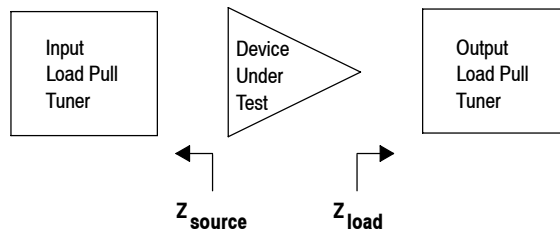


Figure 10. Carrier Side Load Pull Performance — Maximum P1dB Tuning

$V_{DD} = 28 \text{ Vdc}$, $I_{DQB} = 360 \text{ mA}$, Pulsed CW, 10 $\mu\text{sec}(\text{on})$, 10% Duty Cycle

f (MHz)	$Z_{\text{source}} (\Omega)$	$Z_{\text{load}}^{(1)} (\Omega)$	Max Drain Efficiency					
			P1dB			P3dB		
			(dBm)	(W)	η_D (%)	(dBm)	(W)	η_D (%)
2110	6.20 - j10.7	7.60 - j6.30	46.8	48	63.5	48.0	63	64.1
2140	7.80 - j11.5	7.71 - j5.50	46.6	46	63.5	47.8	60	63.9
2170	9.20 - j12.2	6.40 - j5.60	47.0	50	62.3	47.8	60	62.5

(1) Load impedance for optimum P1dB efficiency.

Z_{source} = Impedance as measured from gate contact to ground.

Z_{load} = Impedance as measured from drain contact to ground.

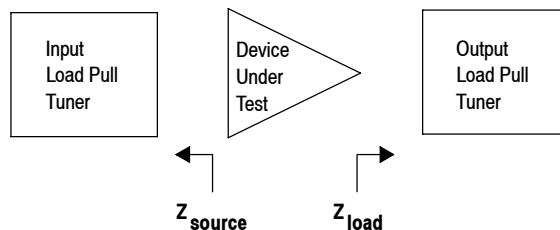


Figure 11. Carrier Side Load Pull Performance — Maximum Efficiency Tuning

$V_{DD} = 28 \text{ Vdc}$, $V_{GSA} = 0.4 \text{ Vdc}$, Pulsed CW, 10 $\mu\text{sec}(\text{on})$, 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	$Z_{\text{load}}^{(1)}$ (Ω)	Max Output Power					
			P1dB			P3dB		
			(dBm)	(W)	η_D (%)	(dBm)	(W)	η_D (%)
2110	3.10 - j7.30	5.40 + j0.50	51.4	138	55.8	52.2	166	56.9
2140	3.77 - j7.80	5.00 + j1.80	51.2	132	54.4	52.0	158	56.7
2170	4.30 - j8.50	4.30 + j1.50	51.2	132	54.1	52.0	158	55.2

(1) Load impedance for optimum P1dB power.

Z_{source} = Impedance as measured from gate contact to ground.

Z_{load} = Impedance as measured from drain contact to ground.

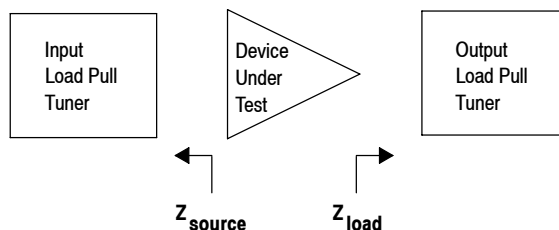


Figure 12. Peaking Side Load Pull Performance — Maximum P1dB Tuning

$V_{DD} = 28 \text{ Vdc}$, $V_{GSA} = 0.4 \text{ Vdc}$, Pulsed CW, 10 $\mu\text{sec}(\text{on})$, 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	$Z_{\text{load}}^{(1)}$ (Ω)	Max Drain Efficiency					
			P1dB			P3dB		
			(dBm)	(W)	η_D (%)	(dBm)	(W)	η_D (%)
2110	3.10 - j7.30	4.80 - j5.20	49.1	81	67.2	51.0	126	68.2
2140	3.77 - j7.80	6.50 - j4.80	49.0	79	66.6	49.9	98	67.5
2170	4.30 - j8.50	6.90 - j4.90	48.8	76	66.7	49.9	98	67.4

(1) Load impedance for optimum P1dB efficiency.

Z_{source} = Impedance as measured from gate contact to ground.

Z_{load} = Impedance as measured from drain contact to ground.

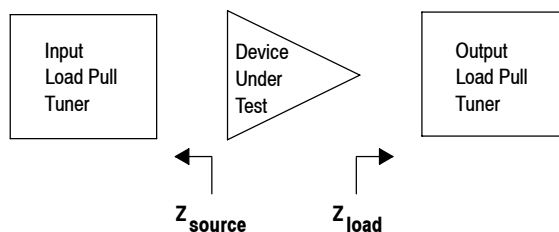
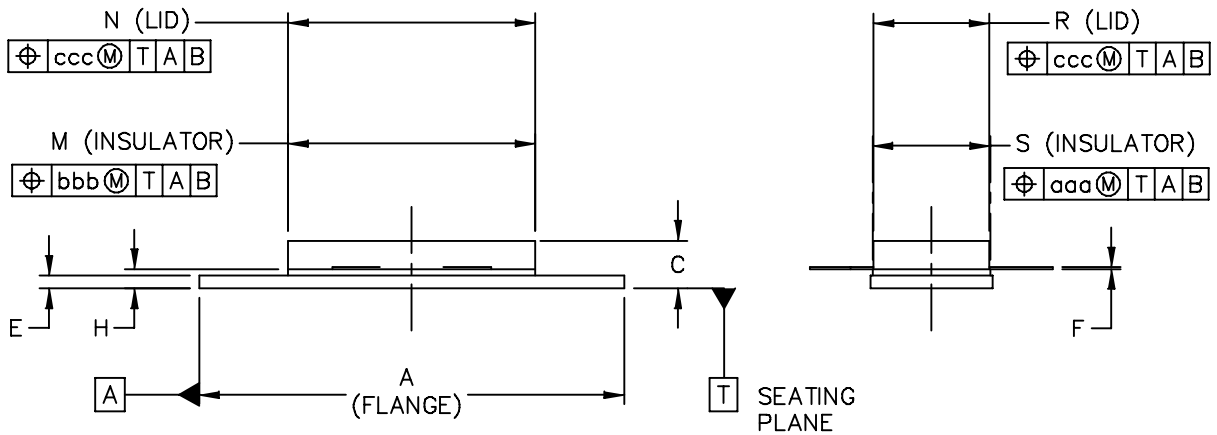
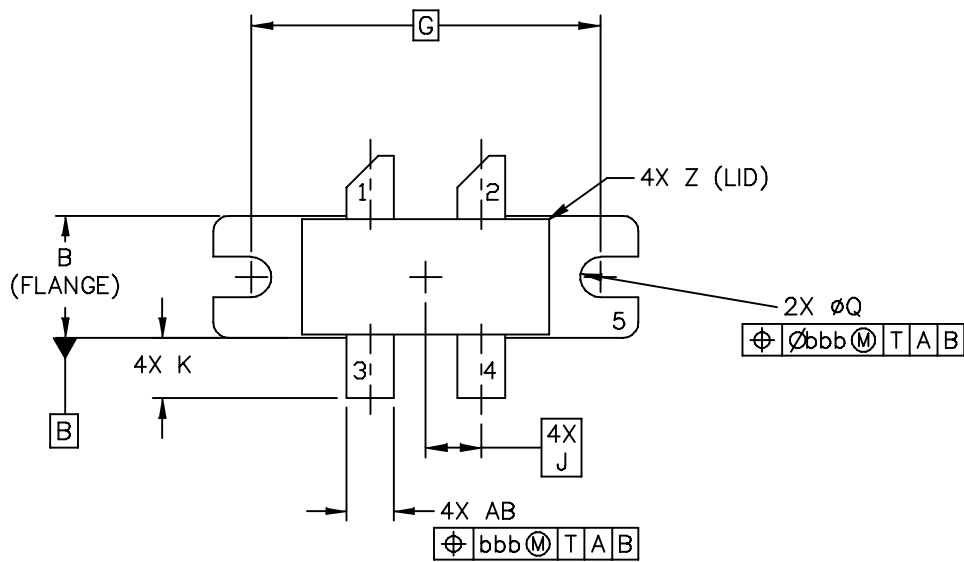


Figure 13. Peaking Side Load Pull Performance — Maximum Efficiency Tuning

PACKAGE DIMENSIONS



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: NI 780-4	DOCUMENT NO: 98ASA10793D CASE NUMBER: 465M-01 STANDARD: NON-JEDEC	REV: 0 27 MAR 2007	

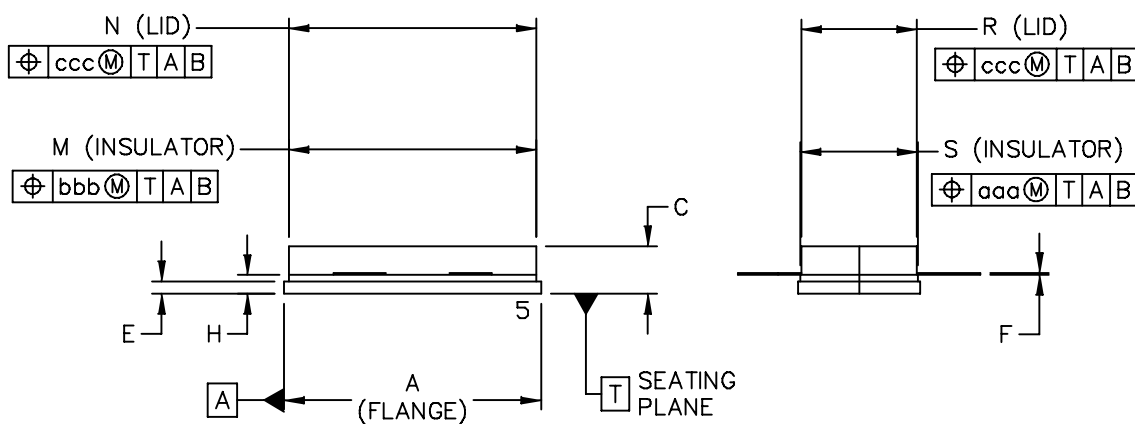
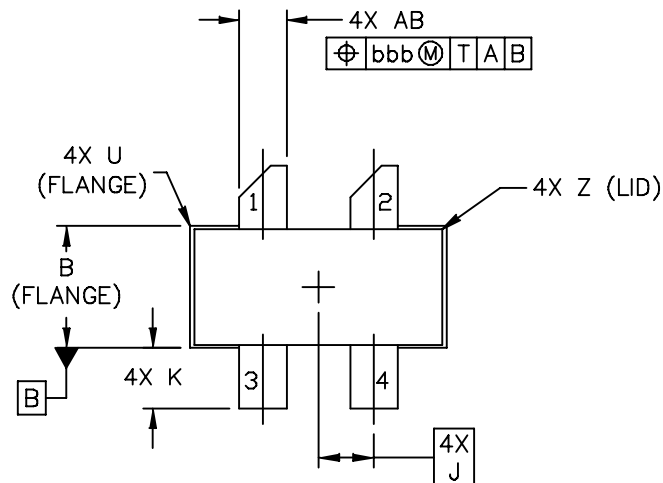
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION H IS MEASURED .030 (0.762) AWAY FROM PACKAGE BODY.

STYLE 1:

- PIN 1. DRAIN
 2. DRAIN
 3. GATE
 4. GATE
 5. SOURCE

DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	1.335	1.345	33.91	34.16	R	.365	.375	9.27	9.53
B	.380	.390	9.65	9.91	S	.365	.375	9.27	9.52
C	.125	.170	3.18	4.32	U		.040		1.02
E	.035	.045	0.89	1.14	Z		.030		0.76
F	.003	.006	0.08	0.15	AB	.145	.155	3.68	3.94
G	1.100 BSC		27.94 BSC						
H	.057	.067	1.45	1.7	aaa		.005		0.127
J	.175 BSC		4.44 BSC		bbb		.010		0.254
K	.170	.210	4.32	5.33	ccc		.015		0.381
M	.774	.786	19.61	20.02					
N	.772	.788	19.61	20.02					
Q	ø.118	ø.138	ø3	ø3.51					
© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.			MECHANICAL OUTLINE			PRINT VERSION NOT TO SCALE			
TITLE: NI 780-4					DOCUMENT NO: 98ASA10793D			REV: 0	
					CASE NUMBER: 465M-01			27 MAR 2007	
					STANDARD: NON-JEDEC				



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: NI 780S-4	DOCUMENT NO: 98ASA10718D	REV: A	
	CASE NUMBER: 465H-02	27 MAR 2007	
	STANDARD: NON-JEDEC		

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH.
3. DELETED
4. DIMENSION H IS MEASURED .030 (0.762) AWAY FROM PACKAGE BODY.

STYLE 1:

- PIN 1. DRAIN
2. DRAIN
3. GATE
4. GATE
5. SOURCE

DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	.805	.815	20.45	20.7	U		.040		1.02
B	.380	.390	9.65	9.91	Z		.030		0.76
C	.125	.170	3.18	4.32	AB	.145	.155	3.68	- 3.94
E	.035	.045	0.89	1.14					
F	.003	.006	0.08	0.15	aaa		.005		0.127
H	.057	.067	1.45	1.7	bbb		.010		0.254
J	.175 BSC		4.44 BSC		ccc		.015		0.381
K	.170	.210	4.32	5.33					
M	.774	.786	19.61	20.02					
N	.772	.788	19.61	20.02					
R	.365	.375	9.27	9.53					
S	.365	.375	9.27	9.52					
© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.			MECHANICAL OUTLINE			PRINT VERSION NOT TO SCALE			
TITLE: NI 780S-4					DOCUMENT NO: 98ASA10718D			REV: A	
					CASE NUMBER: 465H-02			27 MAR 2007	
					STANDARD: NON-JEDEC				

PRODUCT DOCUMENTATION AND SOFTWARE

Refer to the following documents and software to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- .s2p File

For Software, do a Part Number search at <http://www.freescale.com>, and select the “Part Number” link. Go to the Software & Tools tab on the part’s Product Summary page to download the respective tool.

R5 TAPE AND REEL OPTION

R5 Suffix = 50 Units, 56 mm Tape Width, 13 inch Reel.

The R5 tape and reel option for MRF8HP21130H and MRF8HP21130HS parts will be available for 2 years after release of MRF8HP21130H and MRF8HP21130HS. Freescale Semiconductor, Inc. reserves the right to limit the quantities that will be delivered in the R5 tape and reel option. At the end of the 2 year period customers who have purchased these devices in the R5 tape and reel option will be offered MRF8HP21130H and MRF8HP21130HS in the R3 tape and reel option.

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Apr. 2011	• Initial Release of Data Sheet

How to Reach Us:

Home Page:

www.freescale.com

Web Support:

<http://www.freescale.com/support>

USA/Europe or Locations Not Listed:

Freescale Semiconductor, Inc.
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
1-800-521-6274 or +1-480-768-2130
www.freescale.com/support

Europe, Middle East, and Africa:

Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

Japan:

Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:

Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 10 5879 8000
support.asia@freescale.com

For Literature Requests Only:

Freescale Semiconductor Literature Distribution Center
1-800-441-2447 or +1-303-675-2140
Fax: +1-303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals", must be validated for each customer application by customer's technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.

Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners.

© Freescale Semiconductor, Inc. 2011. All rights reserved.

