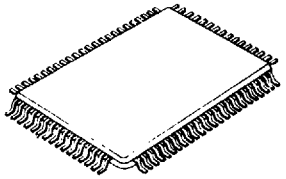
DSP+DAC (16BIT) FOR CDP

The KS9282B is a CMOS integrated circuit designed for the Digital Audio Signal processor of the CDP (Compact Disc Player) application. It is a Monolithic IC that builts-in 16-Bit Digital to Analog Converter to add to the conventional DSP function.

80-QFP-1420B



FEATURES

- **EFM Data Demodulation**
- **Built-in frame sync detection, protection and Injection circuit**
- **Correction of C1, C2 error**
- **Interpolation**
- **8fs oversampling Digital filter (51th+13th +9th)**
- **Subcode data serial output**
- **CLV Servo Controller**
- **Tracking Counter**
- **Micom interface**
- **Built-in 16K SRAM**
- **Digital Audio out**
- **Double speed available**
- **Built-in Digital PLL**
- **Built-in 16-Bit D/A converter**
- **Single power supply: V_{DD}=4.5~5.5V**

ORDERING INFORMATION

Device	Package	Operating Temperature
KS9282B	80-QFP-1420B	-20°C~+75°C

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BLOCK DIAGRAM

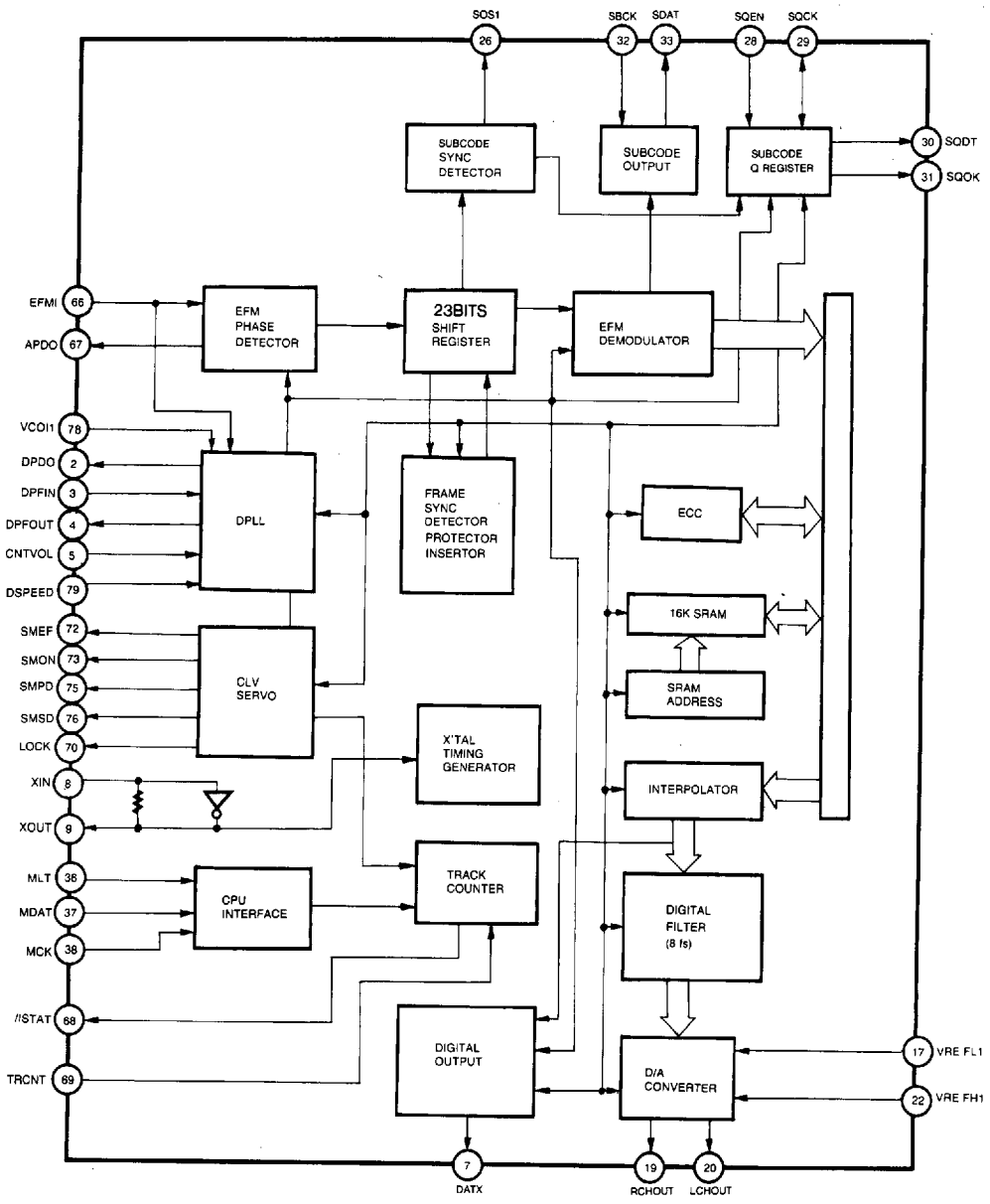
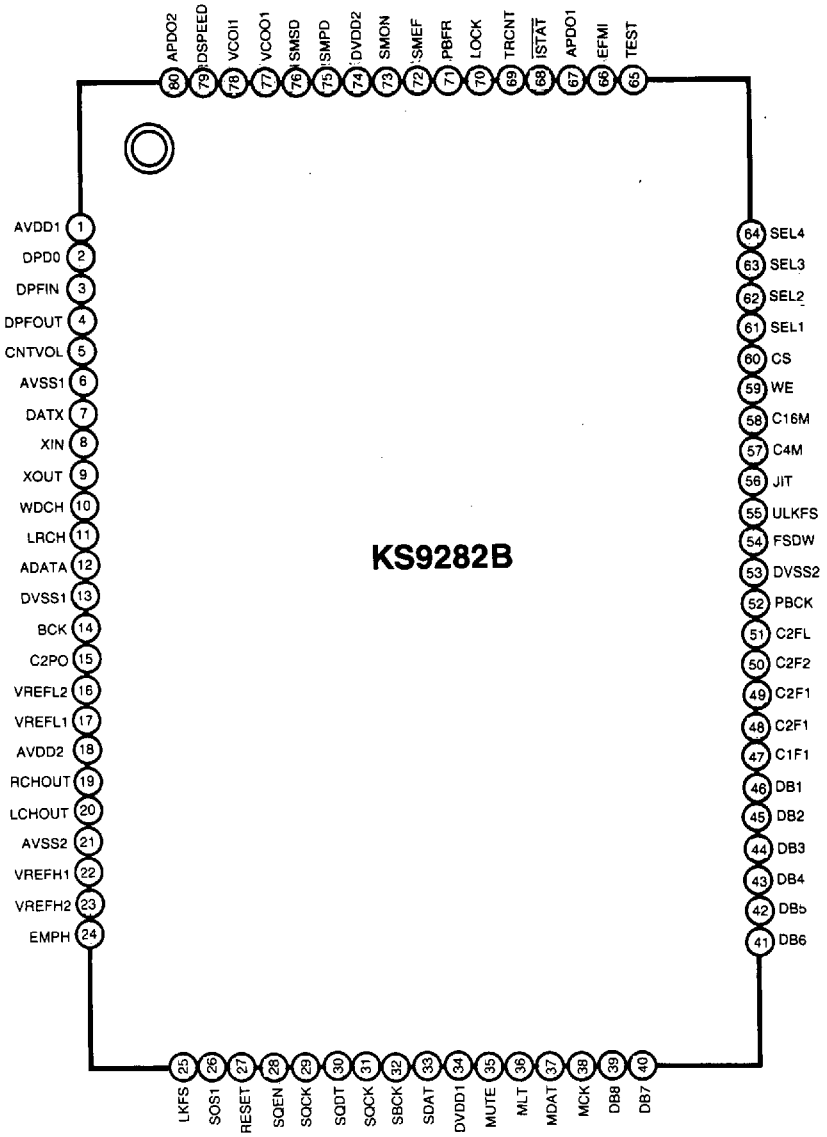


Fig. 1

PIN CONFIGURATION



■ PIN DESCRIPTION

Pin No.	Symbol	I/O	Description
1	AVDD1		Analog Vcc1
2	DPDO	O	Charge pump output for master PLL
3	DPFIN	I	Filter input for master PLL
4	DPFOUT	O	Filter output for master PLL
5	CNTVOL	I	VCO control voltage for master PLL
6	AVSS1		Analog Ground 1
7	DATX	O	Digital audio output
8	XIN	I	X-tal oscillator input
9	XOUT	O	X-tal oscillator output
10	WDCH	O	Word clock of 48 bit/SLOT (Normal speed = 88.2 KHz, Double speed = 176.4KHz)
11	LRCH	O	Channel clock of 48 bit/SLOT (Normal speed = 44.1KHz, Double speed = 88.2KHz)
12	ADATA	O	Serial audio data output of 48 bit/SLOT (MSB first)
13	DVSS1		Digital Ground 1
14	BCK	O	Audio data Bit clock for 48 bit/SLOT (Normal speed = 2.1168KHz, Double speed = 4.2336KHz)
15	C2PO	O	C2 pointer for output audio data
16	VREFL2	I	Input terminal 2 of reference voltage "L" (Floating)
17	VREFL1	I	Input terminal 1 of reference voltage "L" (GND Connection)
18	AVDD2		Analog VCC2
19	RCHOUT	O	Right-Channel audio output through D/A Converter
20	LCHOUT	O	Left-channel audio output through D/A converter
21	AVSS2		Analog Ground 2
22	VREFH1	I	Input terminal 1 of reference voltage "H" (V_{DD} connection)
23	VREFH2	I	Input terminal 2 of reference voltage "H" (Floating)

■ PIN DESCRIPTION (CONTINUED)

Pin No.	Symbol	I/O	Description
24	EMPH	O	Emphasis/Non-Emphasis Output ("H": Emphasis)
25	LKFS	O	The Lock Status output of frame sync
26	SOS1	O	Output of subcode sync signal (S0 + S1)
27	RESET	I	System reset at "L"
28	SQEN	I	SQCK I/O Control ("L": internal CK, "H": external CK)
29	SQCK	I/O	Clock for output Subcode-Q data
30	SQDT	O	Serial output of Subcode-Q data
31	SQOK	O	The CRC check result signal output of subcode-Q
32	SBCK	I	CLOCK for output subcode-Q data
33	SDAT	O	Subcode serial data output
34	$DV_{DD}1$		Digital Vcc1
35	MUTE	I	Mute control Input ("H": Mute ON)
36	MLT	I	Latch Signal Input from Micom
37	MDAT	I	Serial data Input from Micom
38	MCK	I	Serial Clock input from Micom
39	DB8	I/O	SRAM data I/O Port 8 (MSB)
40	DB7	I/O	SRAM data I/O Port 7
41	DB6	I/O	SRAM data I/O Port 6
42	DB5	I/O	SRAM data I/O Port 5
43	DB4	I/O	SRAM data I/O Port 4
44	DB3	I/O	SRAM data I/O Port 3
45	DB2	I/O	SRAM data I/O Port 2
46	DB1	I/O	SRAM data I/O Port 1 (LSB)

■ PIN DESCRIPTION (CONTINUED)

Pin No.	Symbol	I/O	Description
47	C1F1	I/O	Monitoring output for C1 error correction (RA1)
48	C1F2	I/O	Monitoring output for C1 error correction (RA2)
49	C2F1	I/O	Monitoring output for C2 error correction (RA3)
50	C2F2	I/O	Monitoring output ofr C2 error correction (RA4)
51	C2FL	I/O	C2 decoder flag (High: When the processing C2 code is impossible correction state) (RA5)
52	/PBCK	I/O	Output of VCO/2 (Normal speed = 4.3218MHz, Double speed = 8.6436MHz) (RA6)
53	DV_{SS2}		Digital Ground 2
54	FSDW	I/O	Unprotected frame sync (RA7)
55	ULKFS	I/O	Frame sync protection state (RA8)
56	/JIT	I/O	Display of either RAM overflow or underflow for ±4 frame Jitter margin(RA9)
57	C4M	I/O	Only monitoring signal (Normal playback: 4.2336MHz) (RA10)
58	C16M	I/O	16.9344MHz signal output (RA11)
59	/WE	I/O	Terminal for test
60	/CS	I/O	Terminal for test
61	SEL1	I	Mode Selection Terminal 1 (H: 33.8688MHz, L: 16.9344MHz)
62	SEL2	I	Mode Selection Terminal 2 (H: APLL L: DPLL)
63	SEL3	I	Mode Selection Terminal 3 (H: CDROM L: CDP)
64	SEL4	I	Mode Selection Terminal 4 (L: Internal SRAM)
65	TEST	I	Test Terminal (L = Normal operating state)
66	EFMI	I	EFM Signal input
67	APDO	O	Charge Pump output for analog PLL
68	/ISTAT	O	The internal status output
69	TRCNT	I	Tracking counter input signal

■ PIN DESCRIPTION (CONTINUED)

Pin No.	Symbol	I/O	Description
70	LOCK	O	Output signal of LKFS Condition sampled PBFR/16 (If LKFS is "H", Lock is "H". If the LKFS is sampled "L" at least 8 times by PBFR/16, Lock is "L")
71	PBFR	O	Write frame clock (Lock: 7.35KHz)
72	SMEF	O	LPF time constant control of the spindle servo error signal
73	SMON	O	ON/OFF control signal for spindle servo
74	DV_{DD2}		Digital V_{CC} 2
75	SMPD	O	Spindle Motor drive (Rough control in the CLV-S mode Phase control in the CLV-P mode)
76	SMSD	O	Spindle Motor drive (Velocity control in the CLV-P mode)
77	VCO_{O1}	O	Vco output signal (When the state is lock by means of PBFR,it is 8.643MHz)
78	VCO_{I1}	I	VCO input signal
79	DSPEED	I	Double speed mode control (H: Normal Speed, L: Double Speed)
80	APD02	O	Analog PLL Charge Pump output for Double Speed mode

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■ ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{DD}	−0.3 ~ 7.0	V
Input Voltage	V_I	−0.3 ~ 7.0	V
Output Voltage	V_O	−0.3 ~ 7.0	V
Operating Temperature	T_{OPR}	−20 ~ 75	°C
Storage Temperature	T_{STG}	−40 ~ 125	°C

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

(V_{DD} = 5V, Vss = 0V, Ta = 25°C, unless Otherwise Specified)

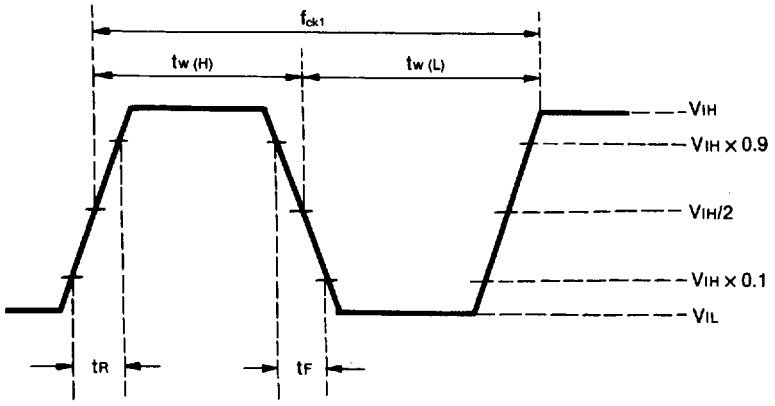
Characteristic	Symbol	Test Conditions	MIN	TYP	MAX	Unit
'H' INPUT VOLTAGE1	VIH (1)	(Note 1)	0.7VDD	—	—	V
'L' INPUT VOLTAGE1	VIL (1)	(Note 1)	—	—	0.3VDD	V
'H' INPUT VOLTAGE2	VIH (2)	(Note 2)	0.8VDD	—	—	V
'L' INPUT VOLTAGE2	VIL (2)	(Note 2)	—	—	0.2VDD	V
'H' OUTPUT VOLTAGE1	VOH (1)	IOH = −1mA (Note 3)	V_{DD}−0.5	—	VDD	V
'L' OUTPUT VOLTAGE1	VOL (1)	IOL = 1mA (Note 3)	0	—	0.4	V
'H' OUTPUT VOLTAGE2	VOH (2)	IOH = −1mA (Note 4)	V_{DD}−0.5	—	VDD	V
'L' OUTPUT VOLTAGE2	VOL (2)	IOL = 2mA (Note 4)	0	—	0.4	V
INPUT LEAK CURRENT	ILKG	VI = 0 ~ VDD (Note 5)	−5	—	5	uA
THREE STATE OUTPUT LEAK CURRENT	Io(LKG)	VO = 0 ~ VDD (Note 5)	−5	—	5	uA

(Note 1) Related pins: All input pins except for pins of Notes
(Note 2) Related pins: DB8 ~ DB1, TRCNT, MCK
(Note 3) Related pins: All output pins except for pins of Note4
(Note 4) Related pins: /ISTAT
(Note 5) Related pins: SMEF, SMPD, SMSD, APDO1, APDO2, DPDO

2. AC Characteristics

A. XIN, VCOI (When the pulse inputs to)
(V_{DD} = 5V, V_{SS} = 0V, T_a = 25°C, Unless otherwise Specified)

Characteristic	SYMBOL	MIN	TYP	MAX	UNIT
'H' LEVEL PULSE WIDTH	$t_{w(H)}$	13	—	—	ns
'L' LEVEL PULSE WIDTH	$t_{w(L)}$	13	—	—	ns
PULSE FREQUENCY	t_{CK}	26	—	—	ns
INPUT 'H' LEVEL	V_{IH}	VDD-1.0	—	—	V
INPUT 'L' LEVEL	V_{IL}	—	—	0.8	V
RISING & FALLING TIME	t_R, t_F	—	—	8	ns



B. MCK, MDAT, MLT, TRCNT
(V_{DD} = 5V, V_{SS} = 0V, T_a = 25°C, unless otherwise specified)

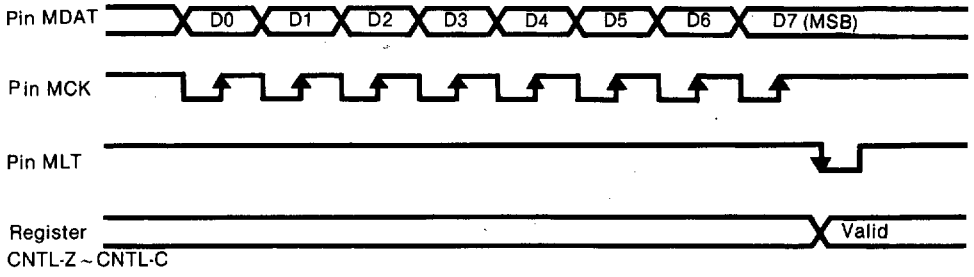
Characteristic	SYMBOL	MIN	TYP	MAX	UNIT
CLOCK FREQUENCY	f_{ck1}	—	—	1	MHz
CLOCK PULSE WIDTH	t_w	300	—	—	ns
SETUP TIME	t_{SU}	300	—	—	ns
HOLD TIME	t_H	300	—	—	ns
DELAY TIME	t_D	300	—	—	ns
LATCH PULSE WIDTH	$t_{w(LATCH)}$	300	—	—	ns
TRCNT SQCK FREQUENCY	$f_{ck2(SQCK)}$	—	—	1	MHz
TRCNT SQCK PULSE WIDTH	$t_{w(SQCK)}$	300	—	—	ns

■ APPLICATION INFORMATION

FUNCTION DESCRIPTION

1. Micom interface
The data inputed from Micom is inputed to MDAT and transfered by MCK.
The inputed signal is loaded to control register by means of MLT.

This timing chart is as follows.



(Fig 1. Micom data input timing chart)

CONTROL REGISTER	COMMENT	ADDRESS D7 ~ D4	DATA				/ISTAT PIN
			D3	D2	D1	D0	
CNTL-Z	DATA CONTROL	1001	ZCMT	HIPD	NCLV	CRCD	HI-Z
CNTL-S	FRAME SYNC PROTECTION ATTENUATION CONTROL	1010	FSEM	FSEL	WSEL	ATTM	HI-Z
CNTL-L	TRACKING COUNTER LOWER 4 BITS	1011	TRC3	TRC2	TRC1	TRC0	/COMPLETE
CNTL-U	TRACKING COUNTER UPPER 4 BITS	1100	TRC7	TRC6	TRC5	TRC4	/COUNT
CNTL-W	CLV CONTROL	1101	COM	WB	WP	GAIN	HI-Z
CNTL-C	CLV MODE	1110	CLV MODE				/(Pw≥64)
CNTL-D	DOUBLE SPEED	1111	—	—	DS1	DS0	HI-Z

(Table 1. Control register and data)

1) CNTL-Z REGISTER
It is a register to control zero cross mute of audio data, phase terminal control, phase servo and having or not of CRCF data in SQDT.

	DATA	DATA = 0	DATA = 1
ZCMT	D3	Zero cross mute is OFF	Zero cross mute is ON
HIPD	D2	It Operates phase normally	The phase becomes "L" to "Hi-Z"
NCLV	D1	Phase Servo is acted by frame sync	Phase servo is controlled by base counter
CRCQ	D0	SQDT outputs except for SQOK	SQDT = CRCF when SOS1 = "H"

(Tabe 2)

2) CNTL-S REGISTER
It is a register to control frame sync protection and attenuation.

FSEM	FSEL	FRAME
0	0	2
0	1	4
1	0	8
1	1	13

WSEL	CLOCK
0	±3
1	±7

ATTM	MUTE	dB
0	0	0
0	1	$-\infty$
1	0	−12
1	1	−12

(Table 3)

3) CNTL-L, U REGISTER
After the counter of track that must be counted is inputed from Micom, the data is loaded to tracking counter by CNTL-L, U register.

4) CNTL-W REGISTER
It is a register to control CLV-SERVO

	DATA	DATA = 0	DATA = 1	Comment
COM	D3	XTFR/4 and PBFR/4		Phase comparison frequency control during phase mode
WB	D2	XTFR/32	XTFR/16	Bottom hold period control during speed or Hspeed-mode.
WP	D1	XTFR/4	XTFR/2	Peak hold period control during speed mode
Gain	D0	– 12dB	0dB	SMPD gain control during speed or Hspeed-Mode

(Table 4)

5) CNTL-C REGISTER

MODE	D7-D4	D3-D0	SMPD	SMSD	SMEF	SMON
FORWARD	1110	1000	H	HI-Z	L	H
REVERSE		1010	L	HI-Z	L	H
SPEED		1110	SPEED-MODE	HI-Z	L	H
HSPEED		1100	HSPEED-MODE	HI-Z	L	H
PHASE		1111	PHASE-MODE	PHASE MODE	HI-Z	H
XPHSP		0110	SPEED PHASE-MODE	HI-Z or PHASE-MODE	L or HI-Z	H
VPHSP		0101	SPEED, PHASE-MODE	HI-Z or PHASE-MODE	L or HI-Z	H
STOP		0000	L	HI-Z	L	L

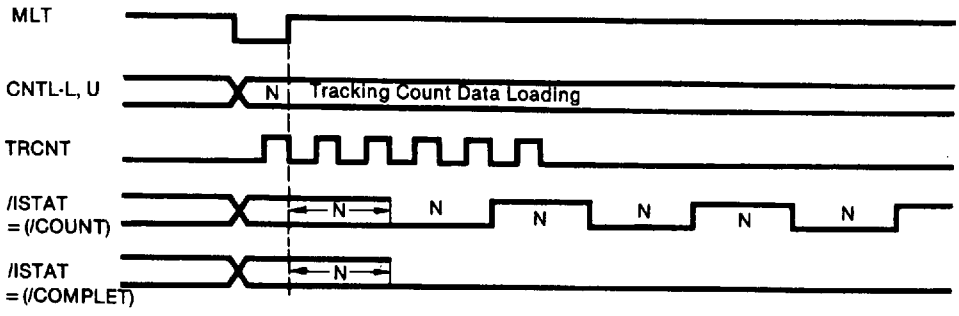
(Table 5)

6) CNTL-D REGISTER
It is a register to control Normal speed mode and Double speed mode.

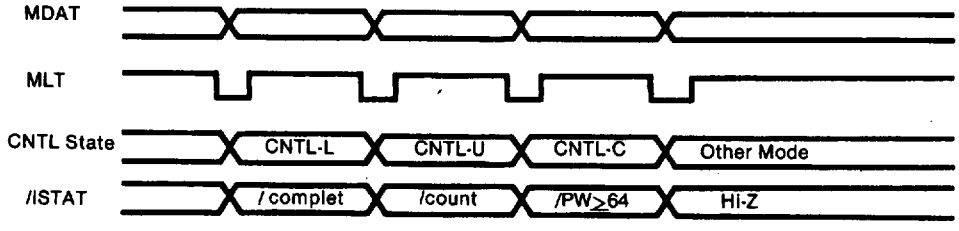
MODE	D7-D4	D3-D0	COMMENT
NORMAL	1111	0000	Normal Speed
DOUBLE		0011	Double Speed

(Table 6)

2. Tracking counter block
This block is used to improve track-jump characteristics.
The number of tracks that are to be jumped are loaded into either register CNTL-L or CNTL-U.
After either register CNTL-L or CNTL-U has been loaded, and at the rising edge of the next MLT, the TRCNT pulse count begins.
When n (if register CNTL-L = register = CNTL-U = 0, then n = 256) is loaded into the register, and then at low level for succeeding pulses. When the address is set in CNTL-U, the signal ($\overline{COUNT}$) TRCNT/2n is output.
The following is timing chart of tracking counter block.



(Fig 2. Tracking Counter timing chart)



(Fig 3. $\overline{ISTAT}$ output signal according to CNTL Register)

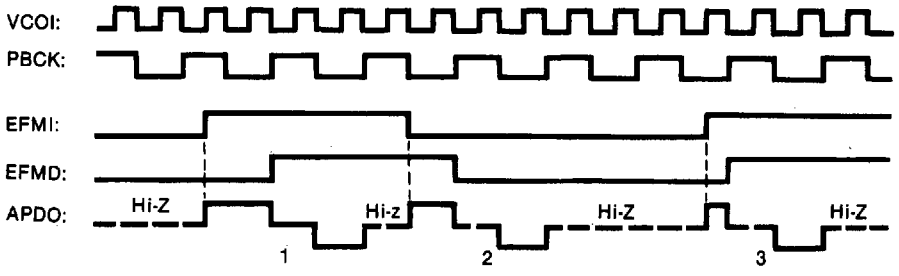
3. EFM demodulation block

The EFM block consists of EFM demodulator which demodulates EFM data obtained from a disc, EFM phase detector and controller etc.

1) EFM phase detector.

As the EFM signal inputed from a disc includes the components of 2.1609MHz, the EFM phase detector uses the Bit clock (PBCK) of 4.3218MHz to detect the phase of this signal.
This PBCK detects the phase at the edge of EFM signal and the result is outputed to the APDO terminal.

A. At Normal operating



In the case of 1: When the EFM signal is slow than VCO
In the case of 2: When the EFM signal is locked with VCO
In the case of 3: When the EFM signal is faster than VOC

(Fig 4. Timing chart of the EFM phase detector)

B. At abnormal operating
If the HIPD of CNTL-Z is "H" and "L" of the LKFS is shorter than 3.5T (a period PBFS is T), the Hi-Z is outputed to APDO terminal as many as "L" and if be over 3.5T, the Hi-Z is outputed as many as 3.5T.

2) EFM demodulator
The 14 Bit data through the circuit changes to demodulate 8 bit data.
Demodulated data has two kind of signal, the one is subcode data and the other is audio data, and that one is inputed into the subcode block and this one is written in the 16K SRAM and performs error correction.

3) Frame sync detector, protector and inserter

A. Frame sync detector
The data consists of frame units, that is, it consists of frame sync, subcode data, PCM data, Redundancy data etc.
The frame sync is detected in order to maintain the sync.

B. Frame sync protector/inserter
Occasionally, the frame sync is omitted or detected in the place where it doesn't exist by the effect of error or Jitter on a disc.
In these cases, we need to protect or insert the signal.
The window is made by using the WSEL to protect the frame sync.
If the frame sync is inputed to window, it is true data and if isn't inputed, it is ignored.
The width of window is determined by WSEL of CNTL-S register.
If the frame sync is not detected in the frame sync protection window, one is inserted from the internal counter block.

When the appointed number of frame is achieved by FSEM, FSEL of CNTL-S register, ULKFS becomes "L" and frame sync protection window is ignored.
The frame sync is received absolutely at that time.
When the frame sync is received, the ULKFS signal becomes "H" and the frame sync in window is received.

LKFS	ULKFS	COMMENT
1	1	Corresponding with playback frame sync and generated frame sync
0	1	① Out of corresponding with playback frame sync and generated frame sync but PBFR Sync is detected in the window selected by WSEL. ② Out of corresponding with PBFR Sync and XTFR Sync, and sync is inserted because it isn't detected in the window selected by WSEL.
0	0	① After insertion as many as the frame decided by FSEM and FSEL of CNTL-S register as frame sync isn't detected in the window. ② In the case that the PBFR sync is not detected continually after ①

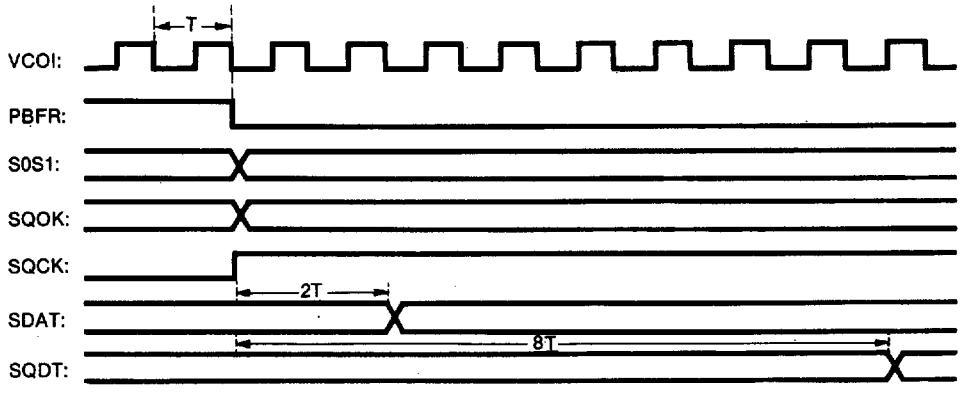
(Table 7)

4) Subcode Block
The 14 Bit subcode sync signal (that is S0, S1) is detected in the sub code sync block.
After S0 + S1 signal is outputed to S0S1 terminal, and the subcode data is outputed to SDAT terminal when the S0S1 signal is "H"
The subcode data among the data inputed to EFMI terminal is demodulated to 8-Bit subcode data (P.Q.R.S.T.U.V.W).
It is synchronized with PBFR signal and it is outputed to SDAT by SBCK Clock
Among the eight subcode data, only Q1 data is selected and loaded to the eighty shift register by PBFR signal

The result of checking the CRC (Cycle Redundancy Check) of loading data is synchronized with S0S1 rising edge and outputed to SQOK terminal.
If the result of checking is error, "L" is outputed to SQOK terminal and if it is true, "H" is outputed to.
And if the CRCD of CNTL-Z Mode is "H", the result of CRC check is outputed to SQDT terminal during from S0S1, "H" to SQCK following edge.

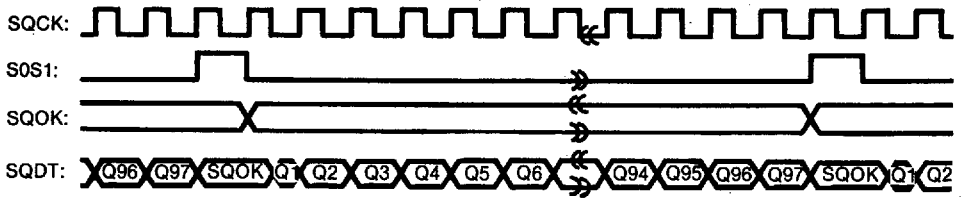
The following is the timing chart of subcode block

1) At SQEN = "L": SDAT, SQDT, S0S1, SQOK, VCOI timing Chart.



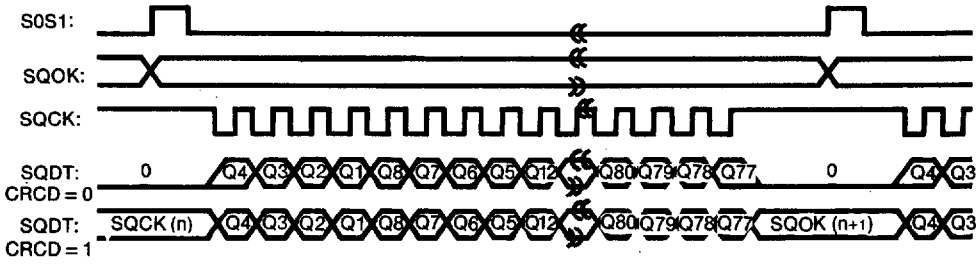
(Fig 5. Subcode-Q Timing Chart 1)

2) At SQEN = "L": SQOK, SQDT, S0S1 timing Chart.



(Fig 6. Subcode-Q timing chart 2)

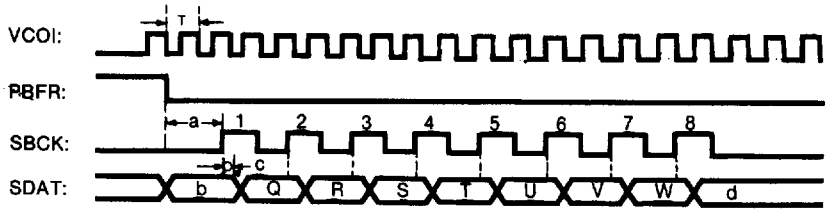
3) At SQEN = "H": SQCK, SQDT, S0S1, SQCK Timing chart.



(Fig 7. Subcode-Q timing chart 3)

Comment: If the SQOK of the subcode Q data is "H" the subcode Data is outputed to SQDT according to SQCK signal.
If the SQOK is "L", it is outputed to SQDT with "L".

4) VCOI, SDAT, SBCK Timing chart.



(Fig 8. Timing chart of subcode data output)

a: After PBFR becomes falling edge, SBCK becomes "L" during about 10μsec.
b: If S0S1 is "L", subcode P is outputed. And if "H", S0S1 is outputed.
c: If a period of VCOI is "T", the width of c is 4T-6T.
d: If the pulse inputed to the SBCK terminal be over seven, subcode Data (P.Q.R.S.T.U.V.W) is repeated.

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4. ECC (Error Correction Code) block

The function of ECC Block is to recover damaged data to some extent when data on a disk is damaged.
By using CIRC (Crossed-Interleave Reed-solomon Code), C1 (32, 28) and C2 (28, 24) errors are corrected.
ECC is performed by the unit of one symbol of eight bit.
In correcting C1, a C1 pointer is generated, and in correcting C2, a C2 pointer is generated.
C1, C2 pointers send error information or the data which ECC is given.
After correcting C2, against uncorrectable data, Error data is sent to display by outputing a C2 flag.
The C2FL signal is handled in the interpolator by using the Signal of C2F1 and C2F2.

C1F1	C1F2	C1, C2 ERROR Status	C2F1	C2F2	C2FL
0	0	NO ERROR	0	0	0
0	1	SINGLE ERROR CORRECTION	0	1	0
1	0	DOUBLE ERROR CORRECTION	1	0	0
1	1	IRRETRIEVABLE ERROR	1	1	1

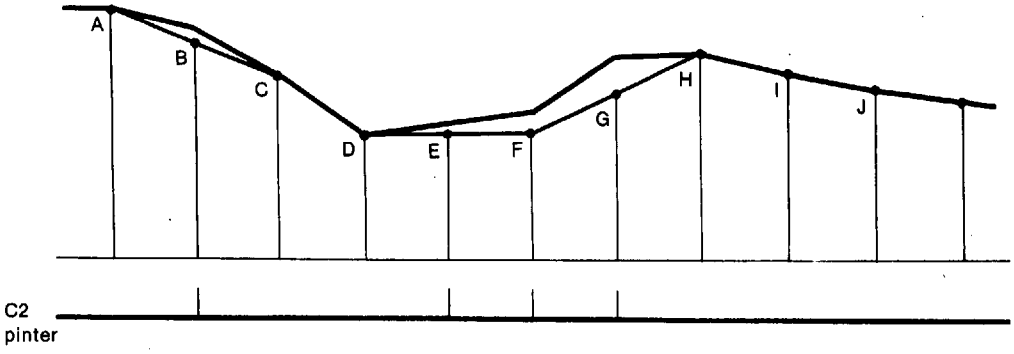
(Table 8)

C1F1, C1F2: The error correct status is outputed by C1 decoder.
C2F1, C2F2: The error correct status is outputed by C2 decoder.
C2FL: In the case that the error can't be corrected by C2 decoder, becomes "H", and the reverse case becomes "L".

5. Interpolator/Mute block

1) Interpolator
When a Burst error occurs on a disc, sometimes the data can't be corrected even if a ECC process is performed.

The interpolator block revises data by using a C2 pointer outputed through the ECC block.
The data inputed to a data bus is inputed to the left and right channel, respectively, in the order of C2 pointer, Lower 8-bit, and upper 8-bit.
A pre-hold method is taken when a C2 pointer is "H" continuously.
In case of the occurrence of a single error, an average interpolation method is carried out with the range of the data before and after an error happens.
When a check against a checked cycle is "L", R-CH data is outputed. L-CH data is outputed when the check is "H".



$B = \frac{A+C}{2}$: AVERAGE INTERPOLATION

F = E = D : PREVIOUS DATA HOLD

$G = \frac{F+H}{2}$: AVERAGE INTERPOLATION

(Fig 9. Interpolation)

4

2. Mute and Attenuation
By using a mute terminal and the ATTM signal of the CNTL-S Register, Audio data is muted or attenuated. There are two kinds of mute: Zero-Cross muting and muting

A. Zero-Cross muting
The audio data is muted, after ZCMT of CNTL-Z register goes to "H", and in case that mute is "H" and the upper 6 Bit of audio data become all "L" or "H".

B. Muting
The audio data is muted when ZCMT of the CNTL-Z register is "L" and mute terminal is "H".

C. Attenuation
The signal attenuation is occured by ATTM of the CNTL-S register and mute signal as following.

ATTM	MUTE	Degree of Attenuation
0	0	0dB
0	1	$-\infty$dB
1	0	-12dB
1	1	-12dB

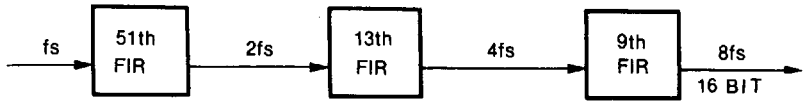
(Table 9)

6. Digital Filter

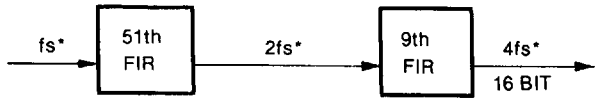
The KS9282B has a built-in FIR (Finite impulse response) Digital filter
This Digital filter Consists of 8 over sampling filter.

A. Block Digram

1. Normal Speed Play mode

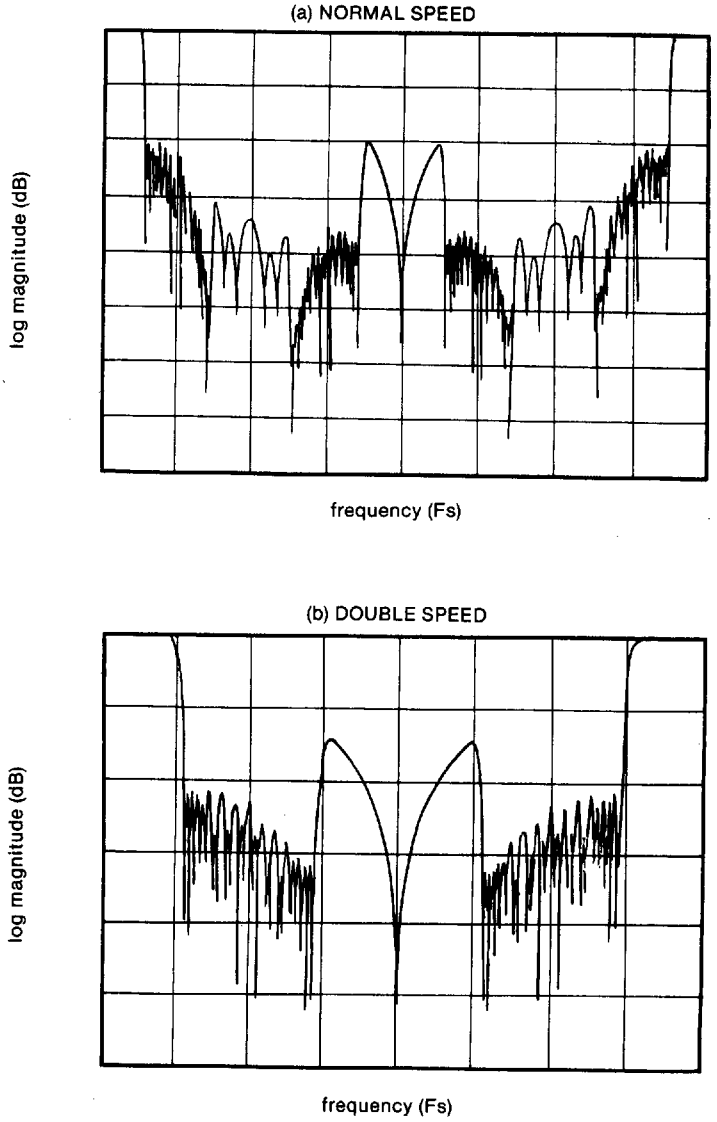


2. Double Speed Play mode



(Fig. 10 Digital filter block digram)

B. Filter characteristic
1. Ripple in passband: Within ±0.5dB
2. Attenuation in stopband: below −42dB

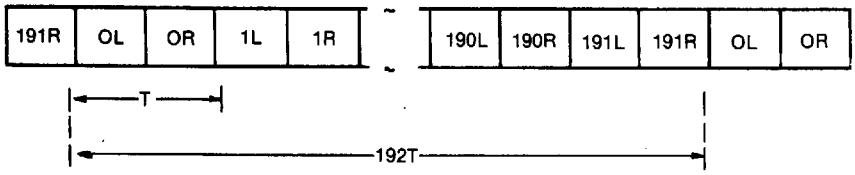


(Fig 11. Filter Characteristic Curve)

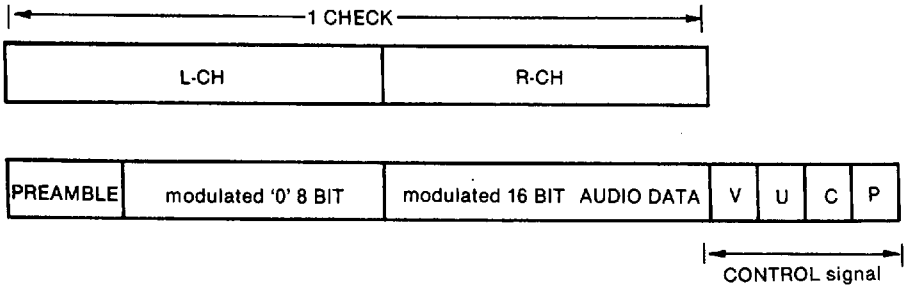
7. Digital audio out block

The 2-channel, 16-Bit data is connected and outputed serially to other digital system by the digital Audio interface format.

1) Digital audio interface format for CD



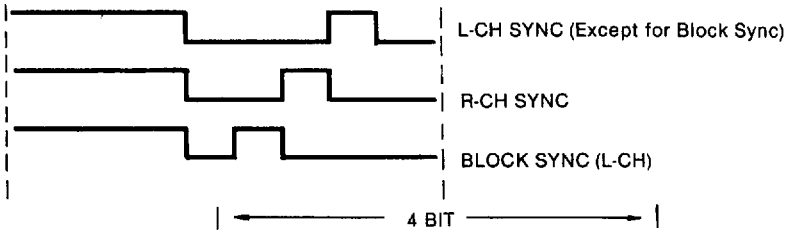
OL: L-CH format included block sync preamble
1L ~ 191L: L-CH format included L-CH sync preamble
0R ~ 191R: R-CH format included R-CH sync preamble



(Fig 12. Digital audio out format)

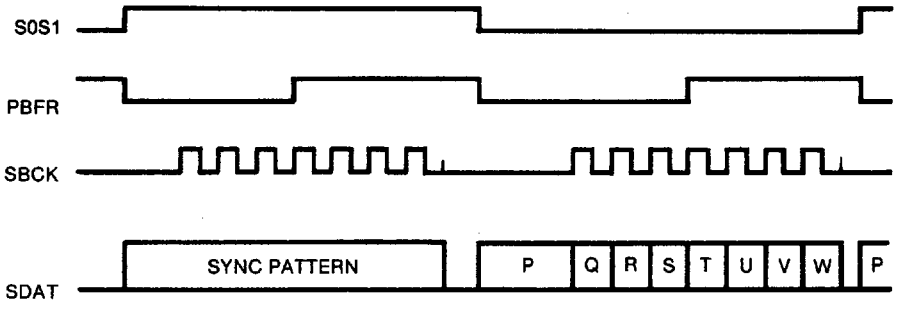
A. Preamble

It is used to discriminated against the block sync of data and L/R-channel of data.



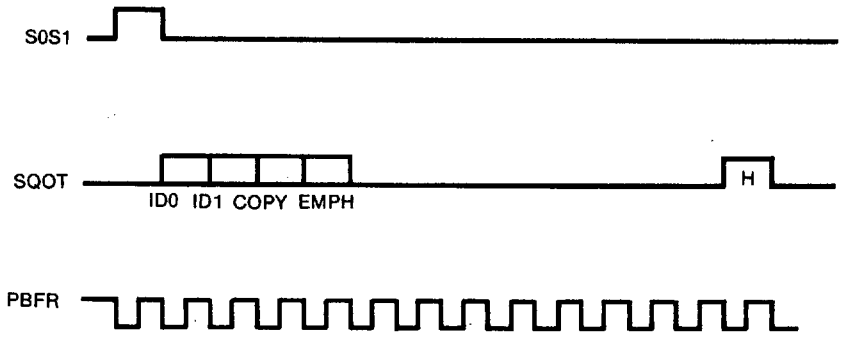
(Fig 13. Preamble Signal)

B. Control Signal
1 Validity bit: It is indicated that the error of 16-Bit audio data exists, or don't ("H" Error, "L": Valid data)
2 User definable bit: Subcode data input.



(Fig 14. Timing chart of digital audio out)

3. Channel status bit:Output a high position information of 4-bit of subcode Q indicate the number of channel, preemphasis and copy etc.
Indicate CDP category



(Fig 15. Timing chart of channel status data output)

4 parity bit: Making even parity

8. CLV Servo block
The CNTL-C register is selected to control CLV (Constant Linear Velocity) servo by the data inputed from Micom In the CNTL-C register, the CLV servo action mode isappointed by the data inputed from Micom to control the spindle motor.

1) Forward Mode
The terminal condition of output mode is that SMPD is "H", SMSD is "Hi-Z", SMEF is "L" and SMON is "H".

2) Reverse mode
The condition of reverse mode is that SMPD is "L", SMSD is "Hi-Z", SMEF is "L" and SMOD is "H".

3) Speed-Mode
The spindle motor is controlled roughly by the mode when track jumping or EFM phase is unlocked.
If a period of VCO is "T", the pulse width of frame sync is 22T.
In case that the signal detected from EFM signal exceed "22T" by noise on the disk... etc., it must be removed, if not, the right frame sync can't be detected. In these case, the pulse width of EFM signal is detected by period of XTFR/2 or XTFR/4 and the pulse width of EFM singal is detected by the period of XTFR/16 or XTFR/32.

*Peak hold clock is XTFR/2 or XTFR/4, and bottom hold clock is XTFR/16 or XTFR/32

The detected value is used for syncronized frame signal.
If syncronized frame signal is less than 24T, the SMPD terminal outputs 'L', equal to 22T, outputs 'Hi-Z', and more than 23T. outputs 'H'.
If the gain signal of CNTL-W Reg is L the output of SMPD terminal is reduced up to-12 dB. If it is 'H', there is no reduction. (refer to figure 4)
Output conditions SMSD = HI-z SMEF = 'L' SMON = 'H'

4) Hi-speed-Mode
The mirror does main of track which havn't pit is duplicated with 20KHz signal to EFM.
In this case, servo action be to unstable because the peak value of mirror singal which is longer than original frame sync signal is detected. In Hi-speed mode, by using the 8.4672/256 MHz signal against peak hold and XTFR/16 or XTFR/32 signal against bottom hold, the mirror is removed, and hi-speed servo action be to stable. Output is that SMSD is 'Hi-z', SMEF is 'L' SMON is 'H".

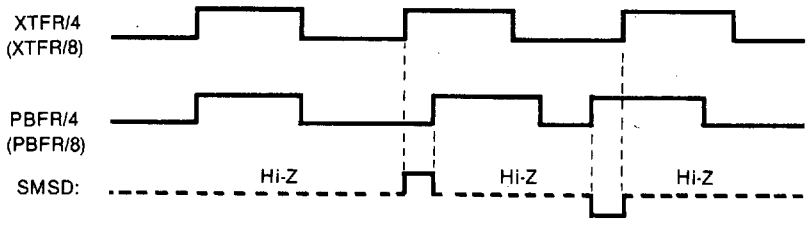
5) Phase-Mode
The mode for controls EFM phase. Phase difference between PBFR/4 and XTFR/4 is detected when NCLV of CNTL-Z is 'L' and phase difference between Read Base Counter/4 and Write Base Counter/4 is detected when NCLV is 'H', and the difference is outputed to SMPD.

'H' is outputed from falling edge of PBFR during (WPO-278T)×32 to SMSD terminal and 'L' is outputed up to falling edge of next PBFR.(refer to figure 5)

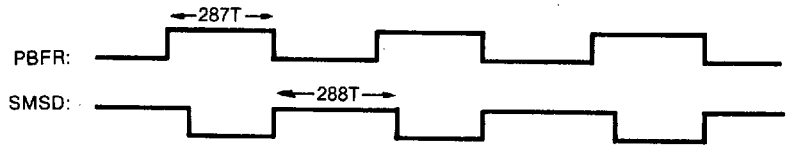
6) XPHSD-Mode
The mode for using normal action.
The LKFS signal made from frame sync block is to sampling which period is PBFR. If sampling is 'H', Phase Mode is performed, and if the sampling is eight of 'L' continuously, speed mode is performed automatically. Selecting Peak hold period of speed mode, and bottom hold period and gain of speed/hi-speed mode is determined by CNTL-W Reg.

7) VPHSP – Mode
The mode to controls rough servo. Instead of X'tal VCO is used to test EFM pattern.
If the center value of VCO is varid the rotation of spindle motor is varied to same direction and VCO is locked easily.

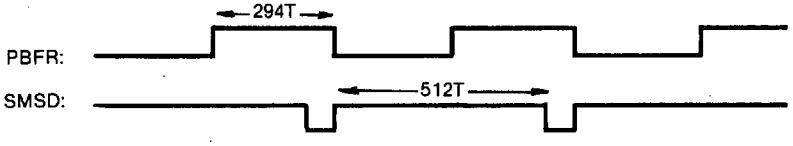
8) STOP
The mode for stop spindle motor. Output is that SMDP is 'L', SMSD = 'Hi-Z' SMEF is 'L', and SMON is 'L'.



(Fig 16 Timing chart of SMSD output)

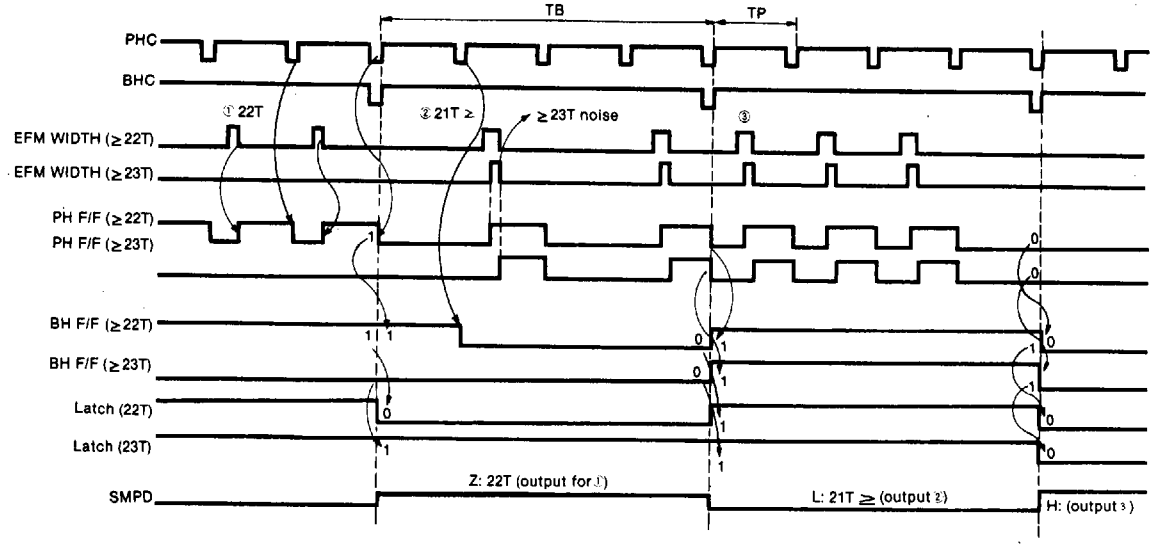


(a) Timing chart of SMSD output when PBFR is "287T".



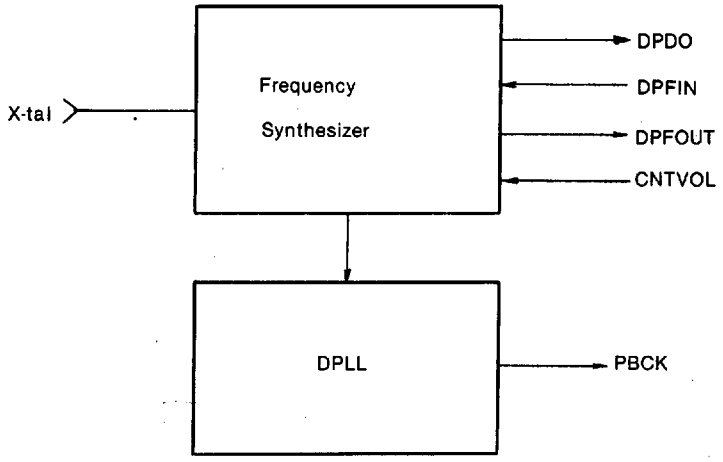
(b) Timing chart of SMSD output when PBFR is "294T

(Fig 17. Timing chart of SMSD output at phase mode)



(Fig 18. Timing chart of SMPD output when the Gain is "H" in the speed Mode).

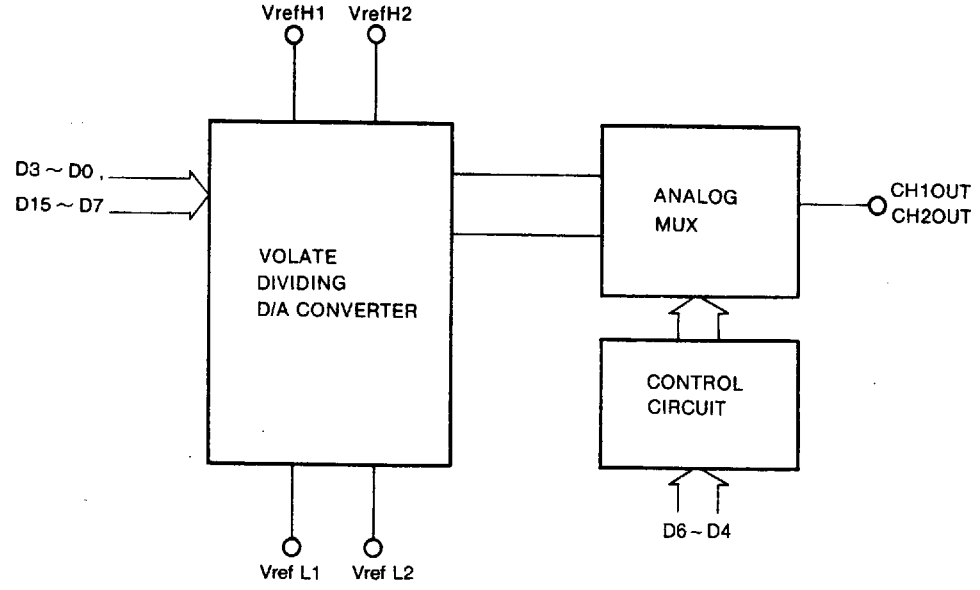
9. Digital PLL Block
This device contains Analog PLL and digital PLL together in order to obtain the stable channel Clock for demodulating EFM signal.
The application diagram of digital PLL is as follows.



(Fig 19. Digital PLL Circuit diagram)

10. D/A Converter (Digital to Analog Converter)
The KS9282B has a built-in 16-Bit D/A converter.
Digital audio data is a 2's complement serial signal. (MSB first)

A. Vref terminal (See. Fig 20)
Vref, the reference voltage across a resistor-ladder, is usually recommended with vrefH1 = 5V, VrefL1 = 0V. One way of avoiding an amplitude mismatching between the Vref and op amp input connected to the output of the D/A converter is to reduce the analog output amplitue with VrefH2 = 5V and VrefL2 = 0V (at this time about /100μF) Capacitor should be connected from VrefH1 and VrefL1 to GND) By the effect of built-in RH and RL with this choice, the maximum analog output amplitude results in a narrow range of about 1.5 ~ 3.5V for 0dB playback.



(Fig 20. Vref relation circuit)

B. D/A Converter Electrical Characteristic
The D/A Converter electrical characteristic built in KS9282B is as follows.

(V_{DD}=5V, V_{SS}=0V T_a = 25°C)

Characteristics	Symbol	Test condition	Min	Typ	Max	Unit
Total harmonic distortion	THD	DATA = 1KHz, 0dB	—	—	0.08	%
Signal to noise ratio	S/N	V_{DD} = 4.5V DATA = 1KHz, 0dB	—	92	—	dB
Cross talk	CT	DATA = 1KHz, 0dB	—	– 85	—	

(Table 10)