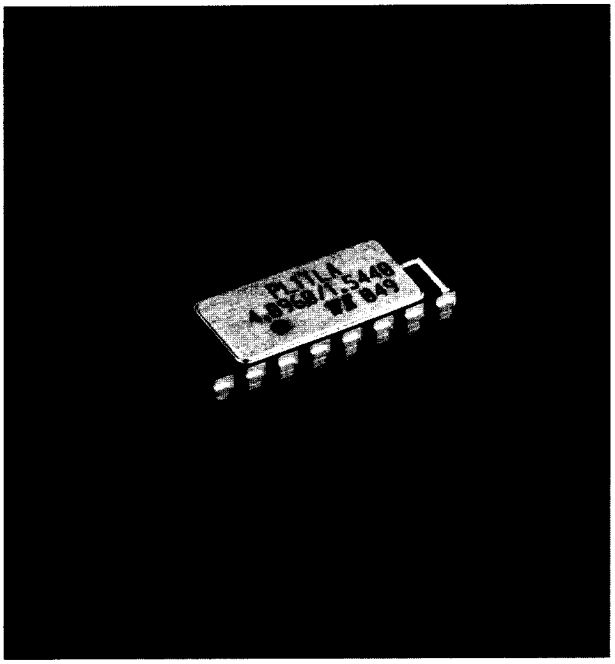
Data Sheet

T1 (DS-1 and CEPT-1) Frequency Translator: PLXO



The AT&T T1 Frequency Translator.

Features

- Translates from:
  —CEPT-1 x 2 (4.096 MHz) to DS-1 (1.544 MHz)
  —CEPT-1 x 2 (4.096 MHz) to DS-1C (3.152 MHz)
  —DS-1 (1.544 MHz) to CEPT-1 x 2 (4.096 MHz)
  —DS-1C (3.152 MHz) to CEPT-1 x 2 (4.096 MHz)
- 3-state option for board-level testing
- Compact 16-Pin DIP
- Fast acquisition time and low noise output
- Machine insertable
- Free-run mode on loss of input signal
- Surface mountable
- Loss of lock indicator
- Loss of input clock indicator

Description

The Phase-locked Crystal Oscillator (PLXO) is a 16-pin, ceramic packaged device that provides frequency translation between telephone standard reference clocks associated with the DS-1, DS-1C, and CEPT-1 transmission rates. Frequency translation is accomplished using an internal, voltage-controlled crystal oscillator (VCXO) based phase-locked loop and user-supplied passive filter elements. The internal phase-locked loop provides two modes of operation. In locked mode, a low-pass filter with a large time constant (narrow bandwidth) is selected to provide a low noise output. In an out of lock mode, a low-pass filter with a small time constant (wide bandwidth) is selected to provide fast acquisition of the inbound clock. By comparing the relative edges of 8 kHz clocks supplied by the input clock and the internal VCXO, the phase detector determines if the loop is in or out of lock. Once lock is achieved, the phase detector switches from wide bandwidth filtering to narrow bandwidth filtering. To achieve this switch, the two outputs of the phase detector (FSTFLT and SLWFLT) are alternately set to a high-impedance state and drive a lead-lag filter created using user-supplied elements.

The PLXO will fully track the long-term stability of an inbound clock to ±130 ppm of the nominal value over its full power supply and temperature range (–40 °C to +85 °C). At 25 °C, with V_{DD} equal to 5 V, and no inbound clock present, the free-run frequency of the VCXO (at CLKOUT) will fall within ±75 ppm of the nominal value. The CLKOUT frequency will fall within ±130 ppm of the nominal value over the VCXO's full voltage and temperature range.

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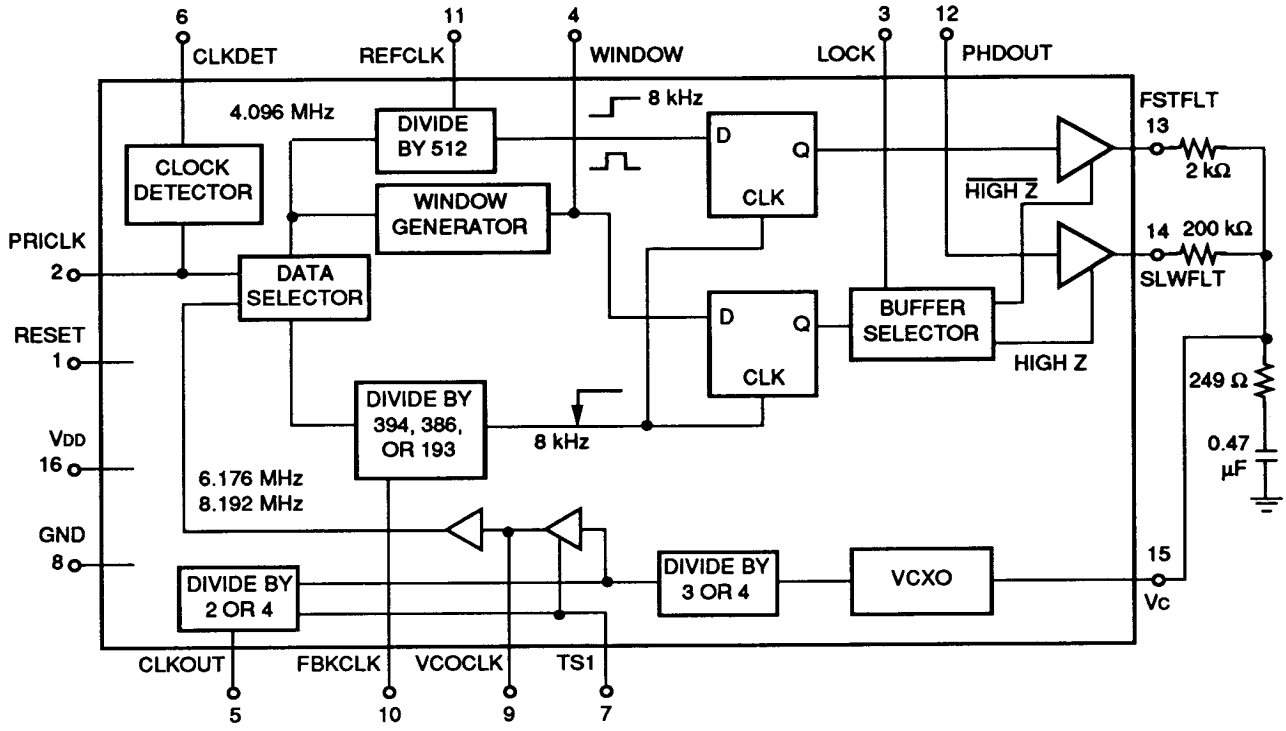


Figure 1. PLXO Functional Block Diagram

Pin Information

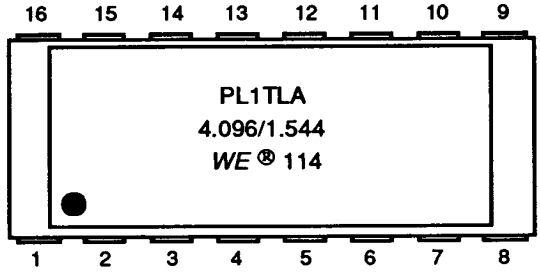


Figure 2. Pin Diagram

Table 1. Pin Descriptions

Pin #	Type	Symbol	Function
1	I	RESET	TTL logic low sets the output buffers of LOCK, WINDOW, CLKOUT, CLKDET, FBKCLK, REFCLK, PHDOUT, FSTFLT, and SLWFLT to a high-impedance state. If no input clock (PRICLK) is present, VCOCLK and CLKOUT go to a free-run mode. If PRICLK is present, the user may control VCOCLK and CLKOUT by varying Vc from 0 V to 5 V. When set to a logic low, a positive edge applied to both PRICLK and VCOCLK will reset all internal logic except the CLKOUT divider. The positive edge, applied to VCOCLK, may be generated either internally by the VCXO or externally by setting TS1 to a TTL logic low and applying a clock to VCOCLK (pin 9). RESET is internally pulled to TTL logic high during normal operation.
2	I	PRICLK	Primary clock input to which CLKOUT and VCOCLK are locked.
3	O	LOCK	Lock is set to a TTL logic high if the positive edge of the 8 kHz clock derived from VCOCLK is within 244 ns of the positive edge of REFCLK. Otherwise, LOCK is set to a TTL logic low.
4	O	WINDOW	This 488 ns pulse occurs at an 8 kHz rate and is centered about the positive edge of the 8 kHz clock derived from PRICLK.
5	O	CLKOUT	The output clock derived from VCOCLK.
6	O	CLKDET	Clock detect is a TTL logic high if a clock is present at pin PRICLK. This pin drops to a TTL logic low if no clock is applied to PRICLK.
7	I	TS1	A TTL logic low at Test Signal 1 (TS1) disables the output buffer from the VCXO and sets the CLKOUT divider to a divide-by-two mode. The user may then inject a test signal at VCOCLK for external circuit testing.
8	I	GND	Circuit and cover ground.
9	I/O	VCOCLK	An output clock derived from the internal on-chip VCXO based phase-locked loop. This pin also serves as an input for test signals with TS1 set to a TTL logic low.
10	O	FBKCLK	16 kHz clock derived from VCOCLK.

Pin Information (continued)

Table 1. Pin Descriptions (continued)

Pin #	Type	Symbol	Function
11	O	REFCLK	8 kHz clock derived from the user-supplied PRICLK.
12	O	PHDOUT	The phase detector output is a TTL logic high if the positive edge of REFCLK leads the positive edge of the 8 kHz clock derived from VCOCLK. The pin is a TTL logic low if the positive edge of the REFCLK lags the positive edge of the 8 kHz clock derived from VCOCLK.
13	O	FSTFLT	This phase detector output drives a relatively wide bandwidth passive loop filter to provide fast acquisition of PRICLK on start-up. If LOCK is a TTL logic high, this output goes to a high-impedance state.
14	O	SLWFLT	This phase detector output pin drives a relatively low bandwidth lead-lag passive loop filter. If LOCK is a TTL logic low, this output is set to a high-impedance state until LOCK returns to a TTL logic high.
15	I	Vc	Control voltage input to internal VCXO. Both the lead-lag passive filter SLWFLT and the wide-band passive filter FSTFLT are connected to this input.
16	I	V_{DD}	5.0 V ± 10% supply voltage.

Handling Precautions

Although protection circuitry has been designed into this device, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting. AT&T employs a human-body model (HBM) and a charged-device model (CDM) for ESD-susceptibility testing and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used to define the mode. Although no industry-wide standard has been adopted for the CDM, a standard HBM (resistance = 1500 Ω, capacitance = 100 pF) is widely used and therefore can be used for comparison purposes. The HBM ESD threshold presented here was obtained by using these circuit parameters.

Table 2. ESD Threshold Voltage

Model	ESD Threshold, Minimum	Unit
Human Body	2500*	V
Charged Device	500	V

* MIL-STD-1686-8/8/88, Class 2.

Electrical Specifications

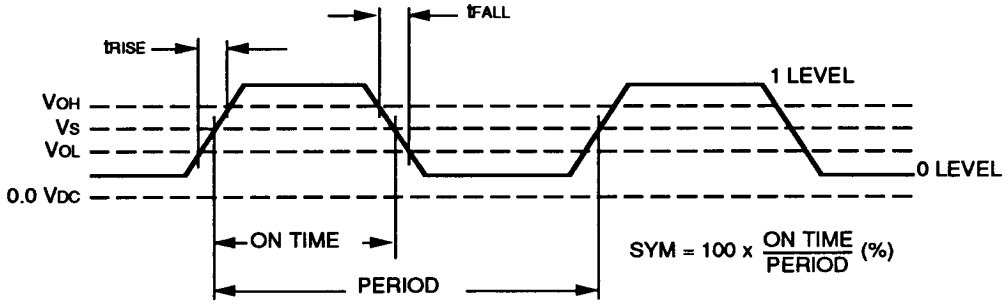


Figure 3. Output Waveform

Table 3. General Electrical Specifications

WARNING: Unit will be severely damaged if inserted backwards in a circuit.

Parameter	Symbol	Min	Max	Unit
Nominal Primary Clock Input Frequency	PRICLK	See Table 4.		MHz
Nominal Output Clock Frequency Nominal Output VCXO Clock Frequency	CLKOUT VCOCLK	See Table 4. See Table 4.		MHz
Supply Voltage	VDD	4.5	5.5	V
Supply Current (VDD = 5.50 V)	IDD	5	30	mA
Input Voltage Levels: Input Logic High* Input Logic Low*	 VIH VIL	 2.0 —	 — 0.8	 V V
Output Voltage Levels: Output Logic High* Output Logic Low*	 VOH VOL	 2.5 —	 — 0.5	 V V
Transition Times:* Rise Time (0.5 V to 2.5 V) Fall Time (2.5 V to 0.5 V)	 tRISE tFALL	 0.5 0.5	 5.0 5.0	 ns ns
Symmetry or Duty Cycle† (options 1 and 2): Output Clock Output VCXO Clock	 CLKOUT VCOCLK	 45 45	 55 55	 % %
Symmetry or Duty Cycle† (options 3 and 4): Output Clock Output VCXO Clock	 CLKOUT VCOCLK	 45 28	 55 38	 % %
Nominal Output Frequency on Loss of Signal: Output Clock (VDD = 5 V, 25 °C) Output VCXO Clock (VDD = 5 V, 25 °C)	 CLKOUT VCOCLK	 –75 ppm –75 ppm	 +75 ppm +75 ppm	 ppm from FNOM ppm from FNOM
Loss of Lock Indication:‡ Output Logic High* Output Logic Low*	CLKDET– VOH VOL	 2.5 —	 — 0.5	 V V
Primary Clock Input Frequency Variation	ΔFNOM	–130	130	ppm

* Figure 3 defines these parameters.
† Symmetry or Duty Cycle is the ON TIME/PERIOD with Vs = 1.4 V for TTL, per Figure 3.
‡ The loss of signal (CLKDET) indicator is set to a TTL logic high if a clock is present at pin PRICLK. CLKDET is set to a TTL logic low if no clock is detected.

Electrical Specifications (continued)

Table 4. Frequency Translation Options

Option	Input Clock (PRICLK)	Output Clock (CLKOUT)	VCXO Clock (VCOCLK)
1	4.096 MHz	1.544 MHz	6.176 MHz
2	4.096 MHz	3.152 MHz	6.304 MHz
3	1.544 MHz	4.096 MHz	8.192 MHz
4	3.152 MHz	4.096 MHz	8.192 MHz

Mechanical Characteristics

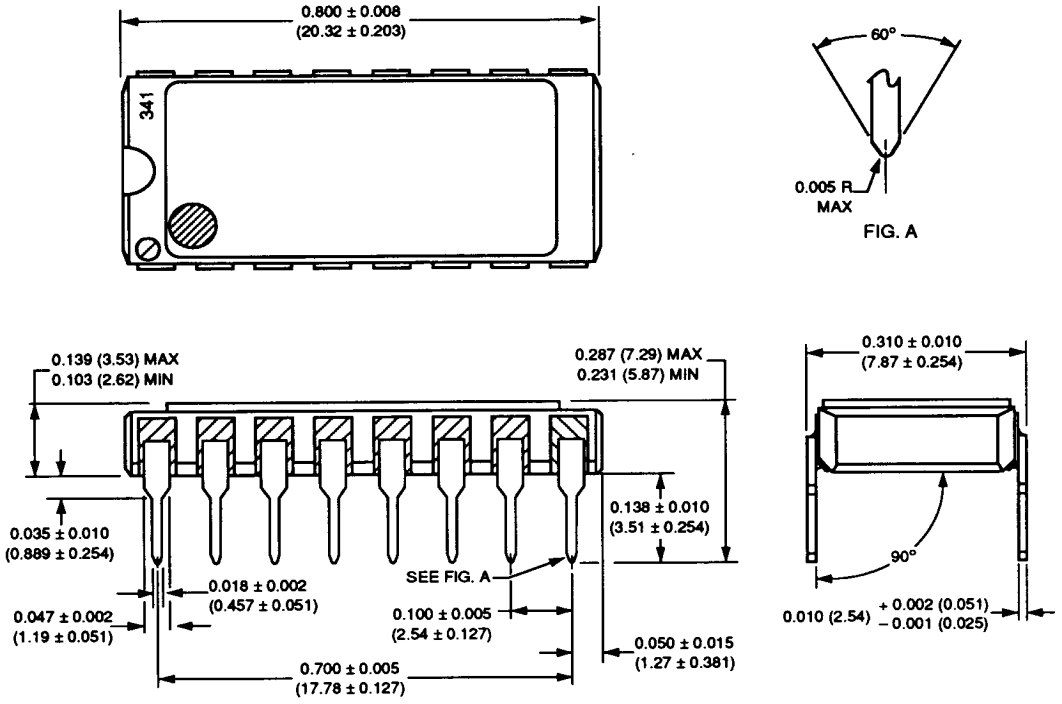
Table 5. Mechanical and Environmental Conditions

Parameter	Value
Mechanical Shock	MIL-STD-883C 2002.3 Test B
Mechanical Vibration	MIL-STD-883C 2007.1 Test C
Solderability	MIL-STD-883C 2003.5
Gross Leak Test	MIL-STD-883C 1014.7
Fine Leak Test	MIL-STD-883C 1014.7
Storage Temperature	–55 °C to +125 °C

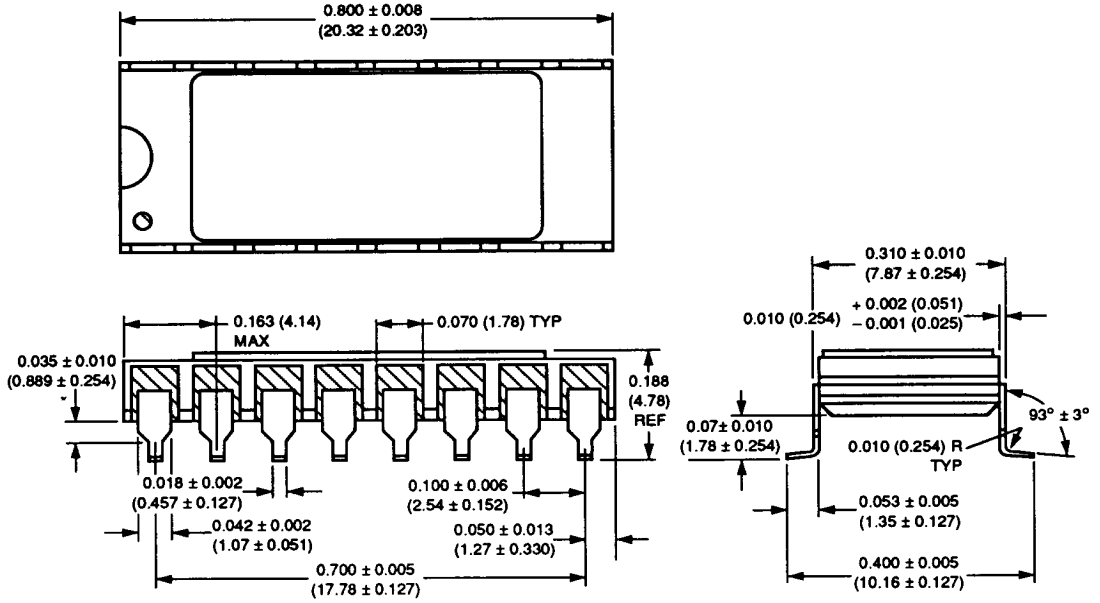
Outline Diagrams

Dimensions are in inches and (millimeters).

PLXO Thru-Hole Package



PLXO Gull-Wing Package



Ordering Information

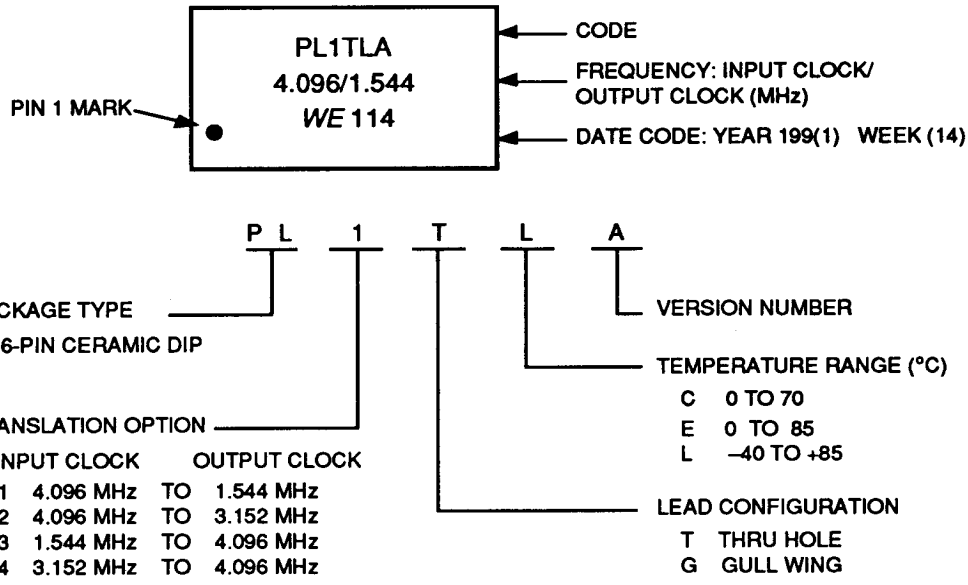


Figure 4. Part Numbering Information

For additional information, contact your AT&T Account Manager or the following:
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