I-Cube

PS48 Data Sheet

Features

- SRAM-based, In–system Programmable
- Non-Blocking Switch Matrix
  - User Configurable Datapath Width of 1, 4, 8, or 16 bits
  - Identical and Predictable Delays
- 48 I/O Ports
  - Individually Programmable as Input, Output or Bidirectional
  - Programmable Clock, Clock Enable, Tristate and Direction Control
  - 16 mA Current Drive
  - Separated Power Pins for Easy Interfacing to 3V/3.3V signals
- RapidConnect™ Interface for Fast, Incremental Switching of Datapaths in 20 ns
- Clocked, Latched and Flow–through Dataflow Modes
  - 10 ns Port–to–Port Delay in Flow–through Mode
  - 100 MHz Clock Frequency
- One–to–One, One–to–Many and Many-to-One Connections
- JTAG Compliant

Description

PS48 is the first member in the *Programmable Switching* device family from I-Cube. The PS48, manufactured using 0.8μm CMOS process, offers high performance and significant architectural flexibility.

The PS48 is designed for use in applications requiring dynamic switching of wide datapaths, such as networking, image processing and high performance computers.

At the heart of the PS48 device is a non–blocking, switch matrix. Using the RapidConnect interface, the signal lines in the switch matrix can be switched individually, or in groups of 4, 8, or 16. The switch matrix lines are connected to I/O ports whose functional attributes are programmable. The PS48 support either flow–through, latched or clocked signal flow. The delays through the device are uniform and predictable.

The connections through the switch matrix and the functional attributes of the I/O ports are programmed by storing data in the switch matrix SRAM cells and I/O block registers.

The PS48 devices support an industry standard JTAG (IEEE 1149.1) interface for boundary scan testing.
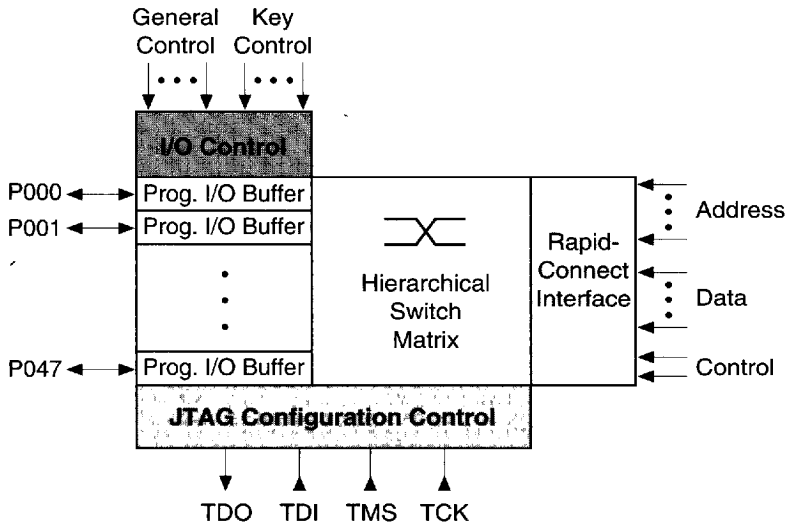

Figure 1: PS48 Functional Block Diagram

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Architecture

The PS48 use SRAM cells for storing configuration information. The device can be configured in–system by storing appropriate data into the internal SRAM cells and registers. The main functional blocks of the device are the switch matrix, programmable I/O ports, I/O control signals, RapidConnect switching interface, and JTAG–based configuration controller.

The I/O ports on the device are programmable and are connected to the lines in the switch matrix. The I/Os can be connected to each other by establishing connections among the corresponding switch matrix lines. The control signals, such as clock, clock enable, tristate, and direction control, are used to control the operation of the I/O ports in certain programmed modes.

The RapidConnect interface is used to directly address the SRAM cells controlling the connections. Using RapidConnect the contents of these SRAM cells and therefore the connections among individual or groups of I/O ports can be changed rapidly.

The JTAG–based serial configuration controller decodes the incoming configuration bit stream and stores configuration data into I/O blocks and switch matrix SRAM cells thereby establishing the desired functional attributes for the I/O ports and their connections through the switch matrix.

Switch Matrix

The switch matrix is an array of pass transistors, each controlled by an SRAM cell. The ON and OFF states of the transistor switches are determined by the contents of the corresponding SRAM cell. The switch matrix is non–blocking. This implies that a connection between any two I/O ports can always be established regardless of the state of other connections in the switch matrix. Moreover, only one switch needs to be turned ON in order to make a connection between a pair of I/O ports. This architecture offers guaranteed connections, and uniform and predictable delays.

A connection can be altered (a new connection made or existing connection broken) without affecting other connections, allowing incremental reconfiguration of the switch matrix.

The PS48 switch matrix, shown in Figure 2, uses a hierarchical structure, allowing connections among individual lines or 4, 8 or 16–line groups. Multicasting/broadcasting operation is supported by allowing one switch matrix line to connect to multiple other lines.
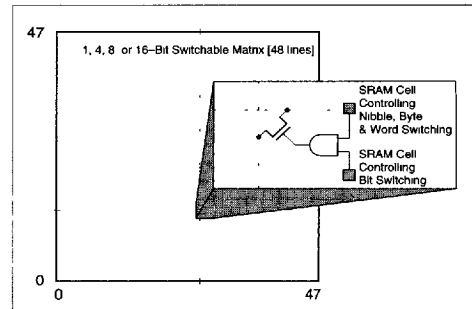

Figure 2: PS48 Switch Matrix

Programmable I/O Buffer

Each line in the switch matrix is connected to a programmable I/O port. The PS48 has a total of 48 I/O ports, P000–P047. The functional attributes of each I/O port are individually programmable. The programmable attributes include signal direction (I/O/B), data flow mode, clock, clock enable, tristate and direction control, clock, tristate and direction control polarity, output voltage level and pull–up current. As one of the programmable options, the I/O buffers can be bypassed.

A pool of 8 general purpose control signals, available through the pins GC0–GC7, is used for clock, tristate and direction control signals. In addition, the Key port, K0–K3 provides clock enable capability. These features are further explained in the section on "I/O Control Signals".

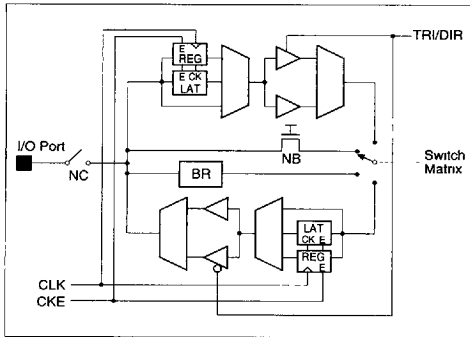Figure 3 shows the structure of the programmable I/O buffer for the PS48.

Figure 3: PS48 Programmable I/O Buffer

I/O/B Functional Attributes

Figure 4 shows the I/O/B functional attributes supported in the PS48. These are described in the following section.

Input Modes

Input (IN) - In this mode, the external signal at the I/O port pin is connected to the corresponding switch matrix line through an input buffer.

Registered Input (RI) - In this mode, the external signal at the I/O port pin is connected to the corresponding switch matrix line through a edge–sensitive register. By default, the clocking action takes place on the rising edge.

Latched Input (LI) - In this mode, the external signal at the I/O port pin is connected to the corresponding switch matrix line through a level–sensitive latch. The default setting is: transparent when the clock signal is high and latched when the clock is low.

In the input modes (IN, RI, LI), the driving of the corresponding switch matrix line can be controlled by a tristate signal. When used, the default is: driving when high and Hi–Z when low.

Output Modes

Output (OP) - In this mode, the corresponding switch matrix line is connected to the I/O port pin through an output buffer.

Registered Output (RO) - In this mode, the corresponding switch matrix line is connected to the I/O port pin through an edge–sensitive register. By default, the clocking action takes place on the rising edge.

Latched Output (LO) - In this mode, the corresponding switch matrix line is connected to the I/O port pin through a level–sensitive latch. The default setting is: transparent when the clock signal is high and latched when the clock is low.

In the output modes (OP, RO and LO) the I/O buffer can be programmed to use an output enable (tristate) signal. When used, the default is: driving when low and Hi–Z when high.

Bidirectional Modes

Bidirectional Transceiver (BT) - In this mode, the I/O buffer acts as a bidirectional transceiver between the I/O port pin and the corresponding switch matrix line. The signal direction is controlled by the direction control signal. The direction control signal. The default setting is: output mode (drive the I/O pin) when direction control signal is low and input mode (drive the switch matrix line) when direction control signal is high.

In this mode, the signal can optionally be registered or latched in one or both directions.

Bus Repeater (BR) - In this mode, the I/O buffer acts as a bidirectional buffer between the I/O port pin and the corresponding switch matrix line. This unique mode, patented by I-Cube, does not require a direction control signal. The on–chip circuitry senses the driving end (input) and internally drives the other side, thus "repeating" the signal.

When multiple I/O ports configured as "Bus Repeater" are connected together through the switch matrix to form a single internal node, a signal appearing at any one of the I/O ports gets repeated (or broadcast) to other I/O ports.
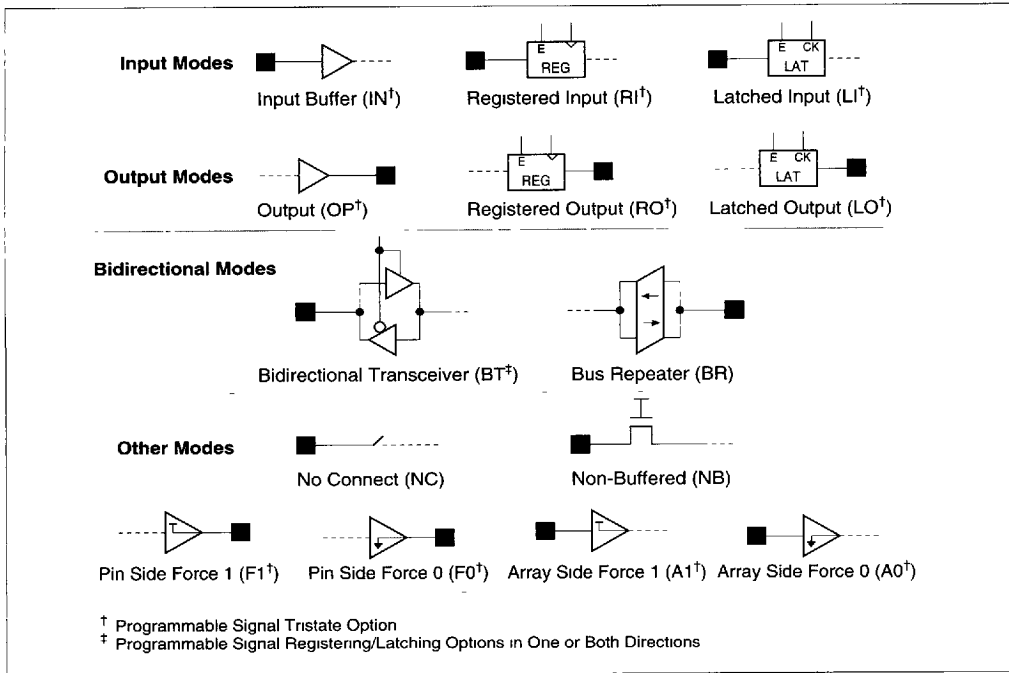
Figure 4: PS48 I/O/B Attributes

I/O/B Function	Data Flow	Tristate Function	Mnemonic (used by I-Cube software)
Input	Flow–through	Yes	IN
	Registered	Yes	RI
	Latched	Yes	LI
Output	Flow–through [1, 2]	Yes	OP
	Registered [1, 2]	Yes	RO
	Latched [1, 2]	Yes	LO
Bidirectional [Transceiver]	[3]	[4]	BT [&R I &LI] [&RO I &LO] [5]
Bidirectional [Bus Repeater]	Flow–through	No	BR
Pin Side Force 0 or 1	Not Applicable	Yes	F0, F1
Array Side Force 0 or 1	Not Applicable	Yes	A0, A1
Non Buffered	Flow–through	Not Applicable	NB
No Connect	Not Applicable	Not Applicable	NC

NOTES:
[1] Voltage level can be programmed as TTL or CMOS.
[2] Additional pull–up current of 2.5 mA or 12.5 mA can be programmed (for CMOS level only).
[3] Data can be registered/latched in input, output or both directions.
[4] In this mode, it is Direction Control.
[5] [ ] ≡ optional, I ≡ either or.

Table 1: Summary of Programmable I/O Attributes for PS48

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Other Modes

Pin Side Force 0 (F0) - In this mode, the I/O port pin is forced low (logic 0), regardless of the signal on the corresponding switch matrix line.

Pin Side Force 1 (F1) - In this mode, the I/O port pin is forced high (logic 1), regardless of the signal on the corresponding switch matrix line.

Array Side Force 0 (A0) - In this mode, the switch matrix line is forced low (logic 0), regardless of the signal on the corresponding I/O port.

Array Side Force 1 (A1) - In this mode, the switch matrix line is forced high (logic 1), regardless of the signal on the corresponding I/O port.

In the above four modes (F0, F1, A0 and A1) the I/O buffer can be programmed to use an a tristate control signal. When used, the default for F0 and F1 is: driving when low and Hi–Z when high, and for A0 and A1, it is: driving when high and Hi–Z when low.

Non–Buffered (NB) - In this mode, the I/O port pin is connected to the corresponding line in the switch matrix through a pass transistor, bypassing the buffer.

No Connect (NC) - In this mode, the I/O port pin is isolated from the switch matrix. This is done by tristating both the input and output part of the I/O buffer. Upon reset (either a hardware reset – TRST* = 0 or a JTAG reset – TMS = "11111"), all I/O ports are automatically configured as No Connect (NC).

Output Voltage Level

When the I/O port is programmed to be in one of the output modes, the output (high) voltage level can be programmed as TTL or CMOS.

Pin and Array side Trickle Current

P-channel devices are used as a trickle current source (nominally 10µA) on the pin side and array side for each I/O port. Upon reset, these current sources are turned ON. They can be turned OFF by properly programming the I/O buffers.

Pull–up Current

A normal pull–up current of 8 mA is supplied by an n– or p– channel device for TTL and CMOS outputs respectively. An **additional** pull–up current of 2.5 mA or 12.5 mA, supplied by p– channel devices, can be programmed at each I/O port. When the additional pull–up current is selected, the p–channel devices are always turned on, and therefore the output high is at the CMOS level. Figure 5 shows the output driver with the n– and p– channel pull–ups and the n–channel pull–down.
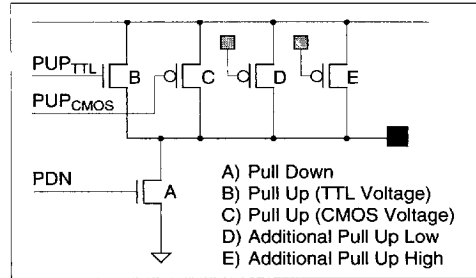
Figure 5: PS48 Output Driver

I/O Control Signals

The PS48 has a flexible control structure that gives the user complete control over the behavior of each I/O port. As shown in Figure 6 and described below, clock, clock enable, tristate and direction control for each I/O port can be programmed to use two control resources:
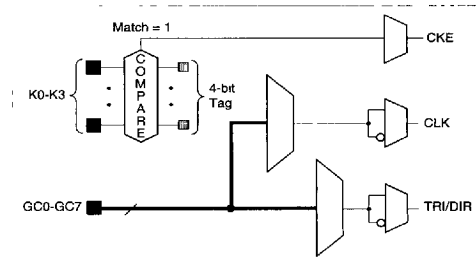
Figure 6: I/O Control

General Control

Eight general control pins, GC0–GC7, are used to carry control signals used for clock, tristate and direction control. Each I/O can be individually programmed to use these signals for control.

Key Control

Four Key control pins, K0–K3 are used to implement clock enable function. Each I/O buffer contains an 4–bit *tag* which can be programmed with a unique value. A comparator in each I/O port continually compares the assigned tag value with the signals present on the Key control pins. The output of the comparator, can be used as a clock enable.

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Configuration Controller

The PS48 is programmed using the JTAG (IEEE 1149.1) serial bus. The JTAG serial bus uses four pins: Test Data In (TDI), Test Data Out (TDO), Test Clock (TCK), and Test Mode Select (TMS). TCK is used to clock data in and out of TDI and TDO. TMS, in conjunction with TDI implements a state machine that controls the various operations of the JTAG protocol. In addition, the reset signal (TRST*) is used to reset the PS48.

The I/O attributes and switch matrix connections in the PS48 can be programmed using the JTAG serial bus. Additionally, RapidConnect interface, described in the next section, can be used for dynamic switching of connections through the switch matrix. This RapidConnect interface, is enabled or disabled using the JTAG serial bus. The RapidConnect interface cannot be used for programming the I/O attributes.

In most cases, the user does not need to know the details of the JTAG protocol. The I-Cube supplied software automatically generates the necessary bit stream from a higher–level textual description of the required configuration.

RapidConnect Interface

The RapidConnect interface is designed to quickly change connections. Using the RapidConnect interface, data is written directly to the SRAM cells controlling the connections in the switch matrix.

The RapidConnect interface, shown in Figure 7, is similar to the CPU–to–Memory interface. The RapidConnect interface is write-only. The SRAM contents cannot be read using this interface.
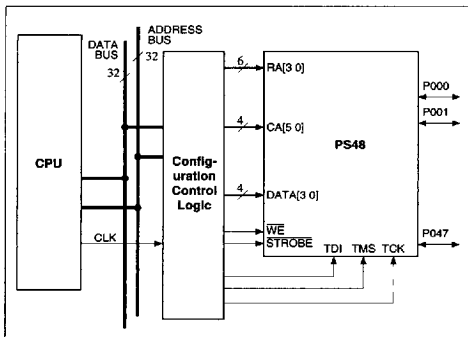

Figure 7: PS48 RapidConnect System Interface

The 16 pins used for the RapidConnect interface are divided into four groups – six Row Address pins RA[5:0], four Column Address pins CA[3:0], four data pins DATA[3:0], and two control pins – $\overline{WE}$ for Write Enable, and $\overline{STROBE}$ for the Write Strobe. In the RapidConnect mode, connections among forty eight 1–bit, twelve 4–bit, six 8–bit or 3 sixteen–bit port groups can be altered (made or broken) in one RapidConnect (write) cycle. The making or breaking of the connection takes place on the falling edge of $\overline{STROBE}$, assuming $\overline{WE}$ is active (low).

The values of Row Address, Column Address and DATA can be computed in real–time or could be pre-computed and stored as a look–up table in system memory.

The I/O port assignment for the 4–, 8– and 16–bit groups is shown in Table 2.

Word Number	Byte Number	Nibble Number	I/O Port Number
0	0	0	P000 – P003
		1	P004 – P007
	1	2	P008 – P011
		3	P012 – P015
1	2	4	P016 – P019
		5	P020 – P023
	3	6	P024 – P027
		7	P028 – P031
2	4	8	P032 – P035
		9	P036 – P039
	5	10	P040 – P043
		11	P044 – P047

Table 2: I/O Port Assignments for Group Switching Using RapidConnect

Upon power–up, the RapidConnect interface is OFF and must be enabled by sending the appropriate serial bit stream through the JTAG–based configuration controller.

The proper sequence of steps for using RapidConnect is as follows:

Following reset, the all the SRAM cells in the switch matrix are cleared and the I/O port attributes are properly programmed. If the RapidConnect interface is used for *bit–switching*, (switching individual I/Os) the second–level SRAM cells are programmed with a "1". If, on the other hand, the interface is used for *bus–switching*, (switching groups of I/O), the connections among individual signals or the bit order within the group, is established by properly programming the first–level SRAM cells. This is followed by downloading the bit stream that enables the RapidConnect mode.

Although it is not recommended, the user can use both RapidConnect and JTAG serial mode to change switch matrix connections. The RapidConnect mode *must* first be turned OFF – by sending the appropriate bit stream over the JTAG bus.

For a comprehensive description on RapidConnect for PS48, refer to the Technical Note, #D-31-012, *RapidConnect Interface for PS48*, or look up the *Programmable Switching and Interconnect Devices: Applications Handbook*.

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In-system Configuration

The primary configuration mode for the PS48 is the JTAG–based serial mode. The JTAG–based serial configuration mode allows the user to initialize the device, configure the I/Os and establish connections through the switch matrix. In addition, the RapidConnect interface can be used for changing switch matrix connections dynamically. Even if the user is planning to use RapidConnect for dynamic switching, the device must first be initialized using the JTAG-based configuration controller.

Configuring the device using JTAG involves two steps. In the first step, the user generates the bit stream, which, when loaded into the device, establishes the desired configuration. Two different software options – off-line and embedded bit stream generation – are available to accomplish this task depending on the target application. The second step is the actual downloading of the bit stream into the device. The downloading circuitry can take on different forms, depending on the target application.

Bit Stream Generation

The configuration bit stream generation can be done off–line or in real–time in the target system. Software available from I-Cube automates this process. See "I-Cube Development Systems and Software" section for more information.

The software used for off–line generation accepts a text file describing the desired configuration — connections between different I/O ports and functional attributes of each I/O port — and generates a file containing the bit stream. This software is a part of the development system. Figure 8 illustrates the steps involved in off–line bitstream generation.
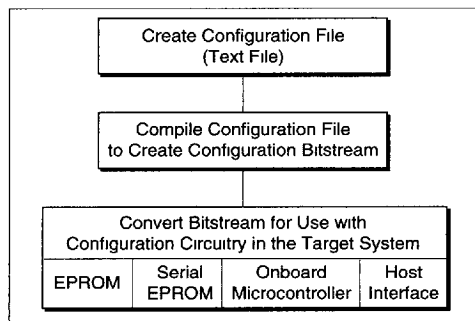
Figure 8: Off–line Bit Stream Generation

Another option shown in Figure 9, is to embed the bit stream generation software into the target system by using the I-Cube supplied "C" source code library.
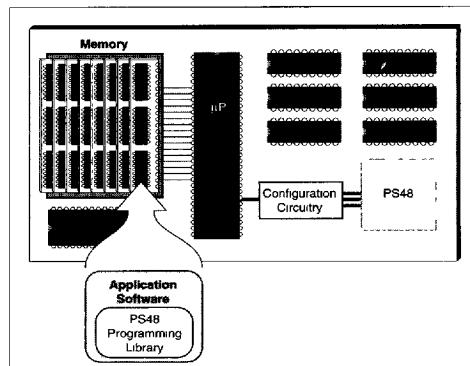
Figure 9: Embedded Bit Stream Generation

Bit Stream Downloading

The bit stream can be downloaded into the PS48 using several different hardware schemes. The choice depends on the end application. All these schemes use the standard JTAG protocol and timing. As per the JTAG protocol, the clock signal (TCK) must be supplied externally.

If the target hardware is controlled by a computer such as a PC, the parallel port on the computer can be used to download the bit stream. I-Cube provides a software utility to perform the downloading. Under this scheme, the necessary data for TDI and TMS pins as well as the (software generated) TCK clock signal are sent over the parallel port.

An on–board EPROM or E^2PROM, in either bit–wide or byte–wide configuration, or a serial EPROM can be used to store the bit stream. Using minimal external logic, the bit stream stored in one of these devices can be downloaded into the PS48 device(s) over the TDI and TMS pins, with the TCK pin used for synchronization. The clock signal for the TCK pin is generated by the external logic.

If the target system has an on–board microcontroller, the bit stream data can be read from memory (either an EPROM or SRAM) and downloaded into the PS48 device(s) using 3 I/O pins on the microcontroller to generate the required TDI, TMS and TCK signals. For real–

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time applications, the microcontroller/ microprocessor can generate the bit stream (using the I–Cube supplied software library for embedded applications) and then download it into the PS48 device in a single operation.

The actual time required to download the configuration bit stream and program a PS48 device depends on the user's specific configuration pattern, and JTAG clock frequency. In real–time, dynamic switching applications, the connections between the I/O pins can be done incrementally, that is, a single connection can be made or broken at a time.

The number of JTAG cycles and the downloading time for some typical configurations is shown in Table 3. Each PS48 requires a maximum of 4.5KB of memory to store the configuration bit stream.

Operation	Number of JTAG Cycles	Config. Time
Reset Device Using JTAG Reset Sequence	5	250 ns
Connect or Disconnect Two I/O Ports or Two 4–, 8– or 16–bit Groups	102	5 10 µs
Change I/O Attributes of One Port	61	3.05 µs
Change I/O Attributes of All Ports	4636	231 8 µs
Enable or Disable RapidConnect	42	2.10 µs
Set All I/O Ports to Default Attributes	27	1.35 µs
Clear All Connections (Clear All Switch Matrix SRAM cells)	689	34 45 µs
Completely Configure the Device (All I/O Attributes + All Connections)	≈ 18,000	≈ 900 µs

Table 3: Configuration Times

Configuring Multiple Devices

The JTAG–based configuration controller allows a single device, or multiple PS48 devices connected in a chain, to be configured in a single operation. For multiple device configuration, the TDI and TDO pins of the adjacent devices are connected, except for the very first and last device. The TMS pins of all devices are connected to the same external signal. The TCK and TRST* (if used) pins on PS48 device(s) are connected in a similar manner. This is shown in Figure 10.
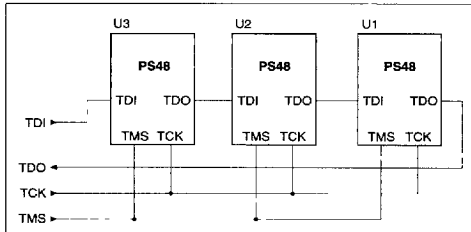

Figure 10: Configuring Multiple Devices

During the initial configuration sequence, the controllers on all PS48 devices are first brought to their default state by either using the TRST* reset pin or by applying the JTAG reset sequence ("11111") on the TMS pin. This is followed by the downloading of the actual configuration bit stream over the TDI and TMS pins.

I-Cube Development Systems and Software

I-Cube offers several different Development System options for designing with the PS48. The IDS Development System accepts a text file describing PS48 device configuration pattern – interconnections and desired I/O port functions – and compiles it to generate the bit stream for downloading into the targeted PS48 device(s). The process is fully automatic and extremely fast. The I-Cube Development System support designs using single or multiple PS48 devices. Off–line and in–system (embedded) options are supported.

A brief description of the Development Systems follows:

IDS100 - PC–based Development System

This IBM–PC and compatible Development System allows complete, off–line bit stream generation on a PC based platform. This development system is particularly useful for users who wish to generate bit streams off–line and store them in firmware in their targeted system. The IDS100 Development System automatically generates a bit stream file from the user supplied configuration file. The IDS100 can also be used to download the bit stream from a PC parallel port.

IDS200 - Sparcstation– based Development System

The Sparcstation–based Development System allows complete off–line bit stream generation on a workstation. The IDS200 Development System includes a module to allow downloading from the parallel port on a PC, if desired.

IDS500 - Programming Library

The IDS500 Development System option is useful for users who wish to reconfigure PS48 devices with a large number of bit stream patterns. This system is also useful where the PS48 configuration pattern is not known, and the bit stream is required to be dynamically generated in the target system. The IDS500 Development System is an unlimited, royalty–free source code license, allowing users to incorporate the desired software routines into their target system.

The IDS500 Development System contains a library of routines in source code form (written in "C") for use in embedded applications. Users have the ability to customize the libraries to meet their application and system memory requirements. The IDS500 library can be compiled and linked to other system application software running on a microcontroller or microprocessor in the target system, as shown in Figure 9.

PS48SK - Starter Kit

In addition to the Development Systems, I-Cube offers a PS48 Starter Kit, complete with a PS48 device, configuration hardware and software, to facilitate the development of the target application. The PS48 mounted on a small board with stake pins can be easily connected to the target system and the PC/Windows based software, included with the kit, can be used to generate the configuration bit stream and configure the PS48 device.

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PS48 Pin Summary

Pin Name	Description
P000 – P047	**Signal I/O Ports** I/O Ports, addressable individually or as Nibbles [N000 – N011], Bytes [B000 – B005] and Words [W000 – W002]
GC0 – GC7	**General Purpose Control Ports** General Purpose Control Signals Used for Clock, Tristate and Direction Control
K0 – K3	**Key Port** Key Signals Used for Clock Enabling
RA[5:0] CA[3:0] DATA[3:0] $\overline{WE}$ $\overline{STROBE}$	**RapidConnect Control Ports** RapidConnect Row Address RapidConnect Column Address RapidConnect Data RapidConnect Write Enable RapidConnect Write Strobe
TDI, TMS, TCK, TDO, TRST*	**JTAG Pins** Used for downloading configuration bitstream in a serial fashion To ensure proper power-on reset, connect 10K resistor between TRST* and V_{cc} and 0.1µF capacitor between TRST* and V_{ss}.
V_{DD}.PAD V_{DD} V_{SS}.PAD V_{SS}	**Power and Ground Pins** Power Pins for I/O Buffer Drivers Only Power Pins for on–chip circuitry other than I/O Buffer Drivers Ground Pins for I/O Buffer Drivers Only. Ground Pins for on–chip circuitry other than I/O Buffer Drivers

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Electrical Specifications

Absolute Maximum Rating [1]

Symbol	Parameter	Limits	Units
V_{DD}	Supply Voltage to Ground	-0.3 to +7.0	V
V_{IN}	Input Voltage [2]	-0.3 to V_{DD}+0.3	V
T_J	Junction Temperature	150	°C
T_{STG}	Storage Temperature	-65 to +150	°C
I_{SINK}	Sink Current per Port Pin	150	mA

Recommended Operating Conditions

Symbol	Parameter	Limits	Units
V_{DD}	Supply Voltage to Ground	+4.75 to +5.25	V
T_A	Operating Temperature	0 to +70	°C

Capacitance [3]

Symbol	Parameter	Max	Units
C_{IN}	Input Capacitance (JTAG pins)	8	pF
C_{OUT}	Output Capacitance (TDO pin)	5	pF
C_{PORT}	I/O Signal Port, Key Port and RapidConnect Pin Capacitance	10	pF
C_{PORT}	Non-Buffered (NB) Signal Port Input Capacitance with One Connection [4]	16	pF
$C_{GC0-GC7}$	General Control Port (GC0-GC7) Capacitance	See Note [5]	pF

NOTES:

(1) Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

(2) A maximum overshoot and undershoot of 2V for a maximum duration of 20 ns is acceptable.

(3) Capacitance measured at 25°C. Sample-tested only.

(4) The input capacitance of an NB port depends on how many ports it is connected to. Each additional connection will add 3.7 pF to the input capacitance. For example, a one-to-eight connection will then have an input capacitance of 45 pF.

(5) The general control port capacitance depends on how many I/O ports use that general control port for its clock tristate or direction control. The capacitance is 22 pF if the general control port is not used by any I/O ports for clock tristate or direction control. Each I/O port using the general control for its clock, tristate or direction control will increase the capacitance by 0.24 pF. The capacitance is 45 pF if the general control port is used as clock, tristate or direction control for the 48 I/Os.

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DC Electrical Specifications ($T_A = 0°C$ to $70°C$, $V_{DD} = 5V \pm 5\%$)

Symbol	Parameter	Condition	Min	Max	Units
V_{IH}	High-Level Input Voltage		2.0	V_{DD}+0.3	V
V_{IL}	Low-Level Input Voltage		- 0.3	0.8	V
V_{OH}	High-Level Output Voltage [1]	V_{DD} = Min, I_{OH} = - 8 mA	2.4	-	V
V_{OL}	Low-Level Output Voltage	V_{DD} = Min, I_{OL} = 16 mA	-	0.4	V
$|I_{IL}|$ $|I_{IH}|$	Input Leakage Current [2] (For all I/O Ports & JTAG pins)	V_{DD} = Max, $0 \leq V_{IN} \leq V_{DD}$	-	5	μA
I_{PT}	I/O Port Trickling Current [2]	V_{DD} = Max, $0 \leq V_{IN} \leq V_{DD}$	-	-25	μA
$|I_{OZ}|$	Tristate Output Off-State Current [2]	V_{DD} = Max, $0 \leq V_{IN} \leq V_{DD}$	-	5	μA
I_{PU-LO}	Programmed-Low Additional Pull Up Current	V_{DD} = Min, V_O = GND	2.0	4.0	mA
I_{PU-HI}	Programmed-High Additional Pull Up Current	V_{DD} = Min, V_O = GND	11	13.5	mA
I_{OS}	Short Circuit Current [1, 3, 4]	V_{DD} = Max, V_O = GND	-60	-	mA
I_{DDQ}	Quiescent Power Supply Current	V_{DD} = Max, Freq = 0 MHz, No Load, $0 \leq V_{IN} \leq V_{DD}$	-	2.0	mA
Q_{DDD}	Dynamic Power Supply Current per Input per MHz [3]	V_{DD} = Max, No Load, Connect one output per input, Toggle one input @ 50% duty cycle with all other inputs at GND or V_{DD}	-	0.1	mA/ MHz

NOTES:
(1)   For TTL output mode.
(2)   There is a Trickling Current Source associated with each I/O port and it can be programed to be on or off. The Trickling Current Source should be turned on during I/O Ports Trickling Current measurements and it should be off during all other DC measurements.
(3)   These parameters are guaranteed but not tested in production.
(4)   No more than one output should be tested at a time, and the duration of the test should be less than one second.

AC Electrical Specifications ($T_A = 0°C$ to $70°C$, $V_{DD} = 5V \pm 5\%$)

(Assume two ports connected through the crossbar array and output levels are TTL with 50pF loading.)

Symbol	Parameter	-100 Min	-100 Max	-80 Min	-80 Max	-66 Min	-66 Max	-50 Min	-50 Max	Units	Ref. Timing Diagram
f_{RIO}	Register Input/Output Clock Frequency [1]	-	100	-	80	-	66	-	50	MHz	
t_{W-RIO}	Register Input/Output Clock Pulse Width, Low or High	5	-	6	-	7	-	9	-	ns	
t_{S-RIO}	Register Input/Output Setup Time	2	-	2	-	2	-	2	-	ns	2
t_{H-RIO}	Register Input/Output Hold Time	0	-	0	-	0	-	0	-	ns	
t_{P-RIO}	Register Input/Output Clock to Data Valid	-	7	-	9	-	12	-	15	ns	
f_{RI}	Register Input Clock Frequency [1]	-	100	-	80	-	66	-	50	MHz	
t_{W-RI}	Register Input Clock Pulse Width, Low or High	5	-	6	-	7	-	9	-	ns	
t_{S-RI}	Register Input Setup Time	2	-	2	-	2	-	2	-	ns	3
t_{H-RI}	Register Input Hold Time	0	-	0	-	0	-	0	-	ns	
t_{P-RI}	Register Input Clock to Data Valid	-	16	-	18	-	22	-	25	ns	
f_{RO}	Register Output Clock Frequency [1]	-	100	-	80	-	66	-	50	MHz	
t_{W-RO}	Register Output Clock Pulse Width, Low or High	5	-	6	-	7	-	9	-	ns	
t_{S-RO}	Register Output Setup Time	7	-	8	-	9	-	10	-	ns	4
t_{H-RO}	Register Output Hold Time	0	-	0	-	0	-	0	-	ns	
t_{P-RO}	Register Output Clock to Output Data Valid	-	7	-	9	-	12	-	15	ns	
t_{PLH}, t_{PHL}	One Way Signal Propagation Delay Time (NB to OP)	-	10	-	12.5	-	15	-	20	ns	5a
t_{PLH}, t_{PHL}	One Way Signal Propagation Delay Time (IN to OP)	-	12.5	-	15	-	17.5	-	22.5	ns	
t_{PD}	Additional Delay per Additional Output Port up to 16 Output Ports [1]	-	0.5	-	0.5	-	0.5	-	0.5	ns	
t_{SK}	Skew Between Output Ports [1]	-	1.5	-	1.5	-	1.5	-	1.5	ns	5b
R_{DATA}	NRZ Data Rate (IN to OP) [1]	-	160	-	133	-	120	-	80	Mbs	
t_{W+}	Positive Input signal Pulse Width (IN to OP)	6	-	7	-	9	-	11	-	ns	
t_{W-}	Negative Input signal Pulse Width (IN to OP)	6.5	-	8	-	11	-	13	-	ns	
t_{PZL-OT} t_{PZH-OT}	Output Enable to Output Data Valid Time	-	10	-	12.5	-	15	-	20	ns	
t_{PLZ-OT} t_{PHZ-OT}	Output Disable to Output at High-Z Time [1]	-	10	-	12.5	-	15	-	20	ns	
t_{PZL-IT} t_{PZH-IT}	Input Enable to Array-side Data Valid Time [1]	-	8	-	10	-	12.5	-	15	ns	
t_{PLZ-IT} t_{PHZ-IT}	Input Pin-side Disable to Array-side at High Z Time [1]	-	8	-	10	-	12.5	-	15	ns	6
t_{PZL-BT} t_{PZH-BT}	DIR Enable to Output Data Valid Time	-	10	-	12.5	-	15	-	20	ns	
t_{PLZ-BT} t_{PHZ-BT}	DIR Disable to Output at High-Z Time [1]	-	10	-	12.5	-	15	-	20	ns	
t_{W-IL}	Input Latch Enable Pulse Width	5	-	6	-	7	-	9	-	ns	
t_{S-IL}	Input Latch to Enable Trailing Edge Setup Time	4	-	4	-	4	-	4	-	ns	
t_{H-IL}	Input Latch to Enable Trailing Edge Hold Time	0	-	0	-	0	-	0	-	ns	7
t_{P-IL}	Input Latch Leading Edge to Data Out	-	16	-	18	-	22	-	25	ns	
t_{P-ILT}	Transparent Mode Propogation Delay	-	12.5	-	15	-	17.5	-	22.5	ns	
t_{W-OL}	Output Latch Enable Pulse Width	5	-	6	-	7	-	9	-	ns	
t_{S-OL}	Output Latch to Enable Trailing Edge Setup Time	4	-	4	-	4	-	4	-	ns	
t_{H-OL}	Output Latch to Enable Trailing Edge Hold Time	0	-	0	-	0	-	0	-	ns	8
t_{P-OL}	Output Latch Leading Edge to Data Out	-	10	-	12.5	-	15	-	20	ns	
t_{P-OLT}	Transparent Mode Propogation Delay	-	12.5	-	15	-	17.5	-	22.5	ns	

NOTES:

(1) These parameters are guaranteed but not tested in production.

The timing specification for control signals CLK, CKE, TRI/DIR is with respect to the external pins used to carry these signals, i.e., General Control ports (GC) for CLK and TRI/DIR, and Key ports (KEY) for CKE. Associated timing diagrams show both the external signals and corresponding internal control signals in parenthesis.

AC Electrical Specifications (Continued)

Symbol	Parameter	Speed Grade -100 Min	Max	-80 Min	Max	-66 Min	Max	-50 Min	Max	Units	Ref. Timing Diagram
t$_{KW-RI}$	Valid Key Pulse Width for Input Clock Enabling [1]	8	-	8	-	8	-	8	-	ns	
t$_{KS-RI}$	Key Setup Time for Input Clock Enabling [1]	8	-	8	-	8	-	8	-	ns	9
t$_{KH-RI}$	Key Hold Time for Input Clock Enabling [1]	0	-	0	-	0	-	0	-	ns	
t$_{KW-RO}$	Valid Key Pulse Width for Output Clock Enabling [1]	8	-	8	-	8	-	8	-	ns	
t$_{KS-RO}$	Key Setup Time for Output Clock Enabling [1]	8	-	8	-	8	-	8	-	ns	10
t$_{KH-RO}$	Key Hold Time for Output Clock Enabling [1]	0	-	0	-	0	-	0	-	ns	
t$_{KW-IL}$	Valid Key Pulse Width when Input Latch Enabled [1]	10	-	11	-	12	-	13	-	ns	
t$_{KS-IL}$	Key Setup Time to Trailing Edge of Latch Enable [1]	0	-	0	-	0	-	0	-	ns	
t$_{KH-IL}$	Key Hold Time to Trailing Edge of Latch Enable [1]	1	-	1	-	1	-	1	-	ns	11
t$_{KP-IL}$	Valid Key to Data Out When Input Latch Enabled [1]	-	16	-	18	-	22	-	25	ns	
t$_{KP-ILT}$	Transparent Mode Propogation Delay [1]	-	12.5	-	15	-	17.5	-	22.5	ns	
t$_{KW-OL}$	Valid Key Pulse Width when Output Latch Enabled [1]	7	-	8	-	9	-	10	-	ns	
t$_{KS-OL}$	Key Setup Time to Trailing Edge of Latch Enable [1]	1	-	1	-	1	-	1	-	ns	
t$_{KH-OL}$	Key Hold Time to Trailing Edge of Latch Enable [1]	0	-	0	-	0	-	0	-	ns	12
t$_{KP-OL}$	Valid Key to Data Out When Output Latch Enabled [1]	-	10	-	12.5	-	15	-	20	ns	
t$_{KP-OLT}$	Transparent Mode Propogation Delay	-	12.5	-	15	-	17.5	-	22.5	ns	
T$_{RC}$	RapidConnect Strobe Period	20	-	20	-	20	-	20	-	ns	
t$_{RCW+}$	RapidConnect Strobe Pulse Width High	8	-	8	-	8	-	8	-	ns	
t$_{RCW-}$	RapidConnect Strobe Pulse Width Low	6	-	6	-	6	-	6	-	ns	
t$_{S-RC}$	RapidConnect Address and Data Set up Time	4	-	4	-	4	-	4	-	ns	13
t$_{H-RC}$	RapidConnect Address and Data Hold Time	4	-	4	-	4	-	4	-	ns	
t$_{P-RC}$	RapidConnect Strobe Falling Edge to Data Valid for Making Connection	20	-	20	-	20	-	20	-	ns	
f$_{JTAG}$	JTAG Clock (TCK) Frequency	-	20	-	20	-	20	-	20	MHz	
t$_{W-JTAG}$	JTAG Clock (TCK) Pulse Width, Low or High	25	-	25	-	25	-	25	-	ns	
t$_{S-JTAG}$	JTAG Setup Time	15	-	15	-	15	-	15	-	ns	14
t$_{H-JTAG}$	JTAG Hold Time	15	-	15	-	15	-	15	-	ns	
t$_{P-JTAG}$	JTAG Clock to Output Valid	15	-	15	-	15	-	15	-	ns	

Note:
(1) These parameters are guaranteed but not tested in production.
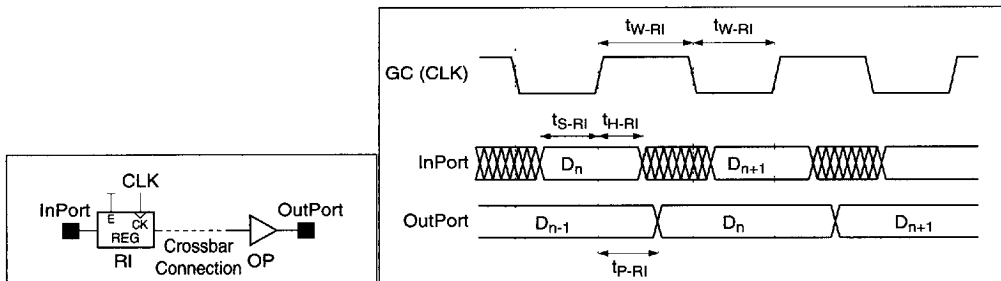
9004188 0000225 511
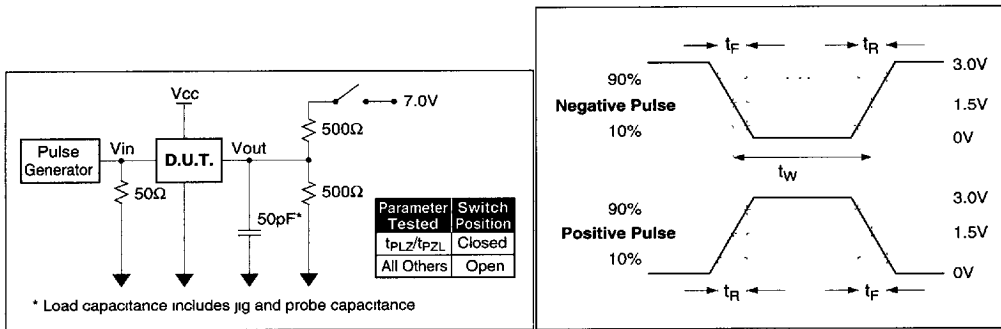
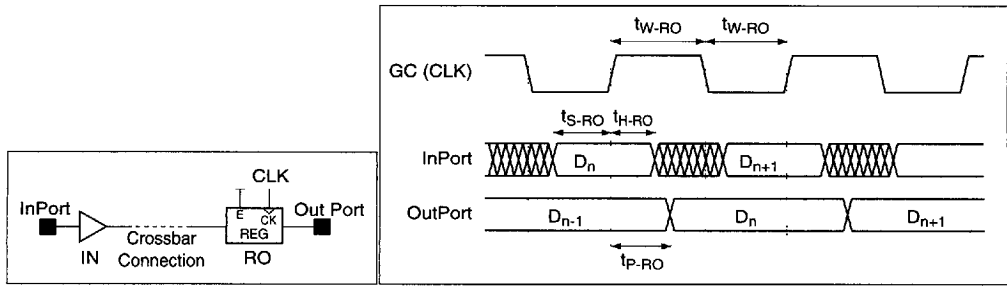## Timing Diagrams

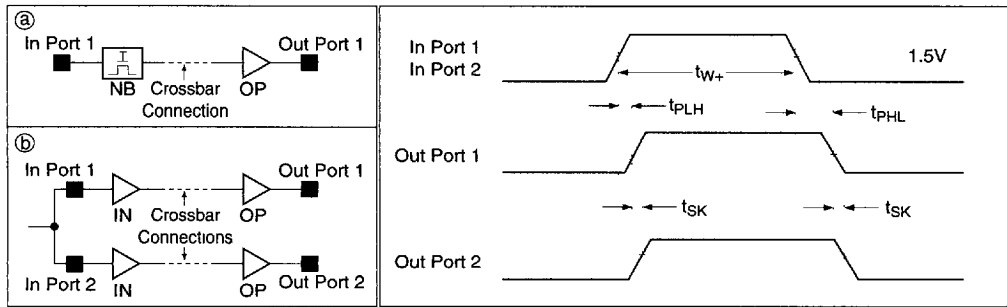**Timing Diagram 1: Test Circuit and Waveform Definition**
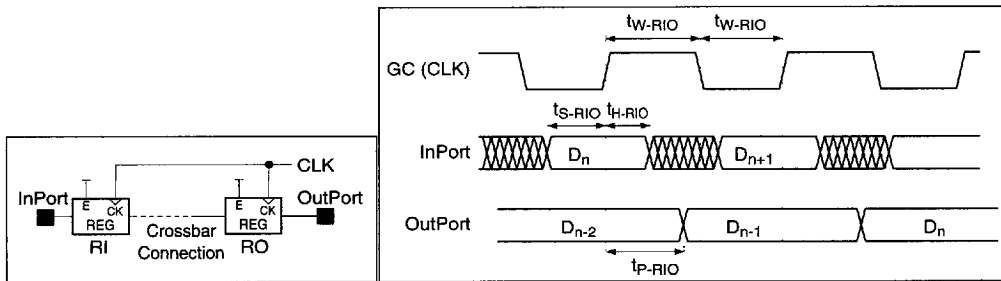
Timing Diagram 2: Registered Input and Registered Output Mode Timing
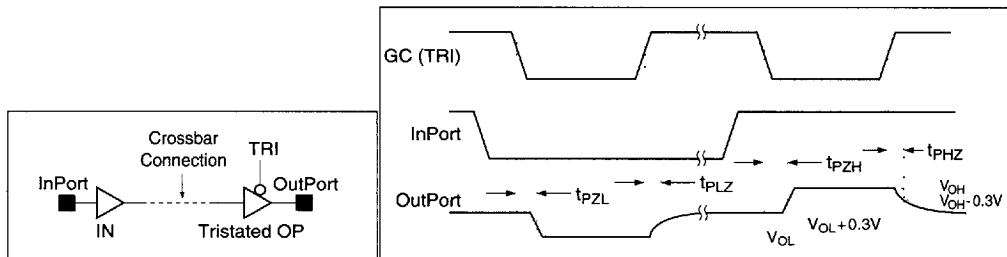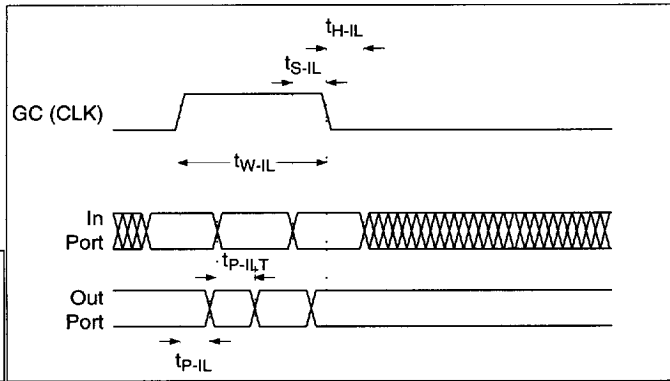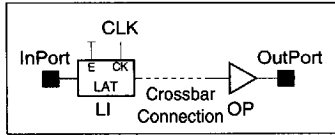

Timing Diagram 3: Registered Input Mode

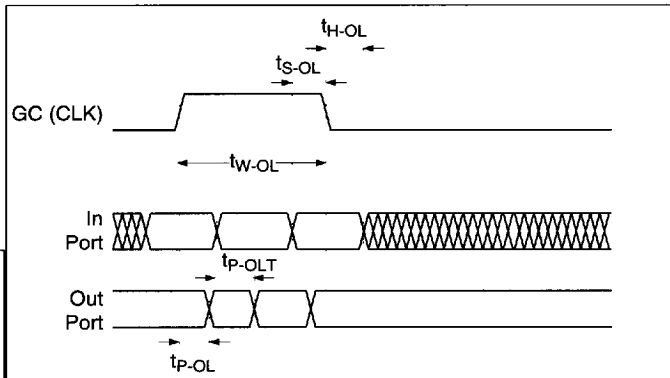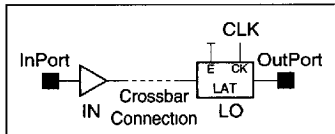**Timing Diagram 4: Registered Output Mode**

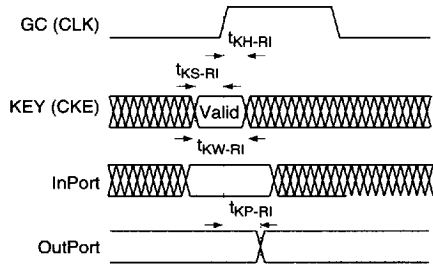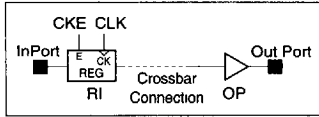**Timing Diagram 5: Pin–to–pin Delay (Flow–through Mode)**
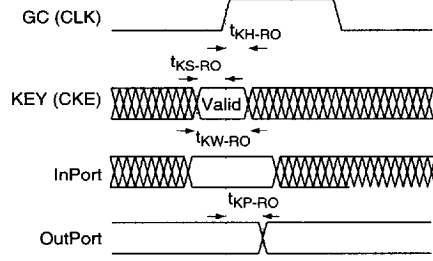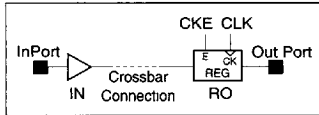

Timing Diagram 6: Tristate (Flow–through Mode)

Timing Diagram 7: Latched Input Mode
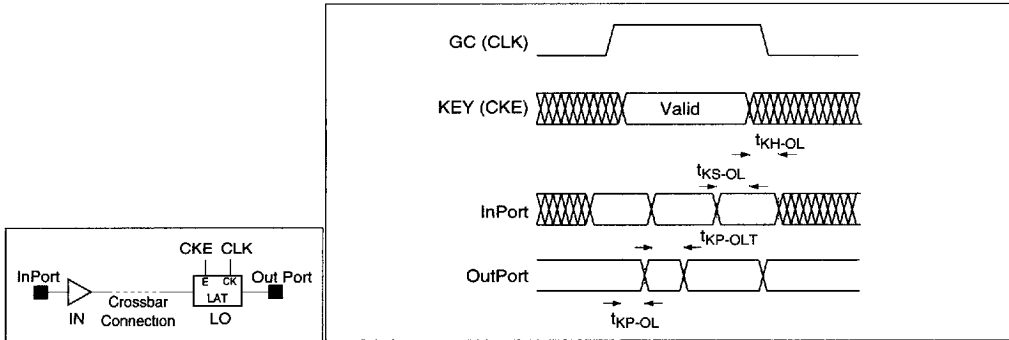

Timing Diagram 8: Latched Output Mode

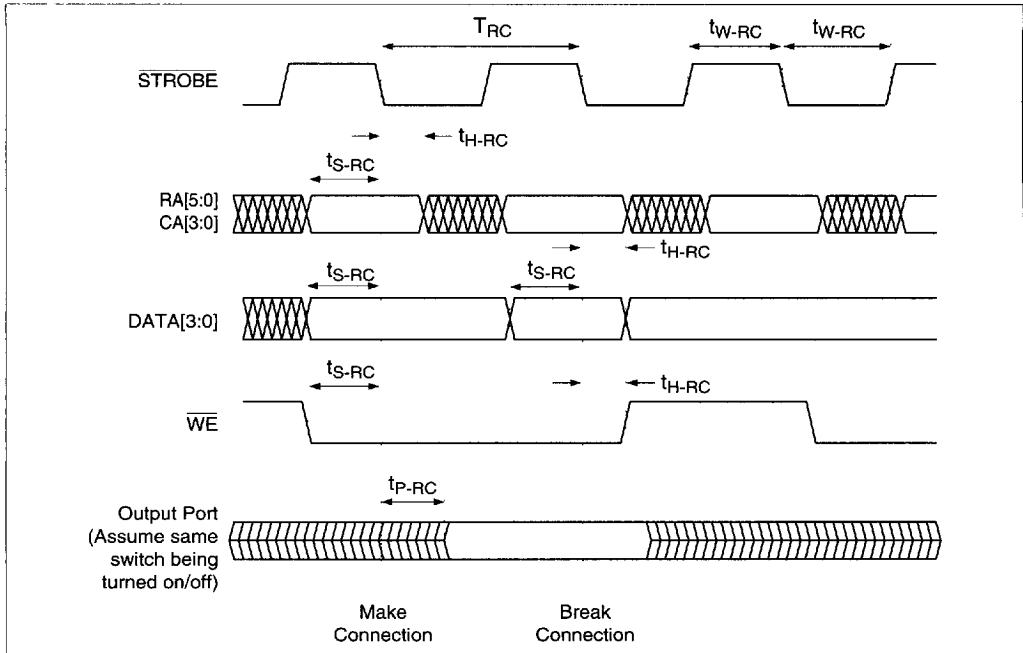**Timing Diagram 9: Key Control (Clock Enable) for Registered Input**

Timing Diagram 10: Key Control (Clock Enable) for Registered Output
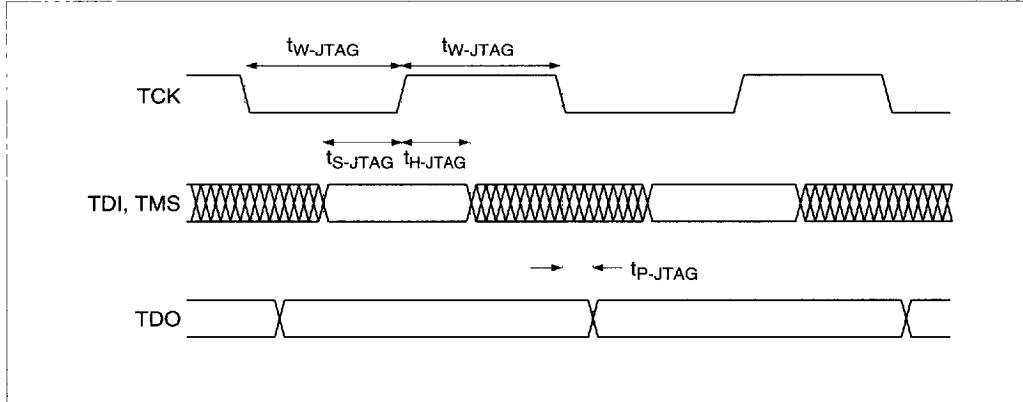
9004188 0000229 167
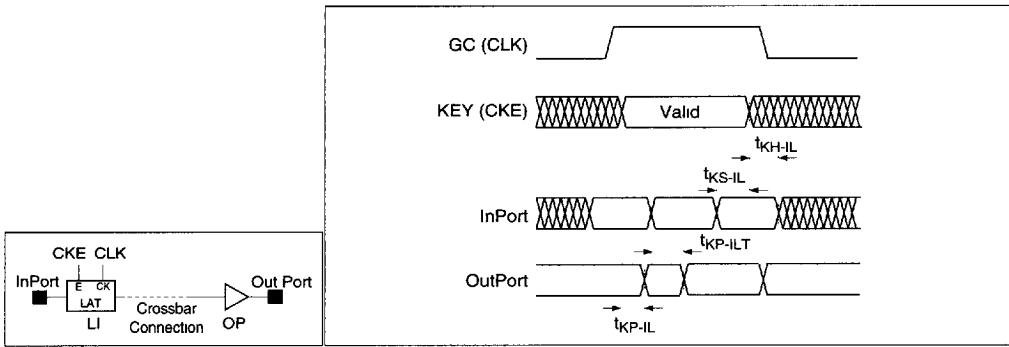
Timing Diagram 11: Key Control (Clock Enable) for Latched Input

Timing Diagram 12: Key Control (Clock Enable) for Latched Output

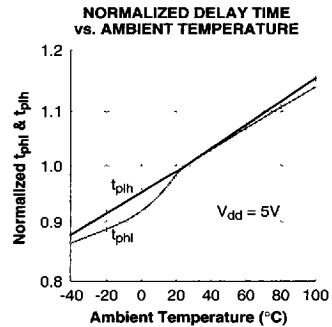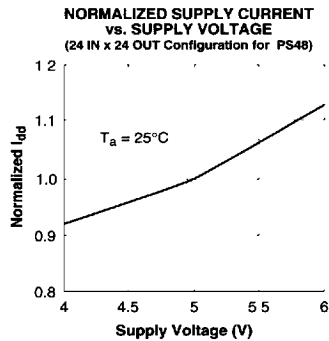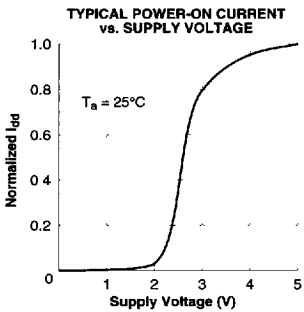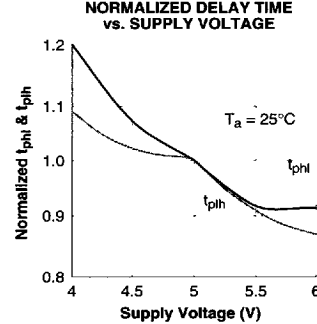**Timing Diagram 13: RapidConnect Interface**

Timing Diagram 14: JTAG Interface

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Typical AC and DC Characteristics

OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE (CMOS Output Mode)

$V_{dd} = 5V$
$T_a = 25°C$

Output Source Current (mA) vs. Output Voltage (V)

OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE (TTL Output Mode)

$V_{dd} = 5V$
$T_a = 25°C$

Output Source Current (mA) vs. Output Voltage (V)

OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE

$V_{dd} = 5V$
$T_a = 25°C$

Output Sink Current (mA) vs. Output Voltage (V)

TYPICAL DELAY TIME vs. OUTPUT LOADING

$V_{dd} = 5V$
$T_a = 25°C$

t_{plh}
t_{phl}

Delta t_{phl} & t_{plh} (ns) vs. Capacitance (pF)

TYPICAL DELAY TIME vs. OUTPUT LOADING

t_{plh}
t_{phl}

$V_{dd} = 5V$
$T_a = 25°C$

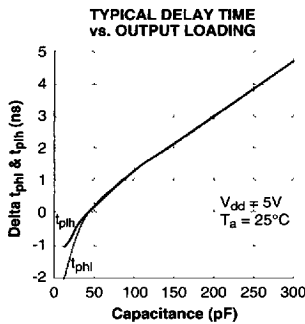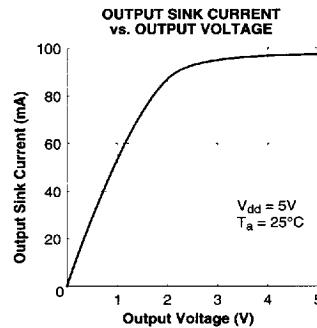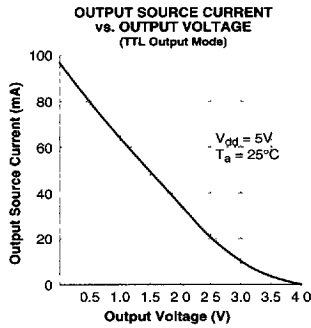Delta t_{phl} & t_{plh} (ns) vs. Capacitance (pF)

NORMALIZED DELAY TIME vs. SUPPLY VOLTAGE

$T_a = 25°C$

t_{plh}
t_{phl}

Normalized t_{phl} & t_{plh} vs. Supply Voltage (V)

TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE

$T_a = 25°C$

Normalized I_{dd} vs. Supply Voltage (V)

NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE (24 IN x 24 OUT Configuration for PS48)

$T_a = 25°C$

Normalized I_{dd} vs. Supply Voltage (V)

NORMALIZED DELAY TIME vs. AMBIENT TEMPERATURE

t_{plh}
t_{phl}

$V_{dd} = 5V$

Normalized t_{phl} & t_{plh} vs. Ambient Temperature (°C)

Mechanical Specification

Package Dimensions

Figure 11: PQFP/100L Package Dimensions

Figure 12: MQUAD/100L Package Dimensions
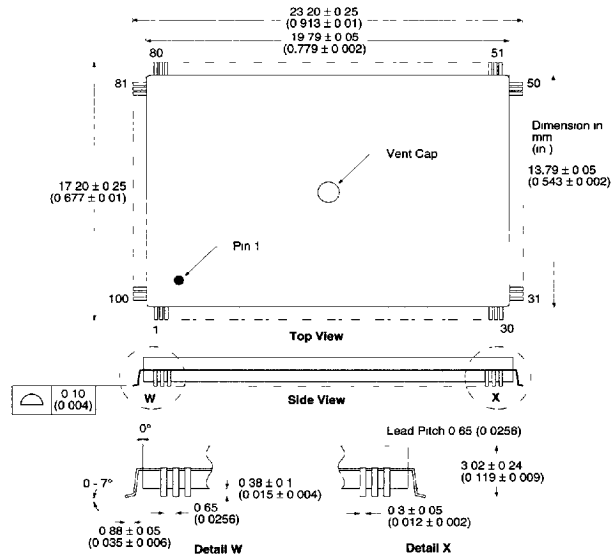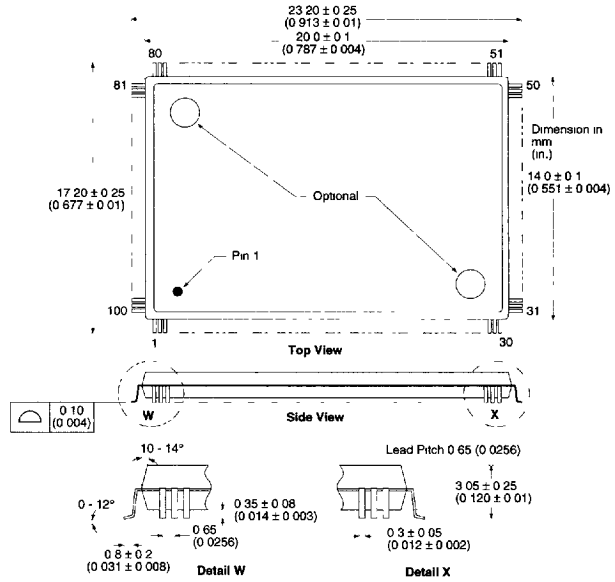
Figure 13: TQFP/100L Package Dimensions

Pinout

PS48 [TQFP/100L Package] Pinout

PS48 [PQFP/100L, MQUAD/100L Package] Pinout

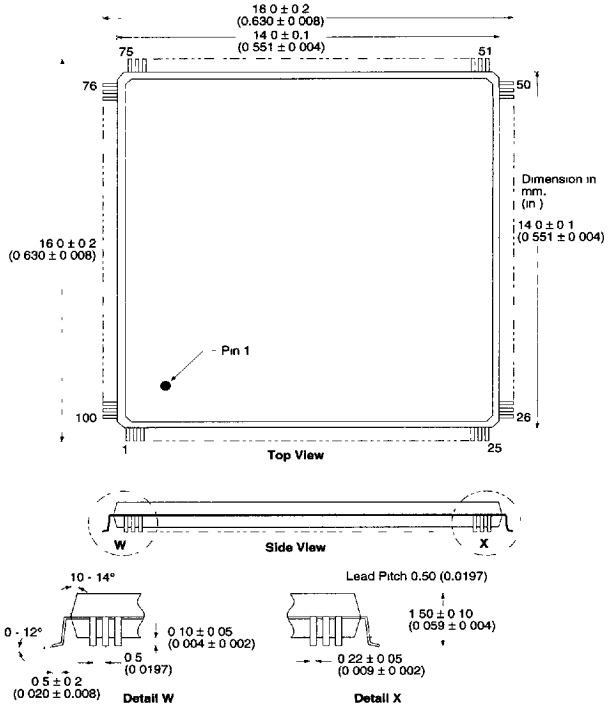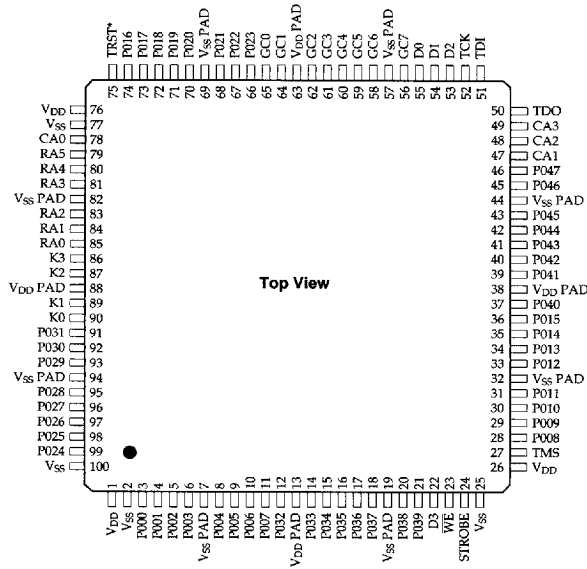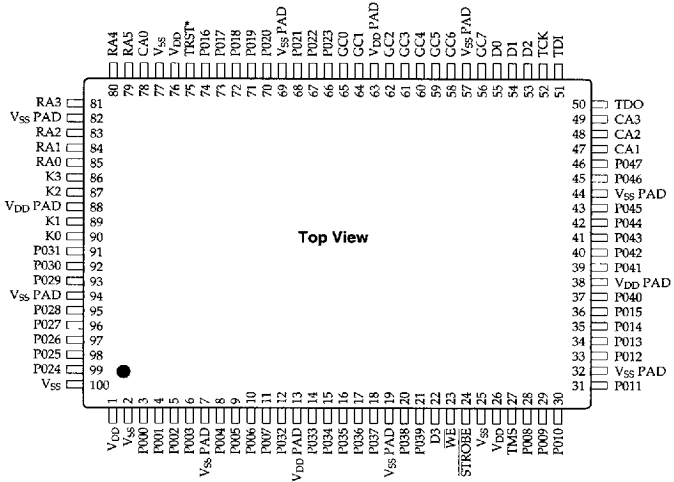**Figure 14: TQFP/PQFP/MQUAD Package Pinout**

PS48 Pinout Table

Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name
1	V_{DD}	26	V_{DD}	51	TDI	76	V_{DD}
2	V_{SS}	27	TMS	52	TCK	77	V_{SS}
3	P000	28	P008	53	D2	78	CA0
4	P001	29	P009	54	D1	79	RA5
5	P002	30	P010	55	D0	80	RA4
6	P003	31	P011	56	GC7	81	RA3
7	V_{SS}.PAD	32	V_{SS}.PAD	57	V_{SS}.PAD	82	V_{SS}.PAD
8	P004	33	P012	58	GC6	83	RA2
9	P005	34	P013	59	GC5	84	RA1
10	P006	35	P014	60	GC4	85	RA0
11	P007	36	P015	61	GC3	86	K3
12	P032	37	P040	62	GC2	87	K2
13	V_{DD}.PAD	38	V_{DD}.PAD	63	V_{DD}.PAD	88	V_{DD}.PAD
14	P033	39	P041	64	GC1	89	K1
15	P034	40	P042	65	GC0	90	K0
16	P035	41	P043	66	P023	91	P031
17	P036	42	P044	67	P022	92	P030
18	P037	43	P045	68	P021	93	P029
19	V_{SS}.PAD	44	V_{SS}.PAD	69	V_{SS}.PAD	94	V_{SS}.PAD
20	P038	45	P046	70	P020	95	P028
21	P039	46	P047	71	P019	96	P027
22	D3	47	CA1	72	P018	97	P026
23	$\overline{WE}$	48	CA2	73	P017	98	P025
24	$\overline{STROBE}$	49	CA3	74	P016	99	P024
25	V_{SS}	50	TDO	75	TRST*	100	V_{SS}

Table 4: PS48 Pinout Table [TQFP/PQFP/MQUAD Packages]

9004188 0000236 3T7

Component Availability and Ordering Information

The following table lists the different package options, speed grades and operating temperature ranges that are currently available for the PS48. Contact I-Cube Marketing for more up-to-date information on product availability.

Device	Package	Package Code	Speed			
			-100	-80	-66	-50
PS48	PQFP/100L	PQ	C	C	C	C
	TQFP/100L	TQ	C	C	C	C
	MQUAD/100L	MQ	C	C	C	C

Table 5: Component Availability

$$\textbf{PS 48-SS PP \#\#\# T}$$

Number of Usable I/O Ports

Speed Grade

Package Code
PQ - Plastic Quad Flat Pack
MQ - MQUAD®
TQ - Thin Quad Flat Pack

Package Pin Count

Temperature Range
Blank - Commercial (0°C to 70°C)
I   - Industrial (-40°C to 85°C)

9004188 0000237 233