PC Clock Generator

Features

- Generates up to 16 preset frequencies, 4 peripheral clocks, and buffers input reference frequency
- Power down, slow down, or stop clock feature supporting "Green PC" applications
- Smooth glitch-free frequency transitions
- Requires three external components: one 14.318 MHz crystal and two 0.1 µF decoupling capacitors
- On-chip loop filters for clock generators
- Supports x86-based designs
- Drop-in replacement for AV9154
- CMOS technology in 16-pin PDIP (300 mil) and SOIC (150 mil)
- 5V or 3.3V supply

Description

CH9054 is a dual PLL clock generator designed for personal computer motherboard applications. CH9054 buffers the reference frequency, provides 16 preset CPU/ 2XCPU clocks and up to four peripheral clocks. CPU and 2XCPU frequencies can be selected with frequency select inputs, FS[3:0]. These frequencies support the new generation of CPU upgradable motherboards. CPU clocks for x86 and Pentium™ are selected by externally setting select pins to VDD or GND.

CH9054 is available with Output Enable (OE), Power Down (PD*), Slow Down (SD*) or Stop Clock (CLKEN) options, which are ideal for low power "Green PC" applications.

Power down is enabled by setting the PD* pin to ground. While power down is active, the internal PLLs and crystal oscillator are disabled to minimize current consumption (less than 10 µA).

Setting the SD* pin to ground enables slow down, which gradually slows the CPU and 2XCPU outputs to 16 MHz, 8 MHz, or 4 MHz.

The clock enable (CLKEN) option supports x86-based systems with stop clock features. When CLKEN is pulled low, CPU and 2XCPU outputs are disabled and held at a low state.

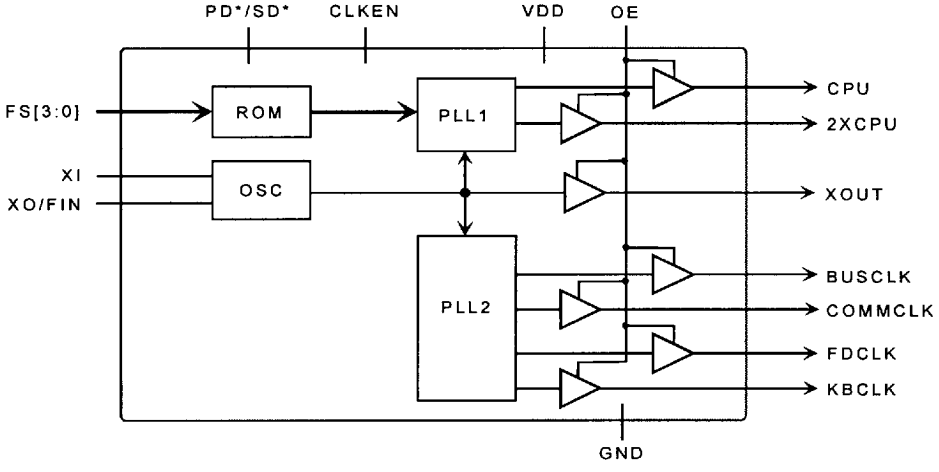

Figure 1: Block Diagram

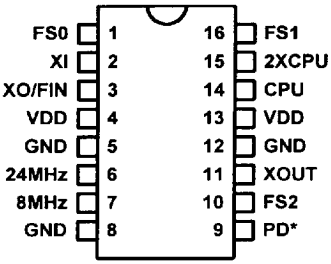

Figure 2: CH9054A

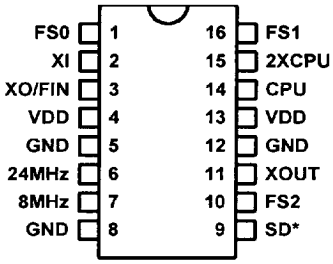

Figure 3: CH9054B

Table 1 • Pin Description CH9054A

Pin	Type	Symbol	Description
1, 10, 16	In	FS0, FS2, FS1	Clock select inputs (internal pull-up)
2	In	XI	Crystal input
3	Out / In	XO / FIN	Crystal output or external FREF input
4, 13	Power	VDD	5V or 3.3V supply
5, 8, 12	Power	GND	Ground
6	Out	24 MHz	24 MHz floppy disk clock output
7	Out	8 MHz	8 MHz keyboard clock output
9	In	PD*	Power down input (active low, internal pull-up)
11	Out	XOUT	Buffered reference (14.318 MHz) clock output
14	Out	CPU	CPU clock output
15	Out	2XCPU	2XCPU clock output

Table 2 • Pin Description CH9054B

Pin	Type	Symbol	Description
1, 10, 16	In	FS0, FS2, FS1	Clock select inputs (internal pull-up)
2	In	XI	Crystal input
3	Out / In	XO / FIN	Crystal output or external FREF input
4, 13	Power	VDD	5V or 3.3V supply
5, 8, 12	Power	GND	Ground
6	Out	24 MHz	24 MHz floppy disk clock output
7	Out	8 MHz	8 MHz keyboard clock output
9	In	SD*	Slow down input (active low, internal pull-up)
11	Out	XOUT	Buffered reference (14.318 MHz) clock output
14	Out	CPU	CPU clock output
15	Out	2XCPU	2XCPU clock output

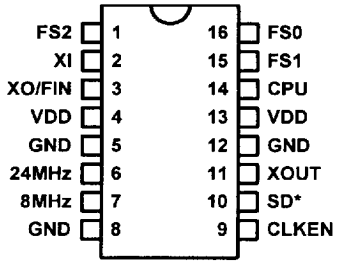

Figure 4: CH9054C

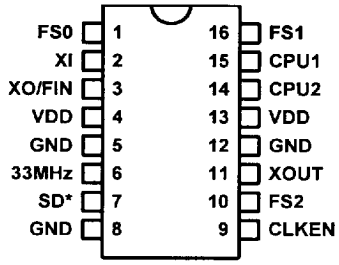

Figure 5: CH9054D

Table 3 • Pin Description CH9054C

Pin	Type	Symbol	Description
1, 15, 16	In	FS2, FS1, FS0	Clock select inputs (internal pull-up)
2	In	XI	Crystal input
3	Out / In	XO / FIN	Crystal output or external FREF input
4, 13	Power	VDD	5V or 3.3V supply
5, 8, 12	Power	GND	Ground
6	Out	24 MHz	24 MHz floppy disk clock output
7	Out	8 MHz	8 MHz keyboard clock output
9	In	CLKEN	CPU clock enable input (active high, internal pull-up). When CLKEN is low, the CPU output is disabled to a low state.
10	In	SD*	Slow down input (active low, internal pull-up)
11	Out	XOUT	Buffered reference (14.318 MHz) clock output
14	Out	CPU	CPU clock output

Table 4 • Pin Description CH9054D

Pin	Type	Symbol	Description
1, 10, 16	In	FS0, FS2, FS1	Clock select inputs (internal pull-up)
2	In	XI	Crystal input
3	Out / In	XO / FIN	Crystal output or external FREF input
4, 13	Power	VDD	5V or 3.3V supply
5, 8, 12	Power	GND	Ground
6	Out	33 MHz	33 MHz floppy disk clock output
7	In	SD*	Slow down input (active low, internal pull-up)
9	In	CLKEN	CPU clock enable input (active high, internal pull-up). When CLKEN is low, the CPU1 output is disabled to a low state.
11	Out	XOUT	Buffered reference (14.318 MHz) clock output
14	Out	CPU2	CPU2 clock output
15	Out	CPU1	CPU1 clock output (pull-low when CLKEN is low)

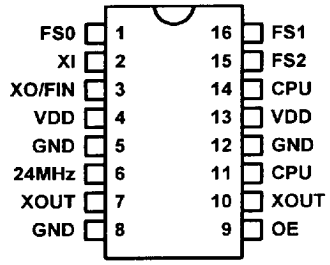

Figure 6: CH9054E

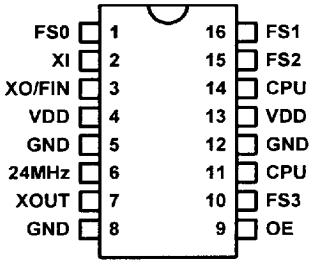

Figure 7: CH9054F

Table 5 • Pin Description CH9054E

Pin	Type	Symbol	Description
1, 15, 16	In	FS0, FS2, FS1	Clock select inputs (internal pull-up)
2	In	XI	Crystal input
3	Out / In	XO / FIN	Crystal output or external FREF input
4, 13	Power	VDD	5V or 3.3V supply
5, 8, 12	Power	GND	Ground
6	Out	24 MHz	24 MHz floppy disk clock output
7, 10	Out	XOUT	Buffered reference (14.318 MHz) clock output
9	In	OE	Output enable input (active high, internal pull-up). When OE is low, all outputs are tristated.
11, 14	Out	CPU	CPU clock outputs

Table 6 • Pin Description CH9054F

Pin	Type	Symbol	Description
1, 10, 15, 16	In	FS0, FS3, FS2, FS1	Clock select inputs (internal pull-up)
2	In	XI	Crystal input
3	Out / In	XO / FIN	Crystal output or external FREF input
4, 13	Power	VDD	5V or 3.3V supply
5, 8, 12	Power	GND	Ground
6	Out	24 MHz	24 MHz floppy disk clock output
7	Out	XOUT	Buffered reference (14.318 MHz) clock output
9	In	OE	Output enable input (active high, internal pull-up). When OE is low, all outputs are tristated.
11, 14	Out	CPU	CPU clock outputs

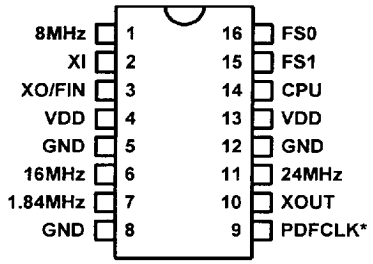

Figure 8: CH9054G

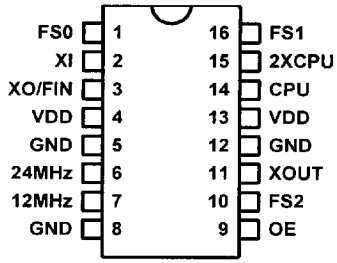

Figure 9: CH9054H

Table 7 • Pin Description CH9054G

Pin	Type	Symbol	Description
1	Out	8 MHz	8 MHz keyboard clock output
2	In	XI	Crystal input
3	Out / In	XO / FIN	Crystal output or external FREF input
4, 13	Power	VDD	5V or 3.3V supply
5, 8, 12	Power	GND	Ground
6	Out	16 MHz	16 MHz AT bus clock output
7	Out	1.84 MHz	1.84 MHz communications clock output
9	In	PDFCLK*	Power down fixed clock input (active low, internal pull-up). When PDFCLK* is low, the 4 fixed clock outputs are disabled and held at a low state.
10	Out	XOUT	Buffered reference (14.318 MHz) clock output
11	Out	24 MHz	24 MHz floppy disk clock output
14	Out	CPU	CPU clock output
15, 16	In	FS1, FS0	Clock select inputs (internal pull-up). When FS1 and FS0 = 0, the CPU clock output is held at a low state.

Table 8 • Pin Description CH9054H

Pin	Type	Symbol	Description
1, 10, 16	In	FS0, FS2, FS1	Clock select inputs (internal pull-up)
2	In	XI	Crystal input
3	Out / In	XO / FIN	Crystal output or external FREF input
4, 13	Power	VDD	5V or 3.3V supply
5, 8, 12	Power	GND	Ground
6	Out	24 MHz	24 MHz floppy disk clock output
7	Out	12 MHz	12 MHz keyboard clock output
9	In	OE	Output enable input (active high, internal pull-up). When OE is low, all outputs are tristated.
11	Out	XOUT	Buffered reference (14.318 MHz) clock output
14	Out	CPU	CPU clock output
15	Out	2XCPU	2XCPU clock output

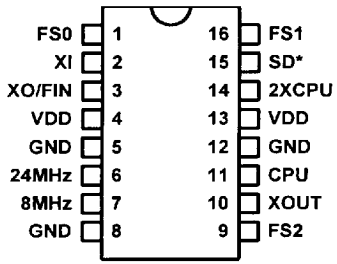

Figure 10: CH9054J

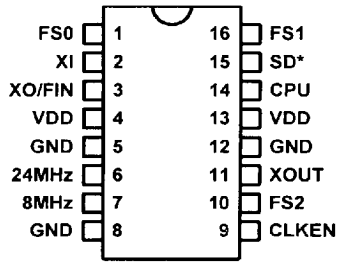

Figure 11: CH9054K

Table 9 • Pin Description CH9054J

Pin	Type	Symbol	Description
1, 9, 16	In	FS0, FS2, FS1	Clock select inputs (internal pull-up)
2	In	XI	Crystal input
3	Out / In	XO / FIN	Crystal output or external FREF input
4, 13	Power	VDD	5V or 3.3V supply
5, 8, 12	Power	GND	Ground
6	Out	24 MHz	24 MHz floppy disk clock output
7	Out	8 MHz	8 MHz keyboard clock output
10	Out	XOUT	Buffered reference (14.318 MHz) clock output
11	Out	CPU	CPU clock output
14	Out	2XCPU	2XCPU clock output
15	In	SD*	Slow down input (active low, internal pull-up)

Table 10 • Pin Description CH9054K

Pin	Type	Symbol	Description
1, 10, 16	In	FS0, FS2, FS1	Clock select inputs (internal pull-up)
2	In	XI	Crystal input
3	Out / In	XO / FIN	Crystal output or external FREF input
4, 13	Power	VDD	5V or 3.3V supply
5, 8, 12	Power	GND	Ground
6	Out	24 MHz	24 MHz floppy disk clock output
7	Out	8 MHz	8 MHz keyboard clock output
9	In	CLKEN	CPU clock enable input (active high, internal pull-up). When CLKEN is low, the CPU output is disabled to a low state.
11	Out	XOUT	Buffered reference (14.318 MHz) clock output
14	Out	CPU	CPU clock output
15	In	SD*	Slow down input (active low, internal pull-up)

Table 11 • Frequencies for CH9054A through C (in MHz)

FS (Frequency Select)				Version A		Version B		Version C	
3	2	1	0	CPU	2XCPU	CPU	2XCPU	CPU	Slow Freq
0	0	0	0	50.0	100.0	50.0	100.0	25.0	8.0
0	0	0	1	40.0	80.0	40.0	80.0	33.33	8.0
0	0	1	0	33.3	66.6	33.3	66.6	40.0	8.0
0	0	1	1	25.0	50.0	25.0	50.0	50.0	16.0
0	1	0	0	20.0	40.0	20.0	40.0	66.6	16.0
0	1	0	1	16.0	32.0	16.0	32.0	60.0	16.0
0	1	1	0	12.0	24.0	12.0	24.0	80.0	16.0
0	1	1	1	8.0	16.0	8.0	16.0	50.0	8.0
1	0	0	0	—	—	—	—	—	—
1	0	0	1	—	—	—	—	—	—
1	0	1	0	—	—	—	—	—	—
1	0	1	1	—	—	—	—	—	—
1	1	0	0	—	—	—	—	—	—
1	1	0	1	—	—	—	—	—	—
1	1	1	0	—	—	—	—	—	—
1	1	1	1	—	—	—	—	—	—
FDCLK (Floppy disk clock output)				24.0		24.0		24.0	
BUSCLK (AT bus clock output)				—		—		—	
KBCLK (Keyboard clock output)				8.0		8.0		8.0	
COMMCLK (Communications clock output)				—		—		—	
XOUT (Reference clock output)				14.318		14.318		14.318	
PDFCLK (Power down fixed clocks)				No		No		No	
Power down				Yes		No		No	
Stop CPU clock				No		No		Yes	
Glitch-free transitions				Yes		Yes		Yes	
Slow down				No		Yes		Yes	
Slow down frequency				N/A		4.0	8.0	See above	

Note: Please consult Chrontel for custom frequency patterns

Table 12 • Frequencies for CH9054D through F (in MHz)

FS (Frequency Select)				Version D		Version E		Version F
3	2	1	0	CPU1, 2	Slow Freq	CPU		CPU
0	0	0	0	25.0	8.0	8.0		75.0
0	0	0	1	33.3	8.0	8.0		32.0
0	0	1	0	40.0	8.0	8.0		60.0
0	0	1	1	50.0	16.0	8.0		40.0
0	1	0	0	66.6	16.0	25.0		50.0
0	1	0	1	60.0	16.0	33.33		66.6
0	1	1	0	80.0	16.0	40.0		80.0
0	1	1	1	50.0	8.0	50.0		52.0
1	0	0	0	—	—	—	—	8.0
1	0	0	1	—	—	—	—	8.0
1	0	1	0	—	—	—	—	8.0
1	0	1	1	—	—	—	—	8.0
1	1	0	0	—	—	—	—	25.0
1	1	0	1	—	—	—	—	33.33
1	1	1	0	—	—	—	—	40.0
1	1	1	1	—	—	—	—	50.0
FDCLK (Floppy disk clock output)				33.3		24.0		24.0
BUSCLK (AT bus clock output)				—		—		—
KBCLK (Keyboard clock output)				—		—		—
COMMCLK (Communications clock output)				—		—		—
XOUT (Reference clock output)				14.318		14.318		14.318
PDFCLK (Power down fixed clocks)				No		No		No
Power down				No		No		No
Stop CPU clock				CPU1 only		Yes[1]		Yes[2]
Glitch-free transitions				Yes		Yes		Yes
Slow down				Yes		No		No
Slow down frequency				See above		N/A		N/A

Note: Please consult Chrontel for custom frequency patterns

1 Slow down controlled by the FS2 pin

2 Slow down controlled by the FS3 pin

Table 13 • Frequencies for CH9054G through K (in MHz)

FS (Frequency Select)				Version G	Version H		Version J		Version K
3	2	1	0	CPU	CPU	2XCPU	CPU	2XCPU	CPU
0	0	0	0	PDCPU[1]	50.0	100.0	8.0	16.0	16.0
0	0	0	1	40.0	40.0	80.0	20.0	40.0	40.0
0	0	1	0	50.0	33.3	66.6	16.7	33.3	33.3
0	0	1	1	66.6	25.0	50.0	12.5	25.0	25.0
0	1	0	0	—	20.0	40.0	30.0	60.0	60.0
0	1	0	1	—	16.0	32.0	10.0	20.0	20.0
0	1	1	0	—	12.0	24.0	33.3	66.6	66.6
0	1	1	1	—	8.0	16.0	25.0	50.0	50.0
1	0	0	0	—	—	—	—	—	—
1	0	0	1	—	—	—	—	—	—
1	0	1	0	—	—	—	—	—	—
1	0	1	1	—	—	—	—	—	—
1	1	0	0	—	—	—	—	—	—
1	1	0	1	—	—	—	—	—	—
1	1	1	0	—	—	—	—	—	—
1	1	1	1	—	—	—	—	—	—
FDCLK (Floppy disk clock output)				24.0	24.0		24.0		24.0
BUSCLK (AT bus clock output)				16.0	—		—		—
KBCLK (Keyboard clock output)				8.0	12.0		8.0		8.0
COMMCLK (Communications clock output)				1.84	—		—		—
XOUT (Reference clock output)				14.318	14.318		14.318		14.318
PDFCLK (Power down fixed clocks)				Yes	No		No		No
Power down				No	No		No		No
Stop CPU clock				No	No		No		Yes
Glitch-free transitions				Yes	Yes		Yes		Yes
Slow down				No	No		Yes		Yes
Slow down frequency				N/A	N/A		4 MHz	8 MHz	8 MHz

Note: Please consult Chrontel for custom frequency pattern

1 Output is low

Table 14 • Absolute Maximum Ratings

Symbol	Description	Value	Unit
V_{DD}	Power supply voltage with respect to GND	−0.5 to +7.0	V
V_{IN}	Input voltage on any pin with respect to GND	−0.5 to V_{DD}+0.5	V
T_{STOR}	Storage temperature	−55 to +150	°C

Note: Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated under the normal operating conditions is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 15 • DC Specifications (Operating Conditions: T_A = 0°C – 70°C, V_{DD} = 5V ±5%)

Symbol	Description	Test Condition @T_A = 25°C	Min	Typ	Max	Unit
V_{OH}	Output high voltage	V_{DD} = 4.75V, I_{OH} = 4mA	2.4			V
V_{OL}	Output low voltage	V_{DD} = 4.75V, I_{OL} = 8mA			0.4	V
V_{IH}	Input high voltage		2.0			V
V_{IL}	Input low voltage				0.8	V
I_{PU}	Input pull-up current			5	20	µA
I_{LK}	Input leakage current		−10		10	µA
C_I	Input capacitance	Except XO / F_{IN}, XI			10	pF
C_I	Input capacitance	Pins XO / F_{IN}, XI		20		pF
I_{PD}	Power down supply current	PD* = Low		10		µA
I_{SD}	Slow down supply current	SD* = Low, V_{DD} = 5V, No load		10		mA
I_{DD}	Operating current	V_{DD} = 5V CPU = 40 MHz, No load CPU = 80 MHz, No load		20 25		mA

Table 16 • AC Specifications (Operating Conditions: T_A = 0°C – 70°C, V_{DD} = 5V ±5%)

Symbol	Description	Test Condition @T_A = 25°C	Min	Typ	Max	Unit
F_{XTAL}	Crystal frequency			14.318		MHz
F_{IN}	Input frequency		1	14.318	32	MHz
T_{IR}	Input clock rise time				20	ns
T_{IF}	Input clock fall time				20	ns
T_R	Output clock rise time	15 pF load, V_{OUT} = 0.8V to 2.0V			3	ns
T_F	Output clock fall time	15 pF load, V_{OUT} = 0.8V to 2.0V			3	ns
T_{DC}	Duty cycle	15 pF load	45	48/52	55	%
T_{JCC}	Jitter, cycle to cycle	CPU = 50 MHz		50	150	ps
T_{FT}	Frequency transition time	8 – 80 MHz		10		ms
T_{PU}	Power up time	From OFF to 100 MHz		15		ms

Table 17 • DC Specifications (Operating Conditions: T_A = 0°C – 70°C, V_{DD} = 3.3V ± 0.3V)

Symbol	Description	Test Condition @T_A = 25°C	Min	Typ	Max	Unit
V_{OH}	Output high voltage	V_{DD} = 3.0V, I_{OH} = 1mA	V_{DD} – 0.5			V
V_{OL}	Output low voltage	V_{DD} = 3.0V, I_{OL} = 2mA			0.5	V
V_{IH}	Input high voltage		2.0			V
V_{IL}	Input low voltage				0.8	V
I_{PU}	Input pull-up current			3		µA
I_{LK}	Input leakage current		–10		10	µA
C_I	Input capacitance	Except XO / F_{IN}, XI			10	pF
C_I	Input capacitance	Pins XO / F_{IN}, XI		20		pF
I_{PD}	Power down supply current	PD* = Low		3		µA
I_{SD}	Slow down supply current	SD* = Low, V_{DD} = 3.3V, No load		10		mA
I_{DD}	Operating current	V_{DD} = 3.3V CPU = 40 MHz, No load CPU = 80 MHz, No load		15 18		mA

Table 18 • AC Specifications (Operating Conditions: T_A = 0°C – 70°C, V_{DD} = 3.3V ± 0.3V)

Symbol	Description	Test Condition @T_A = 25°C	Min	Typ	Max	Unit
F_{XTAL}	Crystal frequency			14.318		MHz
F_{IN}	Input frequency		1	14.318	20	MHz
T_{IR}	Input clock rise time				20	ns
T_{IF}	Input clock fall time				20	ns
T_R	Output clock rise time	15 pF load, V_{OUT} = 0.8V to 2.0V			3	ns
T_F	Output clock fall time	15 pF load, V_{OUT} = 0.8V to 2.0V			3	ns
T_{DC}	Duty cycle	15 pF load	45	48/52	55	%
T_{JCC}	Jitter, cycle to cycle	CPU = 50 MHz		50	150	ps
T_{FT}	Frequency transition time	8 – 80 MHz		10		ms
T_{PU}	Power up time	From OFF to 100 MHz		15		ms

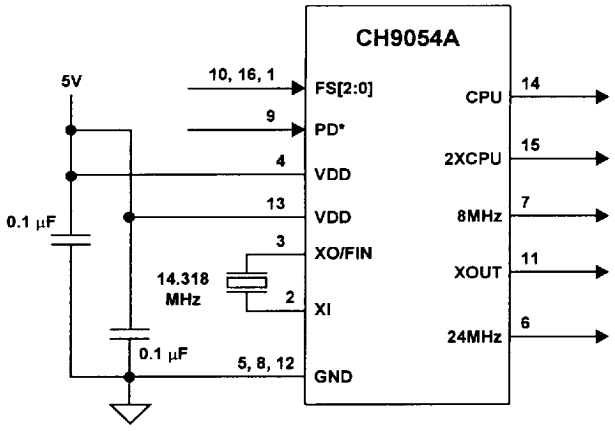

Figure 12: Application Schematic

Note: For other versions, please refer to pin descriptions for exact pin numbers and functions

ORDERING INFORMATION			
Part number	Package type	Number of pins	Voltage supply
CH9054x-N	300 mil PDIP	16	5V
CH9054x-S	150 mil SOIC	16	5V
CH9054x-N-L	300 mil PDIP	16	3.3V
CH9054x-S-L	150 mil SOIC	16	3.3V
Note: x = frequency table version			