

UTC MC4558 LINEAR INTEGRATED CIRCUIT

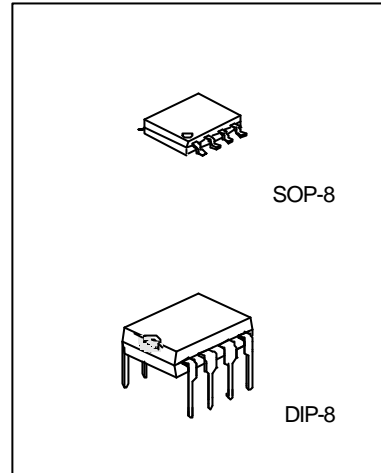
DUAL OPERATIONAL AMPLIFIER

DESCRIPTION

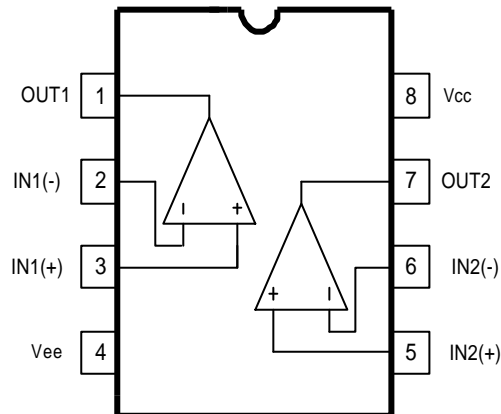
The UTC MC4558 is a monolithic integrated circuit designed for dual operational amplifier.

FEATURES

- *No frequency compensation required
- *No latch-up
- *Large common mode and differential voltage range
- *Parameter tracking over temperature range
- *Gain and phase match between amplifiers
- *Internally frequency compensated
- *Low noise input transistors

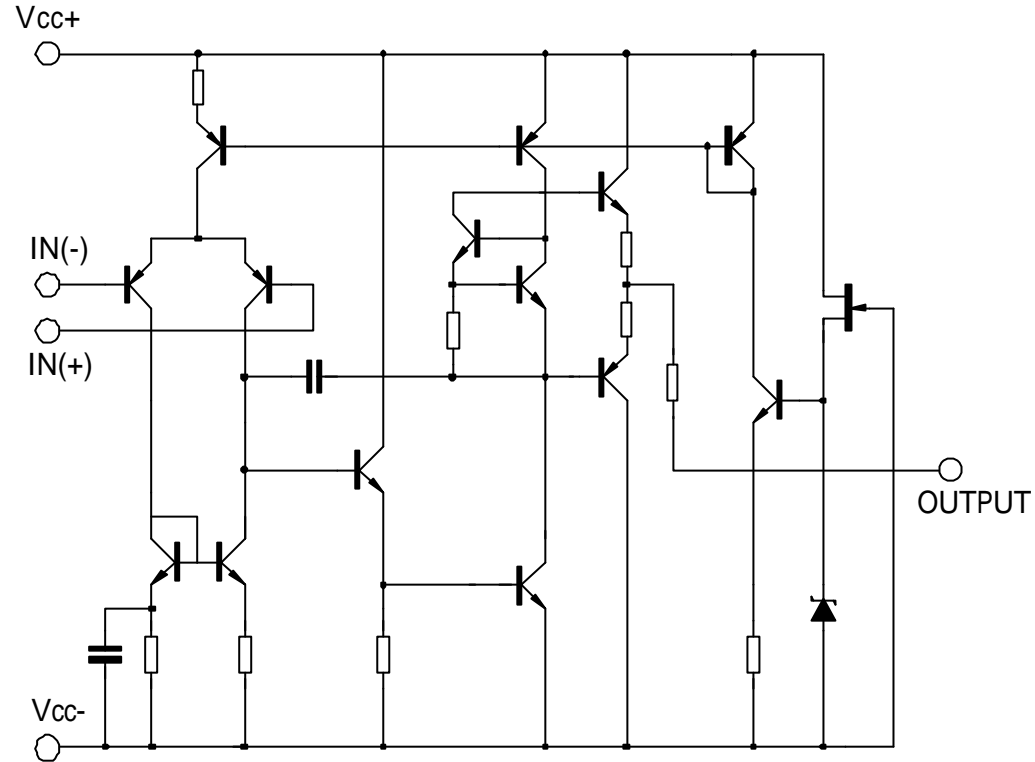


PIN CONFIGURATIONS



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BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V _{cc}	+22	V
Differential input voltage	V _{I(DIFF)}	+18	V
Power Dissipation	P _D	DIP-8	600
		SOP-8	400
Input Voltage	V _I	+15	V
Operating Temperature	T _{OPR}	0 ~ +70	°C
Storage Temperature	T _{STG}	-65 ~ +150	°C

ELECTRICAL CHARACTERISTICS (T_a=25°C, V_{cc}=15V, V_{ee}=-15V)

PARAMETER	SYMBOL	TEST CONDUCTION	MIN	TYP	MAX	UNIT
Supply Current, all Amp, no load	I _{cc}			2.3	4.5	mA
Input offset voltage	V _{IO}	R _s <10kΩ		2	6	mV
Input offset current	I _{IO}			5	200	nA
Input bias current	I _{BIAS}			30	500	nA

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PARAMETER	SYMBOL	TEST CONDUCTION	MIN	TYP	MAX	UNIT
Large signal voltage gain	Gv	Vo(p-p)=±10V, RL≤2kΩ	20	200		V/mV
Common Mode Input Voltage Range	VI(R)		+12	+13		V
Common Mode Rejection Ratio	CMRR	Rs≤10kΩ	70	90		dB
Supply Voltage Rejection Ratio	PSRR	Rs≤10kΩ	76	90		dB
Output Voltage swing	Vo(p-p)	RL≥10kΩ		+12	+14	V
Power Consumption	Pc			70	170	mV
Slew Rate	SR	Vi=±10V, RL≥2kΩ, CL≤100pF	1.2	2.2		V/μs
Rise Time	TRIS	Vi=±20mV, RL≥2kΩ, CL≤100pF		0.3		μs
Overshoot	OS	Vi=±20mV, RL≥2kΩ, CL≤100pF		15		%
Input Resistance	Ri		0.3	2		MΩ
Output Resistance	Ro			75		Ω
Total Harmonic Distortion	THD	f=1kHz, Av=20dB, RL=2kΩ, Vo=2Vpp, CL=100pF		0.008		%
Channel Separation	Vo1/Vo2			120		dB

FREQUENCY CHARACTERISTICS (Ta=25°C, Vcc=15V, Vee=-15V)

PARAMETER	SYMBOL	TEST CONDUCTION	MIN	TYP	MAX	UNIT
Unity Gain Bandwidth	BW		2.0	2.8		MHz

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TYPICAL PERFORMANCE CHARACTERISTICS

Fig. 1 Burst Noise vs Rs

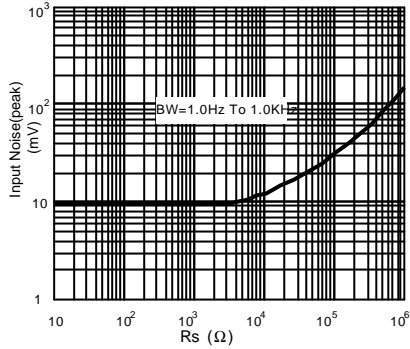


Fig. 2 RMS Noise vs Rs

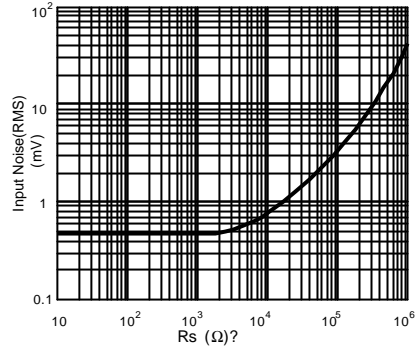


Fig. 3 Output Noise vs Rs

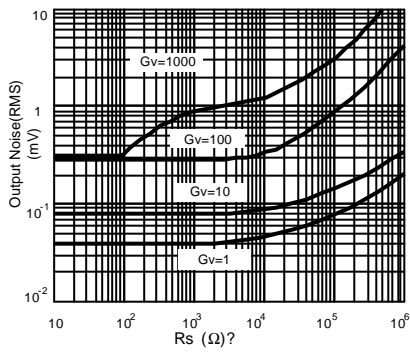


Fig. 4 Spectral Noise Density

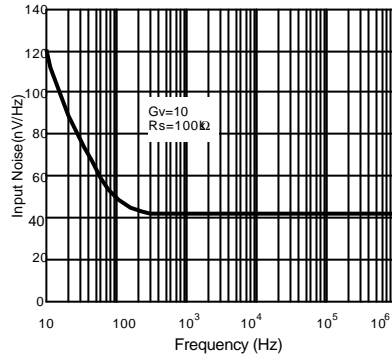


Fig. 5 Open loop frequency response

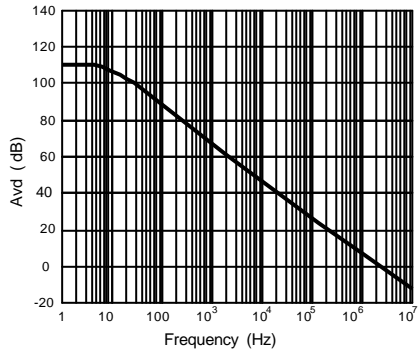
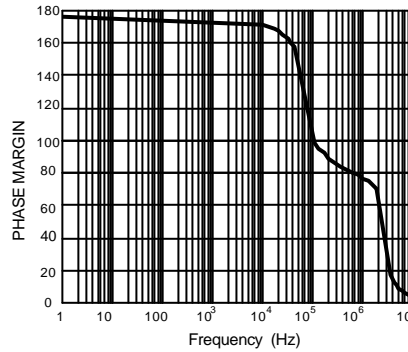


Fig. 6 PHASE MARGIN vs FREQUENCY



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