

HD74UH02

2-input NOR Gate

REJ03D0200-0500Z
(Previous ADE-205-015C (Z))
Rev.5.00
Jan.30.2004

Description

The HD74UH02 is high-speed CMOS two input NOR gate using silicon gate CMOS process. With CMOS low power dissipation, it provides high-speed equivalent to LS-TTL series. The internal circuit of three stages construction with buffer provides wide noise margin and stable output.

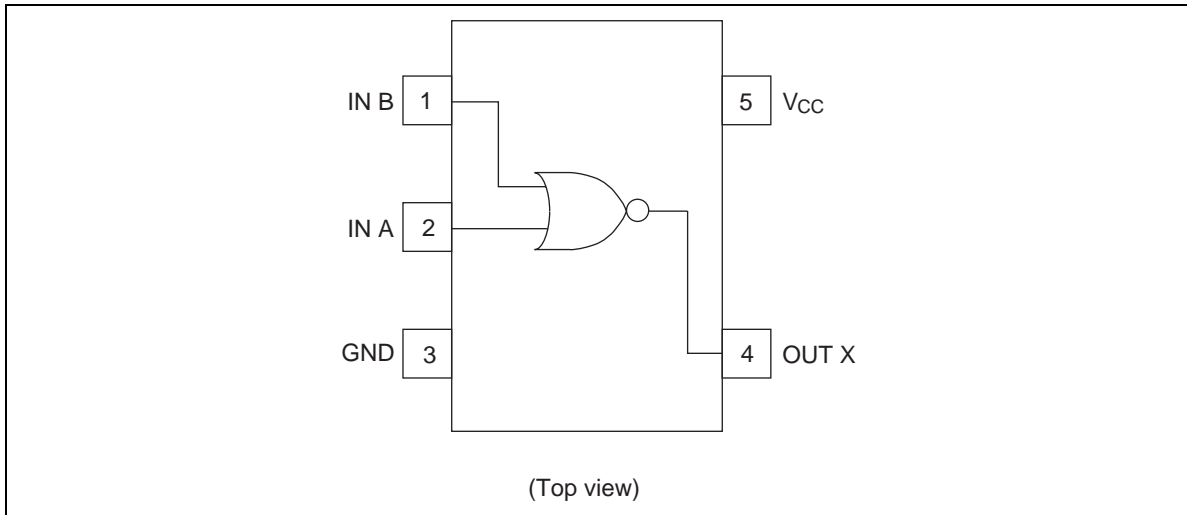
Features

- Encapsulated in very small 5pins package of $2.9 \times 1.6 \times 1.1$ mm, the efficiency to mount on substrate is significantly improved.
- The basic gate function is lined up as Renesas uni logic series.
- Supplied on emboss taping for high-speed automatic mounting.
- Electrical characteristics equivalent to the HD74HC02
Supply voltage range: 2 to 6 V
Operating temperature range: -40 to $+85^{\circ}\text{C}$
- $|I_{OH}| = I_{OL} = 2$ mA (min)
- Ordering Information

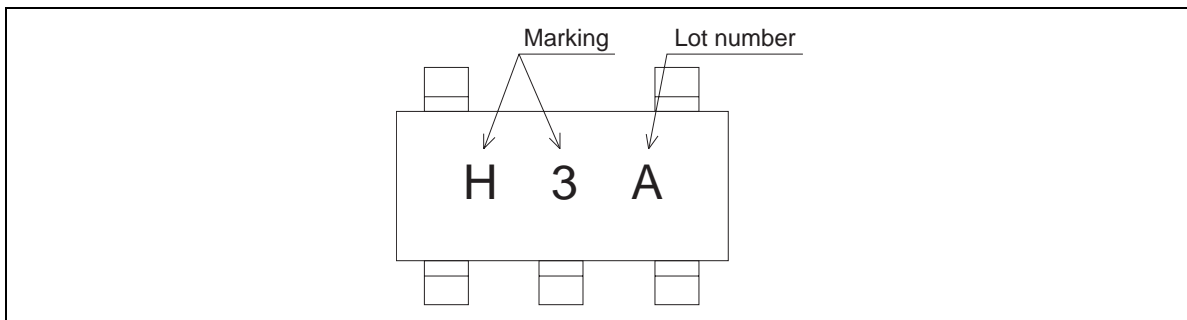
Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
HD74UH02EL	MPAK-5 pin	MPAK-5V	–	EL (3,000 pcs/reel)

HD74UH02

Pin Arrangement



Article Indication



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	V _{CC}	-0.5 to +7.0	V
Input voltage	V _{IN}	-0.5 to V _{CC} +0.5	V
Output voltage	V _{OUT}	-0.5 to V _{CC} +0.5	V
Input diode current	I _{IK}	±20	mA
Output diode current	I _{OK}	±20	mA
Output current	I _{OUT}	±25	mA
V _{CC} /GND current	I _{CC} , I _{GND}	±25	mA
Power dissipation	P _T	200	mW
Storage temperature	T _{stg}	-65 to +150	°C

Recommended Operating Conditions

Item	Symbol	Ratings	Unit
Supply voltage	V_{CC}	2 to 6	V
Input voltage	V_{IN}	0 to V_{CC}	V
Output voltage	V_{OUT}	0 to V_{CC}	V
Operating temperature	T_{opr}	-40 to +85	°C
Input rise/fall time	t_r, t_f	0 to 1000 ($V_{CC} = 2.0$ V)	ns
		0 to 500 ($V_{CC} = 4.5$ V)	
		0 to 400 ($V_{CC} = 6.0$ V)	

Electrical Characteristics

Item	Symbol	V_{CC} (V)	$T_a = 25^\circ\text{C}$			$T_a = -40 \text{ to } 85^\circ\text{C}$		Unit	Test Conditions		
			Min	Typ	Max	Min	Max				
Input voltage	V_{IH}	2.0	1.5	—	—	1.5	—	V			
		4.5	3.15	—	—	3.15	—				
		6.0	4.2	—	—	4.2	—				
	V_{IL}	2.0	—	—	0.5	—	0.5	V			
		4.5	—	—	1.35	—	1.35				
		6.0	—	—	1.8	—	1.8				
Output voltage	V_{OH}	2.0	1.9	2.0	—	1.9	—	V	$V_{IN} = V_{IL}$	$I_{OH} = -20 \mu\text{A}$	
		4.5	4.4	4.5	—	4.4	—				
		6.0	5.9	6.0	—	5.9	—				
		4.5	4.18	4.31	—	4.13	—				$I_{OH} = -2 \text{ mA}$
		6.0	5.68	5.80	—	5.63	—				$I_{OH} = -2.6 \text{ mA}$
		6.0	—	0.0	0.1	—	0.1				V
	4.5	—	0.0	0.1	—	0.1					
	6.0	—	0.0	0.1	—	0.1					
	4.5	—	0.17	0.26	—	0.33	$I_{OL} = 2 \text{ mA}$				
	6.0	—	0.18	0.26	—	0.33	$I_{OL} = 2.6 \text{ mA}$				
	6.0	—	—	±0.1	—	±1.0	μA	$V_{IN} = V_{CC} \text{ or } \text{GND}$			
	Operating current	I_{CC}	6.0	—	—	1.0	—	10.0	$V_{IN} = V_{CC} \text{ or } \text{GND}$		

Switching Characteristics

($C_L = 15 \text{ pF}$, $t_r = t_f = 6 \text{ ns}$, $V_{CC} = 5 \text{ V}$)

Item	Symbol	Ta = 25°C			Unit	Test Conditions
		Min	Typ	Max		
Output rise/fall time	t_{TLH}	—	5	10	ns	See Test circuit
	t_{THL}					
Propagation delay time	t_{PLH}	—	7	15	ns	See Test circuit
	t_{PHL}					

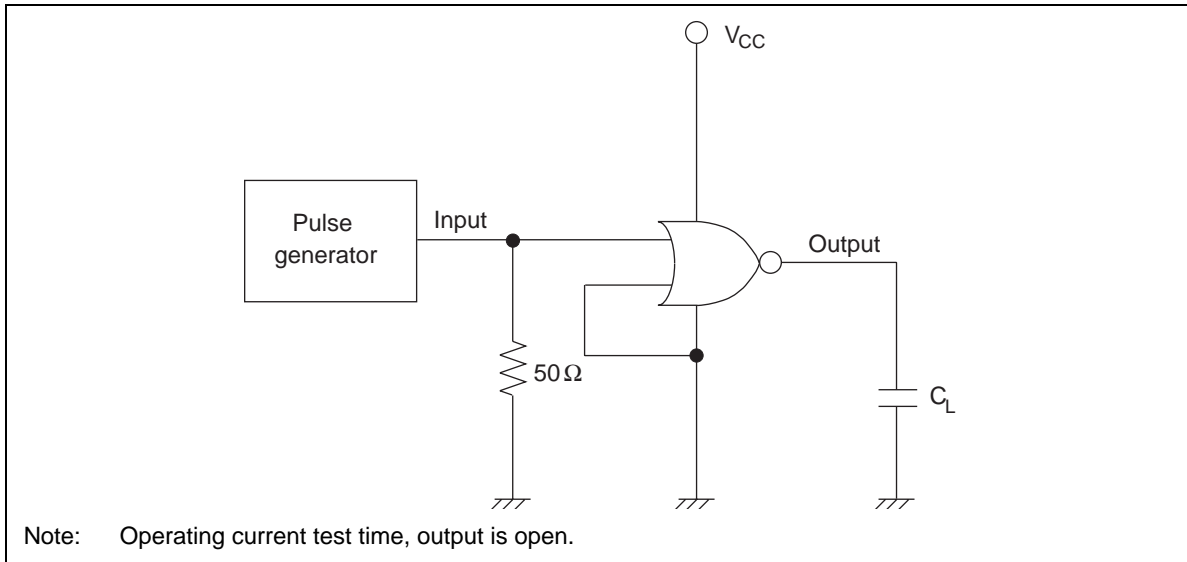
($C_L = 50 \text{ pF}$, $t_r = t_f = 6 \text{ ns}$)

Item	Symbol	V _{CC} (V)	Ta = 25°C			Ta = -40 to 85°C		Unit	Test Conditions
			Min	Typ	Max	Min	Max		
Output rise/fall time	t_{TLH}	2.0	—	50	125	—	155	ns	See Test circuit
	t_{THL}	4.5	—	14	25	—	31		
		6.0	—	12	21	—	26		
Propagation delay time	t_{PLH}	2.0	—	48	100	—	125	ns	See Test circuit
	t_{PHL}	4.5	—	12	20	—	25		
		6.0	—	9	17	—	21		
Input capacitance	C_{IN}	—	—	5	10	—	10	pF	
Equivalent capacitance	C_{PD}	—	—	10	—	—	—		

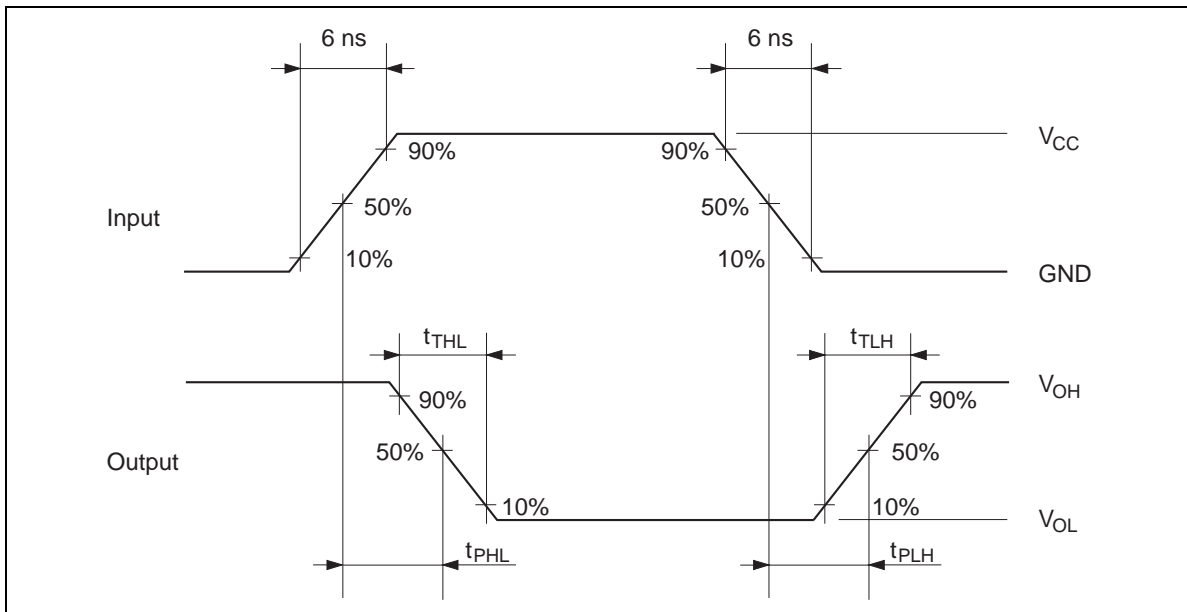
Note: C_{PD} is equivalent capacitance inside of the IC calculated from the operating current without load (see test circuit). The average operating current without load is calculated according to the expression below.

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

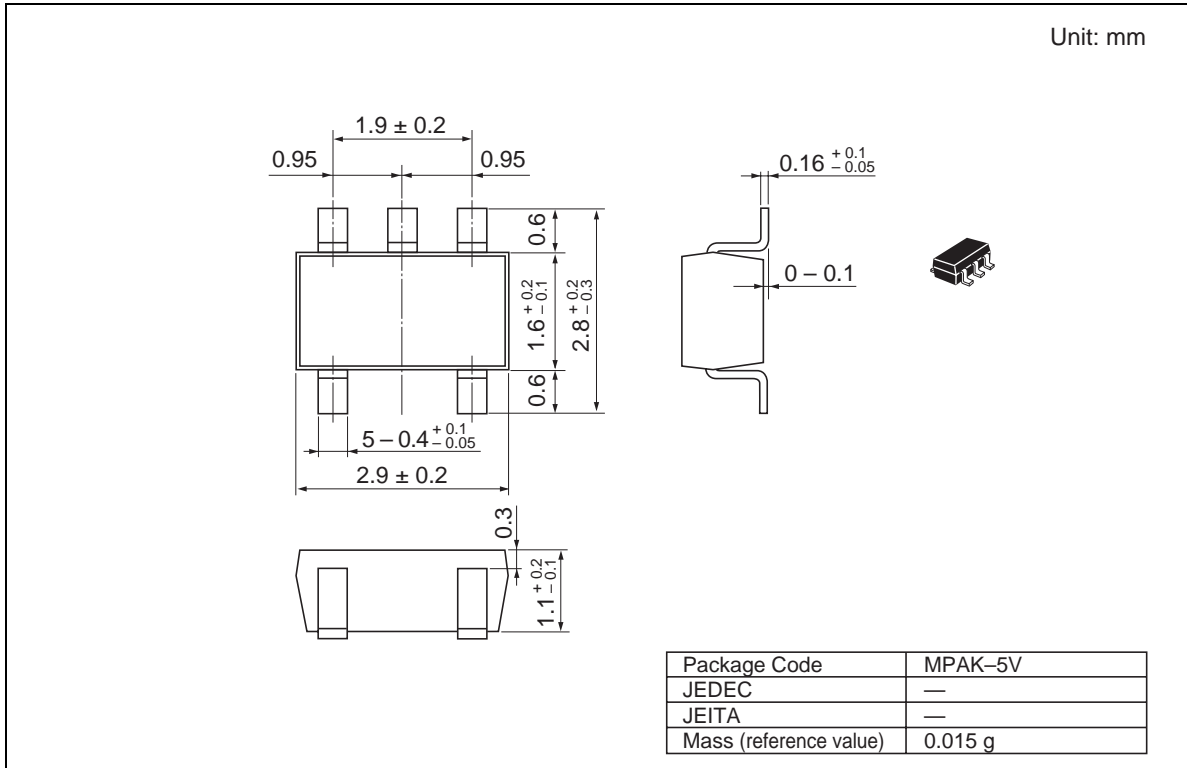
Test Circuit



Waveforms



Package Dimensions



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