LG Semicon Co.,Ltd.

GM76C8128CL/CLL-W

131,072 WORDS x 8 BIT
CMOS STATIC RAM

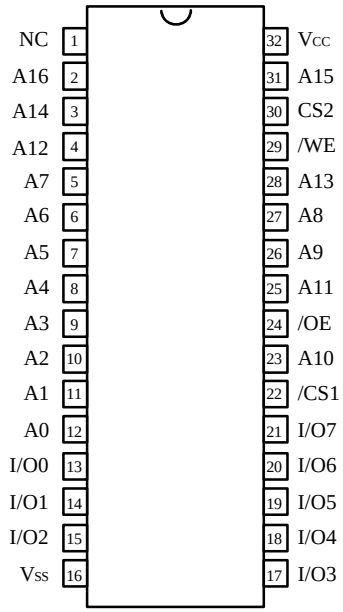
Description

The GM76C8128CL/CLL-W is a 1,048,576 bits static random access memory organized as 131,072 words by 8 bits. Using a 0.6*u*m advanced CMOS technology and operated from a single 2.7V to 5.5V supply. Advanced circuit technique provide both high speed and low power consumption. The device is placed in a low power standby mode with /CS1 high or CS2 low and the output enable (/OE) allows fast memory access. Thus it is suitable for high speed and low power applications, especially where battery back-up is required.

Features

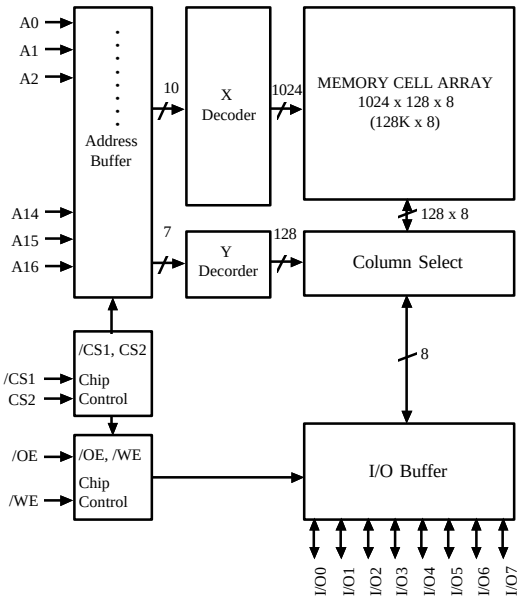
* Fast Speed : 55/70ns at Vcc=5V+/-10%
  120/150ns at Vcc=3V+/-10%
* Low Power Standby and Low Power Operation
  -Standby : 0.11mW Max. at Vcc=5V+/-10%
  49.5uW Max. at Vcc=3V+/-10%
  -Operation : 385mW Max. at Vcc=5V+/-10%
  66mW Max. at Vcc=3V+/-10%
* Completely Static RAM : No Clock or Timing Strobe Required
* Equal Access and Cycle Time
* TTL compatible inputs and outputs
* Capability of Battery Back-up Operation
* Single +2.7V ~ +5.5V Operation
* Standard 32 DIP, SOP and TSOP I

Pin Configuration



(Top View)

Block Diagram



Pin Description

Pin	Function
A0-A16	Address Inputs
/WE	Write Enable Input
/CS1, CS2	Chip Select Input
/OE	Output Enable Input
I/O0-I/O7	Data Inputs/Outputs
V_{CC}	Power Supply (2.7V~5.5V)
V_{SS}	Ground
NC	No Connection

Absolute Maximum Ratings*

Symbol	Parameter	Rating	Unit
T_A	Ambient Temperature under Bias	0 ~ 70	C
T_{STG}	Storage Temperature	-55 ~ 150	C
T_{SOL}	Soldering Temperature and Time	260, 10 (at lead)	C, S
V_{CC}	Supply Voltage	-0.3 ~ 7.0	V
V_{IN}	Input Voltage	-0.3 ~ 7.0	V
$V_{I/O}$	Input and Output Voltage	-0.5 ~ V_{CC} + 0.5	V
P_D	Power Dissipation	1.0	W

*: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions (T_A = 0 ~ 70C)

Symbol	Parameter	Vcc = 5V +/- 10%			Vcc = 2.7 ~ 5.5V			Unit
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5.0	5.5	2.7	3.0	5.5	V
V_{IH}	Input High Voltage	2.2	-	V_{CC} + 0.3	2.2	-	V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	-0.3*	-	0.8	-0.3*	-	0.4	V

*Note :V_{IL}(min) = -3.0V for <= 10ns pulse

Truth Table

/CS1	CS2	/OE	/WE	A0 to A16	DATA I/O	MODE
L	H	L	H	Stable	Output Data	Read
L	H	X	L	Stable	Input Data	Write
L	H	H	H	Stable	Hi-Z	Output Disable
H	X	X	X	-	Hi-Z	Standby
X	L	X	X	-	Hi-Z	

*Note: X means don't care

Capacitance (f = 1MHz, T_A = 25C)

Symbol	Parameter	Test Conditions	Min	Max	Unit
C_{IN}	Input Capacitance	V_I = 0V	-	6	pF
$C_{I/O}$	Output Capacitance	V_O = 0V	-	8	pF

*Note: This parameter is sampled and not 100% tested.

DC Operating Characteristics (V_{CC} = 3V+/-10%, T_A = 0 ~ 70C)

Symbol	Parameter	Conditions		Min	*Typ	Max	Unit
$I_{I(L)}$	Input Leakage Current	V_{IN} = 0 to V_{CC}		-1	-	1	uA
$I_{O(L)}$	Output Leakage Current	/CS1 = V_{IH} or CS2 = V_{IL} /OE = V_{IH}, V_{SS} <=V_{OUT}<=V_{CC}		-1	-	1	uA
V_{OH}	High Level Output Voltage	I_{OH} = -1.0mA		2.2	-	-	V
V_{OL}	Low Level Output Voltage	I_{OL} = 2.1mA		-	-	0.4	V
I_{CC}	Operating Supply Current	/CS1 = V_{IL} and CS2 = V_{IH} V_{IN} = V_{IH}/V_{IL}, I_{OUT} = 0mA		-	-	5	mA
I_{CC1}	Average Operating Current	/CS1 = V_{IL} and CS2 = V_{IH} V_{IN} = V_{IH}/V_{IL} I_{OUT} = 0mA tcycle = Min, cycle		-	-	20	mA
I_{CC2}		/CS1 = 0.2V, CS2 = V_{CC}-0.2V V_{IN} = V_{CC} - 0.2V/0.2V I_{OUT} = 0mA tcycle = 1*u*s		-	-	5	mA
I_{CCS1}	Standby Current (TTL)	/CS1 = V_{IH}, CS2 = V_{IL}		-	-	0.5	mA
I_{CCS2}	Standby Current (CMOS)	/CS1 = V_{CC}-0.2V CS2 = 0.2V	L - Version LL - Version	- -	- -	50 15	uA

*Typ. Values are measured at 25C

AC Operating Characteristics

Test Conditions (V_{CC} = 3V+/-10%, T_A = 0 ~ 70C, unless otherwise noted.)

Parameter	Value
Input Pulse Level	0.4V to 2.2V
Input Rise and Fall Time	5ns
Input and Output Timing Reference Levels	1.5V
Output Load	C_L = 100pF + 1TTL Load

AC Operating Characteristics (V_{CC} = 3V+/-10%, T_A = 0 ~ 70C)

Read Cycle

Symbol	Parameter	GM76C8128C-55W		GM76C8128C-70W		Unit
		Min	Max	Min	Max	
t_{RC}	Read Cycle Time	120	-	150	-	ns
t_{AA}	Address Access Time	-	120	-	150	ns
t_{ACS1}	Chip Select 1 Access Time	-	120	-	150	ns
t_{ACS2}	Chip Select 2 Access Time	-	120	-	150	ns
t_{OE}	Output Enable Access Time	-	55	-	60	ns
t_{CLZ1}	Chip Select 1 Output Setup Time	10	-	10	-	ns
t_{CHZ1}	Chip Select 1 Output Floating	-	40	-	45	ns
t_{CLZ2}	Chip Select 2 Output Setup Time	10	-	10	-	ns
t_{CHZ2}	Chip Select 2 Output Floating	-	40	-	45	ns
t_{OLZ}	Output Enable Output Setup Time	10	-	10	-	ns
t_{OHZ}	Output Enable Output Floating	-	40	-	45	ns
t_{OH}	Output Hold Time	10	-	10	-	ns

Write Cycle

Symbol	Parameter	GM76C8128C-55W		GM76C8128C-70W		Unit
		Min	Max	Min	Max	
t_{WC}	Write Cycle Time	120	-	150	-	ns
t_{CW1}	Chip Select Time 1	100	-	120	-	ns
t_{CW2}	Chip Select Time 2	100	-	120	-	ns
t_{AW}	Address Enable Time	100	-	120	-	ns
t_{AS}	Address Setup Time	0	-	0	-	ns
t_{WP}	Write Pulse Width	65	-	70	-	ns
t_{WR}	Address Hold Time	0	-	0	-	ns
t_{DW}	Input Data Setup Time	40	-	45	-	ns
t_{DH}	Input Data Hold Time	0	-	0	-	ns
t_{WHZ}	Write to Output in High-Z	-	40	-	50	ns
t_{OW}	Output Active from End of Write	10	-	10	-	ns

DC Operating Characteristics (V_{CC} = 5V+/-10%, T_A = 0 ~ 70C)

Symbol	Parameter	Conditions		Min	*Typ	Max	Unit
$I_{I(L)}$	Input Leakage Current	V_{IN} = 0 to V_{CC}		-1	-	1	uA
$I_{O(L)}$	Output Leakage Current	/CS1 = V_{IH} or CS2 = V_{IL} /OE = V_{IH}, V_{SS} <=V_{OUT}<=V_{CC}		-1	-	1	uA
V_{OH}	High Level Output Voltage	I_{OH} = -1.0mA		2.4	-	-	V
V_{OL}	Low Level Output Voltage	I_{OL} = 2.1mA		-	-	0.4	V
I_{CC}	Operating Supply Current	/CS1 = V_{IL} and CS2 = V_{IH} V_{IN} = V_{IH}/V_{IL}, I_{OUT} = 0mA		-	-	15	mA
I_{CC1}	Average Operating Current	/CS1 = V_{IL} and CS2 = V_{IH} V_{IN} = V_{IH}/V_{IL} I_{OUT} = 0mA tcycle = Min, cycle		-	-	70	mA
I_{CC2}		/CS1 = 0.2V, CS2 = V_{CC}-0.2V V_{IN} = V_{CC} - 0.2V/0.2V I_{OUT} = 0mA tcycle = 1*u*s		-	-	10	mA
I_{CCS1}	Standby Current (TTL)	/CS1 = V_{IH}, CS2 = V_{IL}		-	-	2	mA
I_{CCS2}	Standby Current (CMOS)	/CS1 = V_{CC}-0.2V CS2 = 0.2V	L - Version LL - Version	- -	- -	100 20	uA

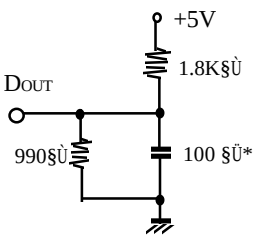
*Typ. Values are measured at 25C

AC Operating Characteristics

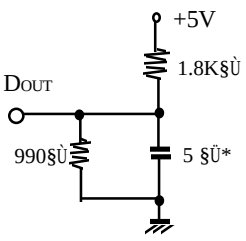
Test Conditions (V_{CC} = 5V+/-10%, T_A = 0 ~ 70C, unless otherwise noted.)

Parameter	Value
Input Pulse Level	0.6V to 2.4V
Input Rise and Fall Time	5ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

Output Load (A)



Output Load (B) (for tCHZ, tCLZ, tWHZ, tOW, tOLZ & tOHZ)



AC Operating Characteristics (V_{CC} = 5V+/-10%, T_A = 0 ~ 70C)

Read Cycle

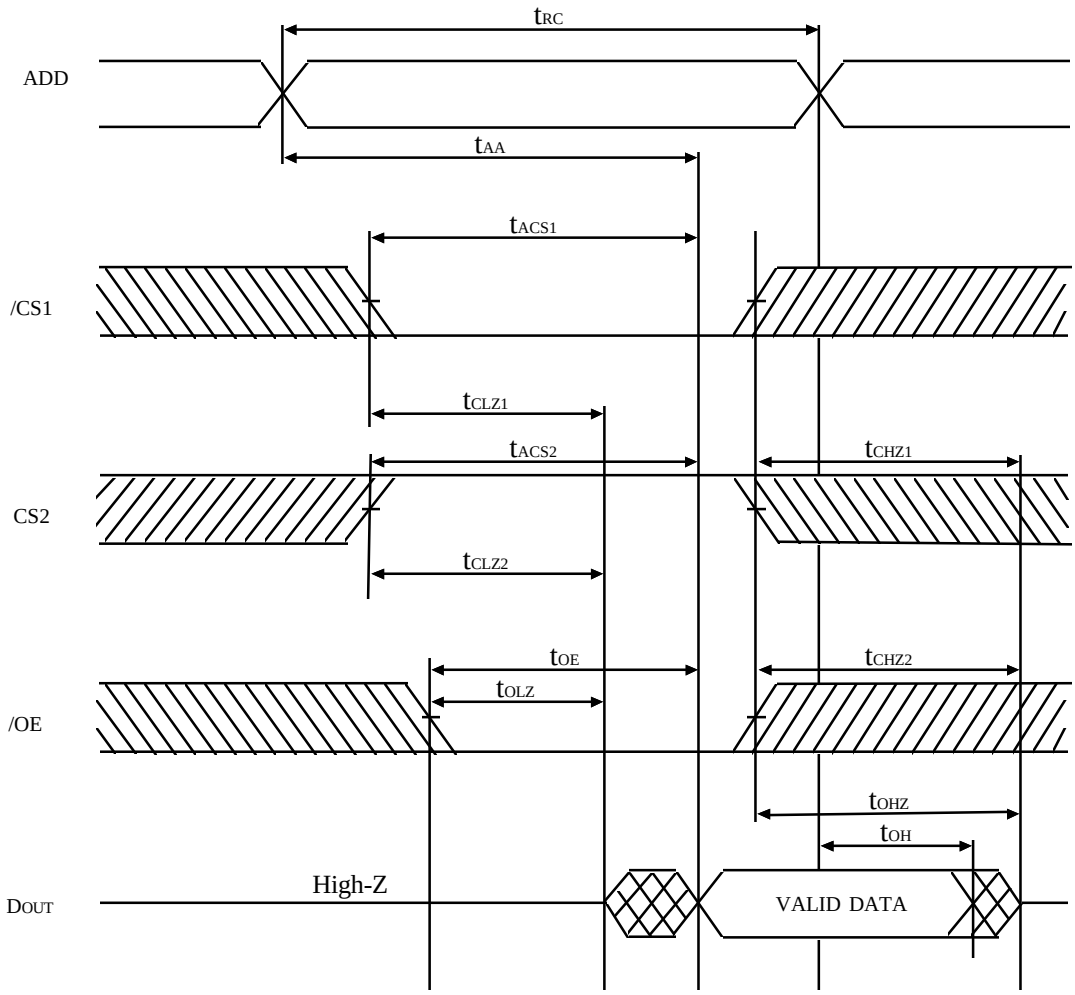
Symbol	Parameter	GM76C8128C-55W		GM76C8128C-70W		Unit
		Min	Max	Min	Max	
t_{RC}	Read Cycle Time	55	-	70	-	ns
t_{AA}	Address Access Time	-	55	-	70	ns
t_{ACS1}	Chip Select 1 Access Time	-	55	-	70	ns
t_{ACS2}	Chip Select 2 Access Time	-	55	-	70	ns
t_{OE}	Output Enable Access Time	-	30	-	35	ns
t_{CLZ1}	Chip Select 1 Output Setup Time	5	-	5	-	ns
t_{CHZ1}	Chip Select 1 Output Floating	-	20	-	25	ns
t_{CLZ2}	Chip Select 2 Output Setup Time	5	-	5	-	ns
t_{CHZ2}	Chip Select 2 Output Floating	-	20	-	25	ns
t_{OLZ}	Output Enable Output Setup Time	0	-	0	-	ns
t_{OHZ}	Output Enable Output Floating	-	20	-	25	ns
t_{OH}	Output Hold Time	10	-	10	-	ns

Write Cycle

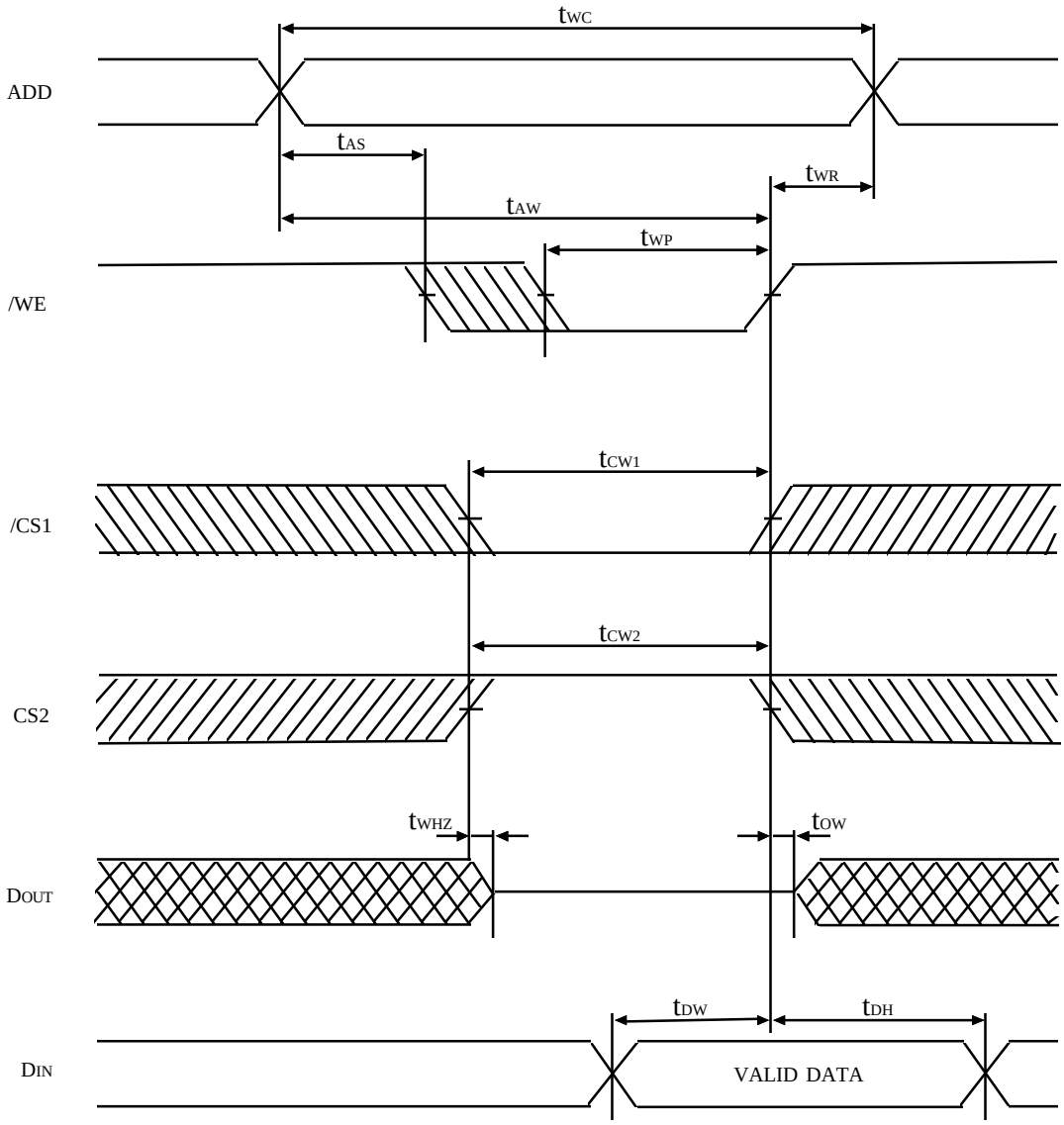
Symbol	Parameter	GM76C8128C-55W		GM76C8128C-70W		Unit
		Min	Max	Min	Max	
t_{WC}	Write Cycle Time	55	-	70	-	ns
t_{CW1}	Chip Select Time 1	50	-	65	-	ns
t_{CW2}	Chip Select Time 2	50	-	65	-	ns
t_{AW}	Address Enable Time	50	-	60	-	ns
t_{AS}	Address Setup Time	0	-	0	-	ns
t_{WP}	Write Pulse Width	45	-	50	-	ns
t_{WR}	Address Hold Time	0	-	0	-	ns
t_{DW}	Input Data Setup Time	25	-	30	-	ns
t_{DH}	Input Data Hold Time	0	-	0	-	ns
t_{WHZ}	Write to Output in High-Z	-	20	-	25	ns
t_{OW}	Output Active from End of Write	0	-	0	-	ns

Timing Waveforms

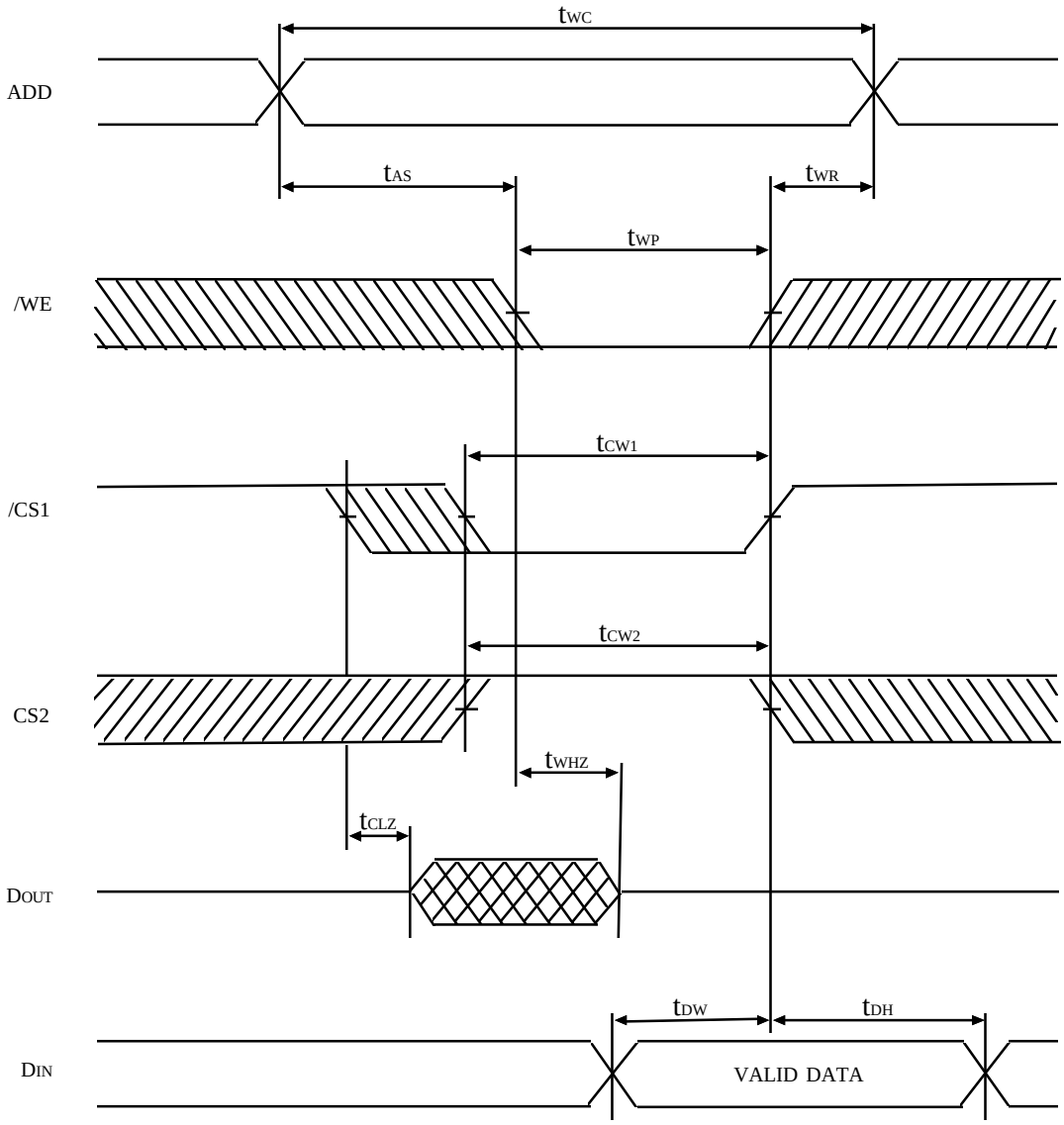
Read Cycle (Note 1)



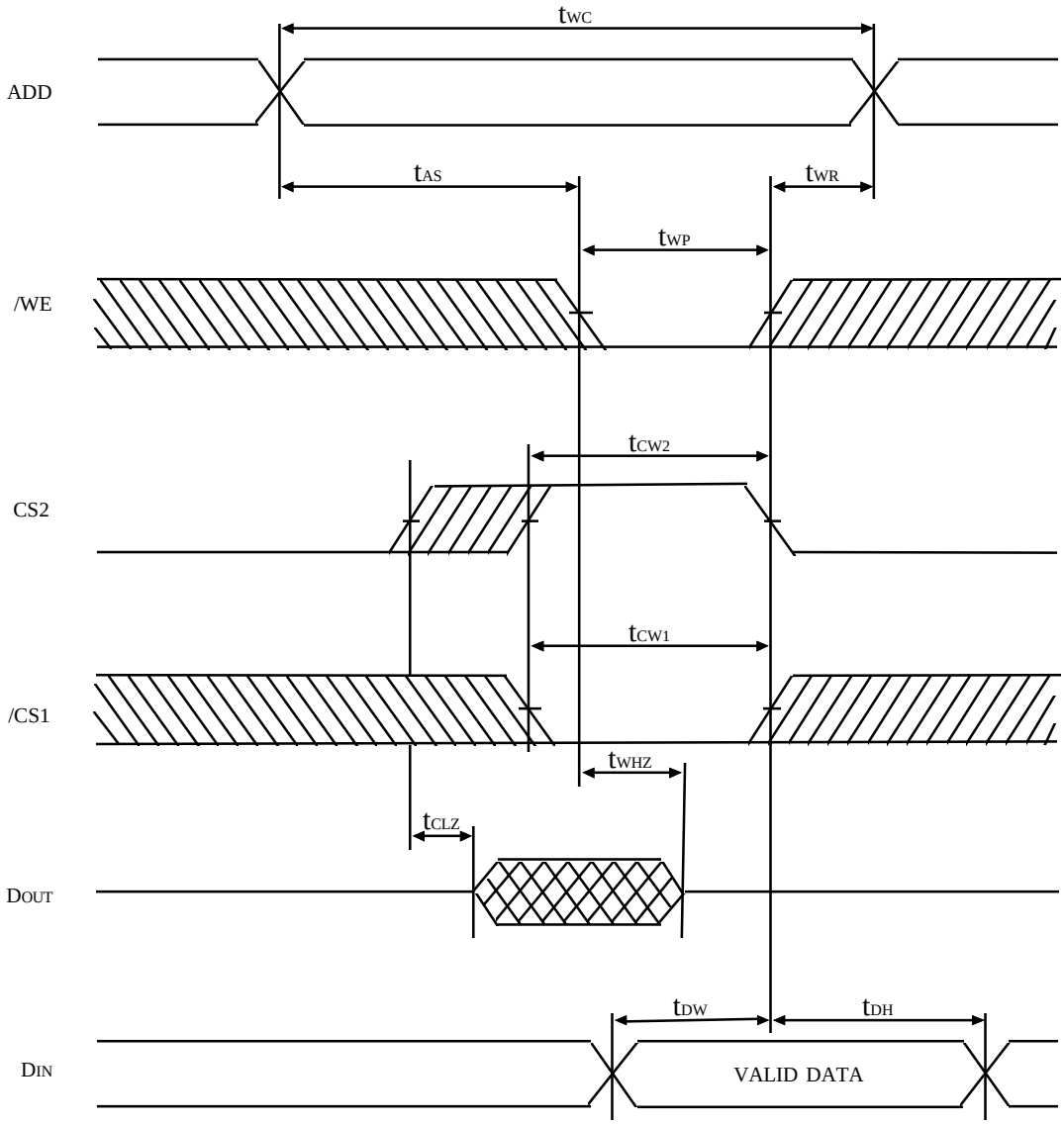
Write Cycle (1) (/WE Controlled) (Notes 2, 3, 4)



Write Cycle (2) (/CS1 Controlled) (Notes 4)



Write Cycle (3) (CS2 Controlled) (Notes 4)



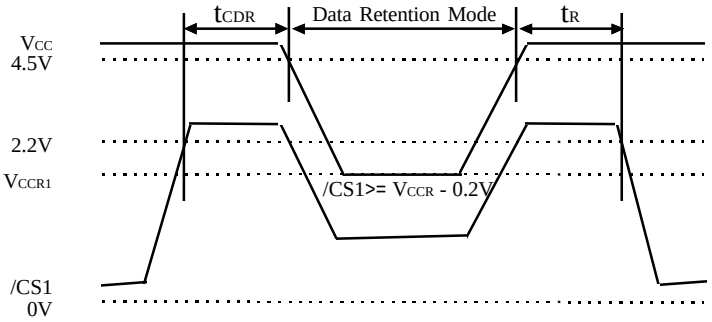
Notes:
1. /WE is High for Read Cycle.
2. Assuming that /CS1 Low transition or CS2 High transition occurs coincident with or after /WE Low transition. Outputs remain in a high impedance state.
3. Assuming that /CS1 High transition or CS2 Low transition occurs coincident with or prior to /WE High transition. Outputs remain in a high impedance state.
4. Assuming that /OE is high for write cycle. Outputs are in a high impedance state during this period.

Data Retention Characteristics

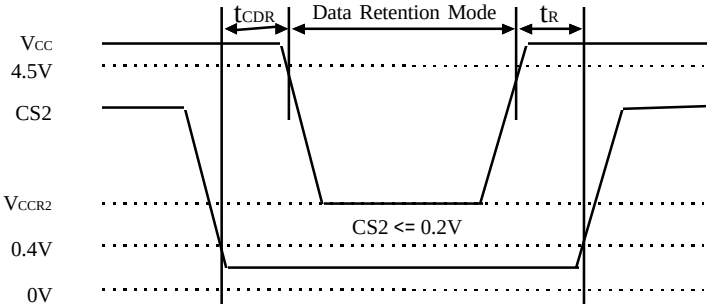
Symbol	Parameter			Min	Typ	Max	Unit
V_{CCR}	Data Retention Supply Voltage			2.0	-	5.5	V
I_{CCR}	Data Retention Current	VCC=3.0V	L - Version LL - Version	- -	1 0.5	50 15*	*u*A
t_{CDR}	Chip Select to Data Retention Time			0	-	-	ns
t_R	Operation Recovery Time			t_{RC}**	-	-	ns

* 3*u*A max at T_A = 0 ~ 40C
** tRC = Read Cycle

* Low V_{CC} Data Retention Mode: (1) /CS1 Controlled



* Low V_{CC} Data Retention Mode: (2) CS2 Controlled

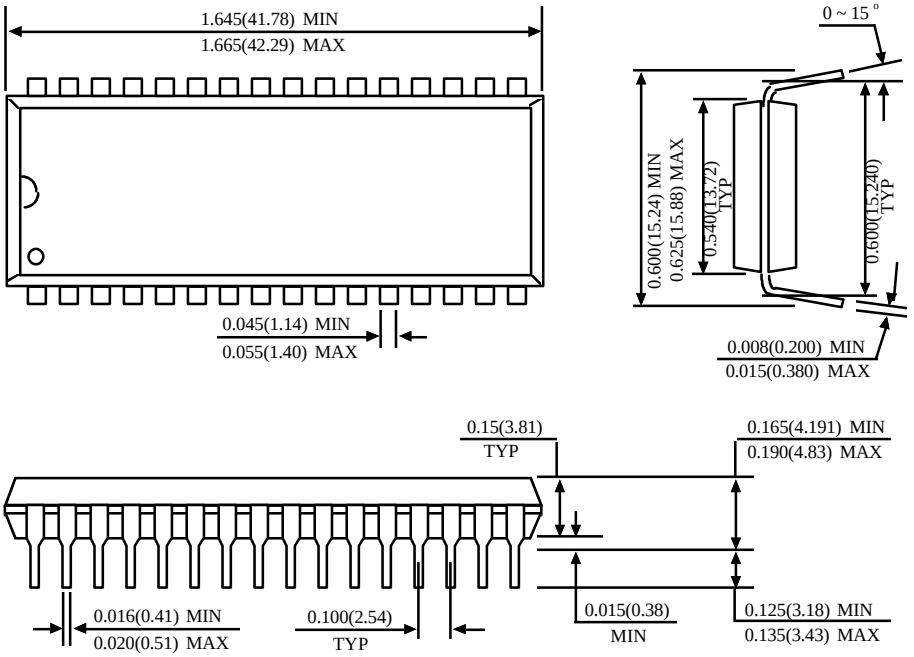


Notes: In Data Retention Mode, CS2 controls the Address, /WE, /CS1, /OE and D_{IN} buffer. If CS2 controls data retention mode, V_{IN} for these inputs can be in the high impedance state. If /CS1 controls the data retention mode, CS2 must satisfy either CS2≥V_{CCR} - 0.2V or CS2<=0.2V. The other input levels (Address, /WE, /OE, I/O) can be in the high impedance state.

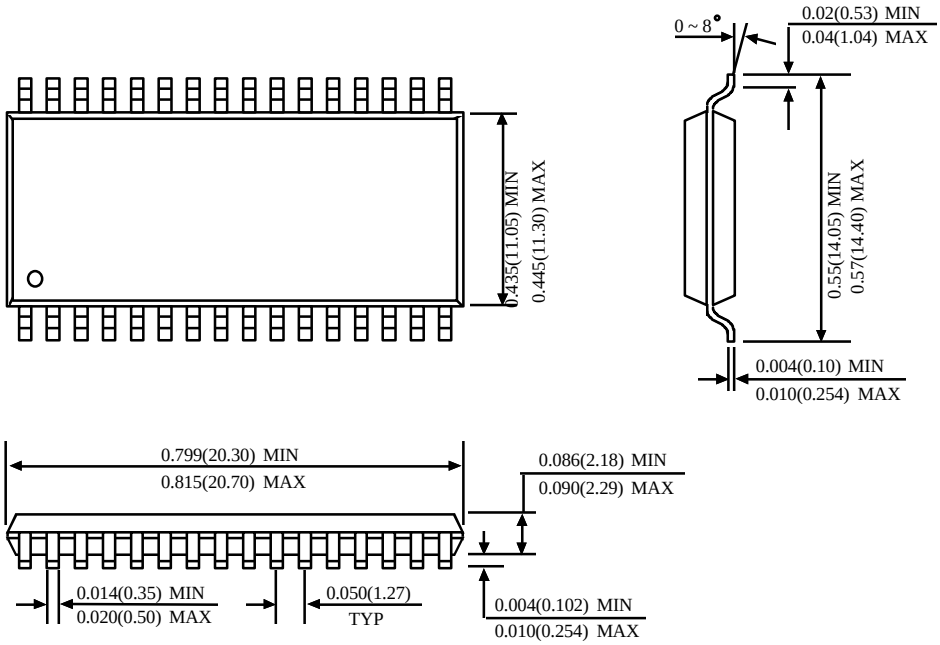
Package Dimensions

Unit: Inches (mm)

32 DIP



32 SOP



32 TSOP I (8x20mm)