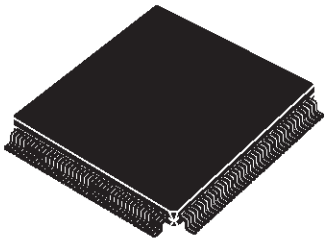
STLC5465B

MULTI-HDLC WITH n x 64 SWITCHING MATRIX ASSOCIATED

- 32 TxHDLCs WITH BROADCASTING CAPABILITY AND/OR CSMA/CR FUNCTION WITH AUTOMATIC RESTART IN CASE OF TX FRAME ABORT
- 32 RxHDLCs INCLUDING ADDRESS RECOGNITION
- 16 COMMAND/INDICATE CHANNELS (4 OR 6-BIT PRIMITIVE)
- 16 MONITOR CHANNELS PROCESSED IN ACCORDANCE WITH GCI OR V*
- 256 x 256 SWITCHING MATRIX WITHOUT BLOCKING AND WITH TIME SLOT SEQUENCE INTEGRITY AND LOOPBACK PER BIDIRECTIONAL CONNECTION
- DMA CONTROLLER FOR 32 Tx CHANNELS AND 32 Rx CHANNELS
- HDLCs AND DMA CONTROLLER ARE CAPABLE OF HANDLING A MIX OF LAPD, LAPB, SS7, CAS AND PROPRIETARY SIGNALLINGS
- EXTERNAL SHARED MEMORY ACCESS BETWEEN DMA CONTROLLER AND MICROPROCESSOR
- SINGLE MEMORY SHARED BETWEEN n x *MULTI-HDLC*s AND SINGLE MICROPROCESSOR ALLOWS TO HANDLE n x 32 CHANNELS
- BUS ARBITRATION
- INTERFACE FOR VARIOUS 8,16 OR 32 BIT MICROPROCESSORS
- RAM CONTROLLER ALLOWS TO INTERFACE UP TO :
  -16 MEGABYTES OF DYNAMIC RAM OR
  -1 MEGABYTE OF STATIC RAM
- INTERRUPT CONTROLLER TO STORE AUTOMATICALLY EVENTS IN SHARED MEMORY
- PQFP160 PACKAGE
- BOUNDARY SCAN FOR TEST FACILITY

DESCRIPTION

The STLC5465B is a Subscriber line interface card controller for Central Office, Central Exchange, NT2 and PBX capable of handling :
- 16 U Interfaces or
- 2 Megabits line interface cards or
- 16 SLICs (Plain Old Telephone Service) or
- Mixed analogue and digital Interfaces (SLICs or U Interfaces) or
- 16 S Interfaces
- Switching Network with centralized processing



PQFP160
(Plastic Quad Flat Pack)

ORDERING NUMBER : STLC5465B

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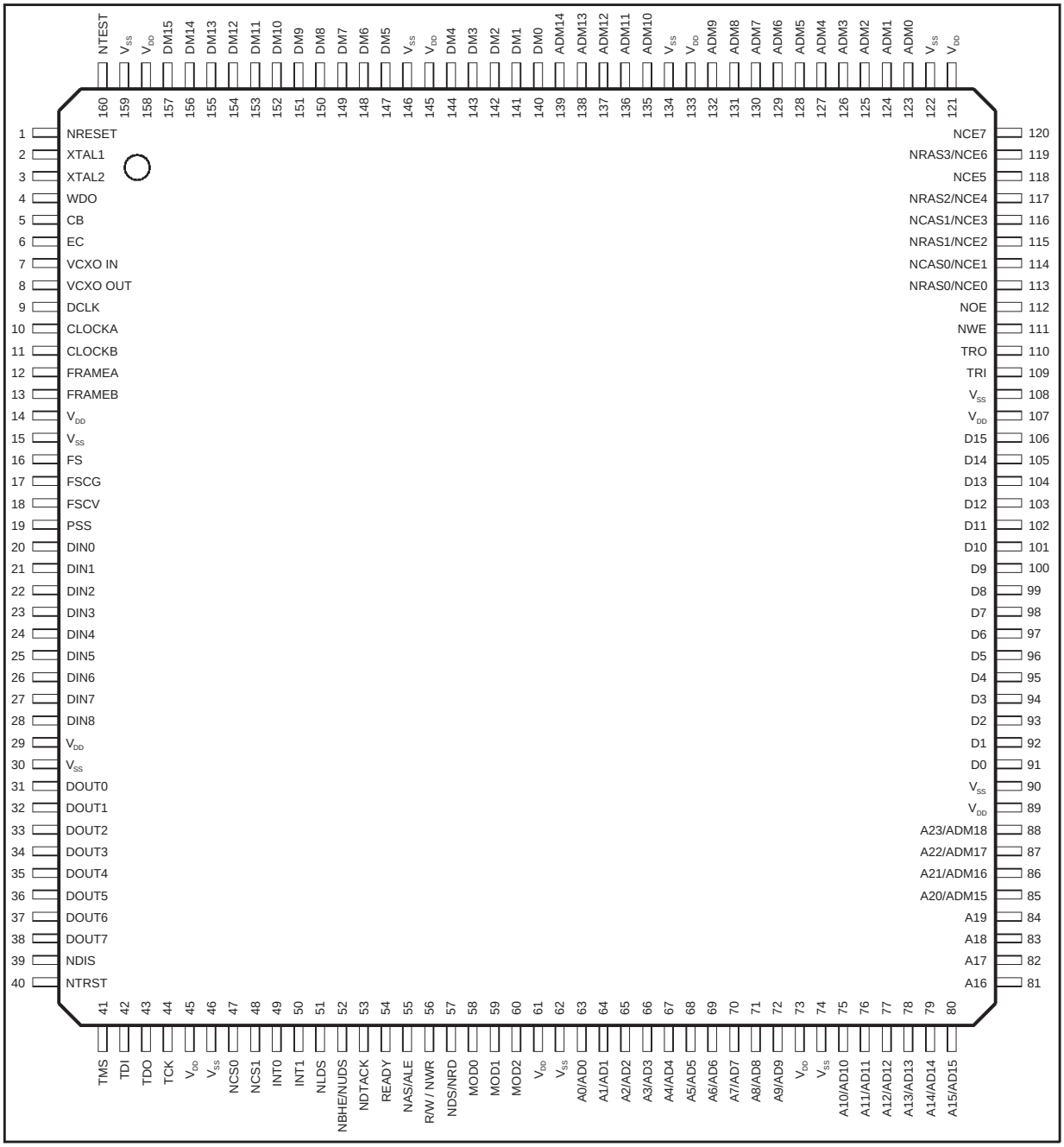
I - PIN INFORMATION

I.1 - Pin Connections



I - PIN INFORMATION (continued)

I.2 - Pin Description

Pin N°	Symbol	Type	Function
POWER PINS (all the power and ground pins must be connected)			
14	V_{DD1}	Power	DC supply
15	V_{SS1}	Ground	DC ground
29	V_{DD2}	Power	DC supply
30	V_{SS2}	Ground	DC ground
45	V_{DD3}	Power	DC supply
46	V_{SS3}	Ground	DC ground
61	V_{DD4}	Power	DC supply
62	V_{SS4}	Ground	DC ground
73	V_{DD5}	Power	DC supply
74	V_{SS5}	Ground	DC ground
89	V_{DD6}	Power	DC supply
90	V_{SS6}	Ground	DC ground
107	V_{DD7}	Power	DC supply
108	V_{SS7}	Ground	DC ground
121	V_{DD8}	Power	DC supply
122	V_{SS8}	Ground	DC ground
133	V_{DD9}	Power	DC supply
134	V_{SS9}	Ground	DC ground
145	V_{DD10}	Power	DC supply
146	V_{SS10}	Ground	DC ground
158	V_{DD11}	Power	DC supply
159	V_{SS11}	Ground	DC ground (Total 22)
CLOCKS			
2	XTAL1	I	Crystal 1. A clock pulse at $f_{Min.}$ = 32000kHz can be applied to this input (or one pin of two crystal pins) with : $-50.10^{-6} < \Delta f < +50.10^{-6}$.
3	XTAL2	O	Crystal 2. If the internal crystal oscillator is used, the second crystal pin is applied to this output.
7	VCXO IN	I3	VCXO input signal. This signal is compared to clock A(or B) selected inside the *Multi-HDLC*.
8	VCXO OUT	O4	VCXO error signal. This pin delivers the result of the comparison.
10	CLOCKA	I3	Input Clock A (4096kHz or 8192kHz)
11	CLOCKB	I3	Input Clock B (4096kHz or 8192kHz)
12	FRAMEA	I3	Clock A at 8kHz
13	FRAMEB	I3	Clock B at 8kHz
9	DCLK	O8	Data Clock issued from Input Clock A (or B). This clock is delivered by the circuit at 4096kHz (or 2048kHz). DOUT0/7 are transmitted on the rising edge of this signal. DIN0/7 are sampled on the falling edge of this signal.
17	FSCG	O8	Frame synchronization for GCI at 8kHz. This clock is issued from FRAME A (or B).
18	FSCV*	O8	Frame synchronization for V Star at 8kHz
16	FS	I3	Frame synchronization.This signal synchronizes DIN0/7 and DOUT0/7.
19	PSS	O8	Programmable synchronization Signal. The PS bit of connection memory is read in real time.

Type : I1 = Input TTL ; I2 = I1 + Pull-up ; I3 = I1 + Hysteresis ; I4 = I3 + Pull-up ;
O4 = Output CMOS 4mA ; O4T = O4 + Tristate ; O8 = Output CMOS 8mA, "1" and "0" at Low Impedance ;
O8D = Output CMOS 8mA, Open Drain ; O8DT = Output CMOS 8mA, Open Drain or Tristate ;
O8T = Output CMOS 8mA, Tristate
I1 and I3 must be connected to VDD and VSS if not used

I - PIN INFORMATION (continued)

I.2 - Pin Description (continued)

Pin N°	Symbol	Type	Function
TIME DIVISION MULTIPLEXES (TDM)			
20	DIN0	I1	TDM0 Data Input 0
21	DIN1	I1	TDM1 Data Input 1
22	DIN2	I1	TDM2 Data Input 2
23	DIN3	I1	TDM3 Data Input 3
24	DIN4	I1	TDM4 Data Input 4
25	DIN5	I1	TDM5 Data Input 5
26	DIN6	I1	TDM6 Data Input 6
27	DIN7	I1	TDM7 Data Input 7
28	DIN8	I1	TDM8 Data Input 8
31	DOUT0	O8DT	TDM0 Data Output 0
32	DOUT1	O8DT	TDM1 Data Output 1
33	DOUT2	O8DT	TDM2 Data Output 2
34	DOUT3	O8DT	TDM3 Data Output 3
35	DOUT4	O8DT	TDM4 Data Output 4
36	DOUT5	O8DT	TDM5 Data Output 5
37	DOUT6	O8DT	TDM6 Data Output 6
38	DOUT7	O8DT	TDM7 Data Output 7
39	NDIS	I1	DOUT 0/7 Not Disable. When this pin is at 0V, the Data Output 0/7 are at high impedance. Wired at VDD if not used.
5	CB	O8D	Contention Bus for CSMA/CR
6	EC	I1	Echo
BOUDARY SCAN			
40	NTRST	I4	Reset for boundary scan
41	TMS	I2	Mode Selection for boundary scan
42	TDI	I2	Input Data for boundary scan
43	TDO	O4	Output Data for boundary scan
44	TCK	I2	Clock for boundary scan
MICROPROCESSOR INTERFACE			
58	MOD0	I1	1 1 0 0 1 1 0
59	MOD1	I1	1 1 0 0 0 0 1
60	MOD2	I1	0 1 1 0 0 1 1
			80C188 80C186 68000 68020 ST9 ST10m ST10Nm
1	NRESET	I3	Circuit Reset
47	NCS0	I3	Chip Select 0 : internal registers are selected
48	NCS1	I3	Chip Select 1 : external memory is selected
49	INT0	O4	Interrupt generated by HDLC, RxC/I or RxMON. Active high.
50	INT1	O4	Interrupt1.This pin goes to 5V when the selected clock A (or B) has disappeared ; 250µs after reset this pin goes to 5V also if clock A is not present.
4	WDO	O4	Watch Dog Output.This pin goes to 5V during 1ms when the microprocessor has not reset the Watch Dog during the programmable time.

Type : I1 = Input TTL ; I2 = I1 + Pull-up ; I3 = I1 + Hysteresis ; I4 = I3 + Pull-up ;
O4 = Output CMOS 4mA ; O4T = O4 + Tristate ; O8 = Output CMOS 8mA, "1" and "0" at Low Impedance ;
O8D = Output CMOS 8mA, Open Drain ; O8DT = Output CMOS 8mA, Open Drain or Tristate ;
O8T = Output CMOS 8mA, Tristate

I - PIN INFORMATION (continued)

I.2 - Pin Description (continued)

Pin N°	Symbol	Type	Function
MICROPROCESSOR INTERFACE (continued)			
51	SIZE0/NLDS	I3	Transfer Size0 (68020)/Lower Data Strobe (68000)
52	SIZE1/NBHE/NUDS	I3	Transfer Size1 (68020)/Bus High Enable (Intel) / Upper Data Strobe (68000)
53	NDSACK0/NDTACK	O8T	Data Strobe, Acknowledge and Size0 (68020)/Data Transfer Acknowledge (68000)
54	NDSACK1/READY	O8T	Data Strobe, Acknowledge and Size0 (68020)/Data Transfer Acknowledge (Intel)
55	NAS/ALE	I3	Address Strobe(Motorola) / Addresss Latch Enable(Intel)
56	R/W / NWR	I3	Read/Write (Motorola / Write(Intel)
57	NDS/NRD	I3	Data Strobe (Motorola 68020); at Vdd for 68000/Read Data (Intel)
63	A0/AD0	I/O	Address bit 0 (Motorola 68020); at Vdd for 68000 / Address/Data bit 0 (Intel)
64	A1/AD1	I/O	Address bit 1 (Motorola) / Address/Data bit 1 (Intel)
65	A2/AD2	I/O	Address bit 2 (Motorola) / Address/Data bit 2 (Intel)
66	A3/AD3	I/O	Address bit 3 (Motorola) / Address/Data bit 3 (Intel)
67	A4/AD4	I/O	Address bit 4 (Motorola) / Address/Data bit 4 (Intel)
68	A5/AD5	I/O	Address bit 5 (Motorola) / Address/Data bit 5 (Intel)
69	A6/AD6	I/O	Address bit 6 (Motorola) / Address/Data bit 6 (Intel)
70	A7/AD7	I/O	Address bit 7 (Motorola) / Address/Data bit 7 (Intel)
71	A8/AD8	I/O	Address bit 8 (Motorola) / Address/Data bit 8 (Intel)
72	A9/AD9	I/O	Address bit 9 (Motorola) / Address/Data bit 9 (Intel)
75	A10/AD10	I/O	Address bit 10 (Motorola) / Address/Data bit 10 (Intel)
76	A11/AD11	I/O	Address bit 11 (Motorola) / Address/Data bit 11 (Intel)
77	A12/AD12	I/O	Address bit 12 (Motorola) / Address/Data bit 12 (Intel)
78	A13/AD13	I/O	Address bit 13 (Motorola) / Address/Data bit 13 (Intel)
79	A14/AD14	I/O	Address bit14 (Motorola) / Address/Data bit 14 (Intel)
80	A15/AD15	I/O	Address bit15 (Motorola) / Address/Data bit 15 (Intel)
81	A16	I1	Address bit16 (Motorola) / Address bit 16 (Intel)
82	A17	I1	Address bit17 (Motorola) / Address bit 17 (Intel)
83	A18	I1	Address bit18 (Motorola) / Address bit 18 (Intel)
84	A19	I1	Address bit19 (Motorola) / Address bit 19 (Intel)
85	A20/ADM15	I/O	Address bit 20 from µP (input) / Address bit 15 for SRAM (output)
86	A21/ADM16	I/O	Address bit 21 from µP (input) / Address bit 16 for SRAM (output)
87	A22/ADM17	I/O	Address bit 22 from µP (input) / Address bit 17 for SRAM (output)
88	A23/ADM18	I/O	Address bit 23 from µP (input) / Address bit 18 for SRAM (output)
91	DO	I/O	Data bit 0 for µP if not multiplexed (see Note 1).
92	D1	I/O	Data bit 1 for µP if not multiplexed
93	D2	I/O	Data bit 2 for µP if not multiplexed
94	D3	I/O	Data bit 3 for µP if not multiplexed
95	D4	I/O	Data bit 4 for µP if not multiplexed
96	D5	I/O	Data bit 5 for µP if not multiplexed
97	D6	I/O	Data bit 6 for µP if not multiplexed
98	D7	I/O	Data bit 7 for µP if not multiplexed
99	D8	I/O	Data bit 8 for µP if not multiplexed

Type : I1 = Input TTL ; I2 = I1 + Pull-up ; I3 = I1 + Hysteresis ; I4 = I3 + Pull-up ;
O4 = Output CMOS 4mA ; O4T = O4 + Tristate ; O8 = Output CMOS 8mA, "1" and "0" at Low Impedance ;
O8D = Output CMOS 8mA, Open Drain ; O8DT = Output CMOS 8mA, Open Drain or Tristate ;
O8T = Output CMOS 8mA, Tristate

I - PIN INFORMATION (continued)

I.2 - Pin Description (continued)

Pin N°	Symbol	Type	Function
MICROPROCESSOR INTERFACE (continued)			
100	D9	I/O	Data bit 9 for µP if not multiplexed
101	D10	I/O	Data bit 10 for µP if not multiplexed
102	D11	I/O	Data bit 11 for µP if not multiplexed
103	D12	I/O	Data bit 12 for µP if not multiplexed
104	D13	I/O	Data bit 13 for µP if not multiplexed
105	D14	I/O	Data bit 14 for µP if not multiplexed
106	D15	I/O	Data bit 15 for µP if not multiplexed
MEMORY INTERFACE			
109	TRI	I3	Token Ring Input (for use *Multi-HDLC*s in cascade)
110	TRO	O4	Token Ring Output (for use *Multi-HDLC*s in cascade)
111	NWE	O4T	Write Enable for memory circuits
112	NOE	O4T	Control Output Enable for memory circuits
113	NRAS0/NCE0	O4T	Row Address Strobe Bank 0 / Chip Enable 0 for SRAM
114	NCAS0/NCE1	O4T	Column Address Strobe Bank 0 / Chip Enable1 for SRAM
115	NRAS1/NCE2	O4T	Row Address Strobe Bank 1 / Chip Enable 2 for SRAM
116	NCAS1/NCE3	O4T	Column Address Strobe Bank 1 / Chip Enable 3 for SRAM
117	NRAS2/NCE4	O4T	Row Address Strobe Bank 2 / Chip Enable 4 for SRAM
118	NCE5	O4T	Chip Enable 5 for SRAM
119	NRAS3/NCE6	O4T	Row Address Strobe Bank 3 / Chip Enable 6 for SRAM
120	NCE7	O4T	Chip Enable 7 for SRAM
123	ADM0	O8T	Address bit 0 for SRAM and DRAM
124	ADM1	O8T	Address bit 1 for SRAM and DRAM
125	ADM2	O8T	Address bit 2 for SRAM and DRAM
126	ADM3	O8T	Address bit 3 for SRAM and DRAM
127	ADM4	O8T	Address bit 4 for SRAM and DRAM
128	ADM5	O8T	Address bit 5 for SRAM and DRAM
129	ADM6	O8T	Address bit 6 for SRAM and DRAM
130	ADM7	O8T	Address bit 7 for SRAM and DRAM
131	ADM8	O8T	Address bit 8 for SRAM and DRAM
132	ADM9	O8T	Address bit 9 for SRAM and DRAM
135	ADM10	O8T	Address bit 10 for SRAM and DRAM
136	ADM11	O8T	Address bit 11 for SRAM only
137	ADM12	O8T	Address bit 12 for SRAM only
138	ADM13	O8T	Address bit 13 for SRAM only
139	ADM14	O8T	Address bit 14 for SRAM only

Type : I1 = Input TTL ; I2 = I1 + Pull-up ; I3 = I1 + Hysteresis ; I4 = I3 + Pull-up ;
O4 = Output CMOS 4mA ; O4T = O4 + Tristate ; O8 = Output CMOS 8mA, "1" and "0" at Low Impedance ;
O8D = Output CMOS 8mA, Open Drain ; O8DT = Output CMOS 8mA, Open Drain or Tristate ;
O8T = Output CMOS 8mA, Tristate

I - PIN INFORMATION (continued)

I.2 - Pin Description (continued)

Pin N°	Symbol	Type	Function
MEMORY INTERFACE (continued)			
140	DM0	I/O	Memory Data bit 0
141	DM1	I/O	Memory Data bit 1
142	DM2	I/O	Memory Data bit 2
143	DM3	I/O	Memory Data bit 3
144	DM4	I/O	Memory Data bit 4
147	DM5	I/O	Memory Data bit 5
148	DM6	I/O	Memory Data bit 6
149	DM7	I/O	Memory Data bit 7
150	DM8	I/O	Memory Data bit 8
151	DM9	I/O	Memory Data bit 9
152	DM10	I/O	Memory Data bit 10
153	DM11	I/O	Memory Data bit 11
154	DM12	I/O	Memory Data bit 12
155	DM13	I/O	Memory Data bit 13
156	DM14	I/O	Memory Data bit 14
157	DM15	I/O	Memory Data bit 15
160	NTEST	I2	Test Control. When this pin is at 0V each output is high impedance except XTAL2 Pin.

Type : I1 = Input TTL ; I2 = I1 + Pull-up ; I3 = I1 + Hysteresis ; I4 = I3 + Pull-up ;
O4 = Output CMOS 4mA ; O4T = O4 + Tristate ; O8 = Output CMOS 8mA, "1" and "0" at Low Impedance ;
O8D = Output CMOS 8mA, Open Drain ; O8DT = Output CMOS 8mA, Open Drain or Tristate ;
O8T = Output CMOS 8mA, Tristate

Note : D0/15 input/output pins must be connected to one single external pull up resistor if not used.

I.3 - Pin Definition

I.3.1 - Input Pin Definition

I1 : Input 1 TTL
I2 : Input 2 TTL + pull-up
I3 : Input 3 TTL + hysteresis
I4 : Input 4 TTL + hysteresis +pull-up

I.3.2 - Output Pin Definition

O4 : Output CMOS 4mA
O4T : Output CMOS 4mA, Tristate
O8 : Output CMOS 8mA
O8T : Output CMOS 8mA,Tristate
O8D : Output CMOS 8mA,Open Drain
O8DT : Output CMOS 8mA,Open Drain or Tristate (Programmable pin)

Moreover, each output is high impedance when the NTEST Pin is at 0 volt except XTAL2 Pin which is a CMOS output.

I.3.3 - Input/Output Pin Definition

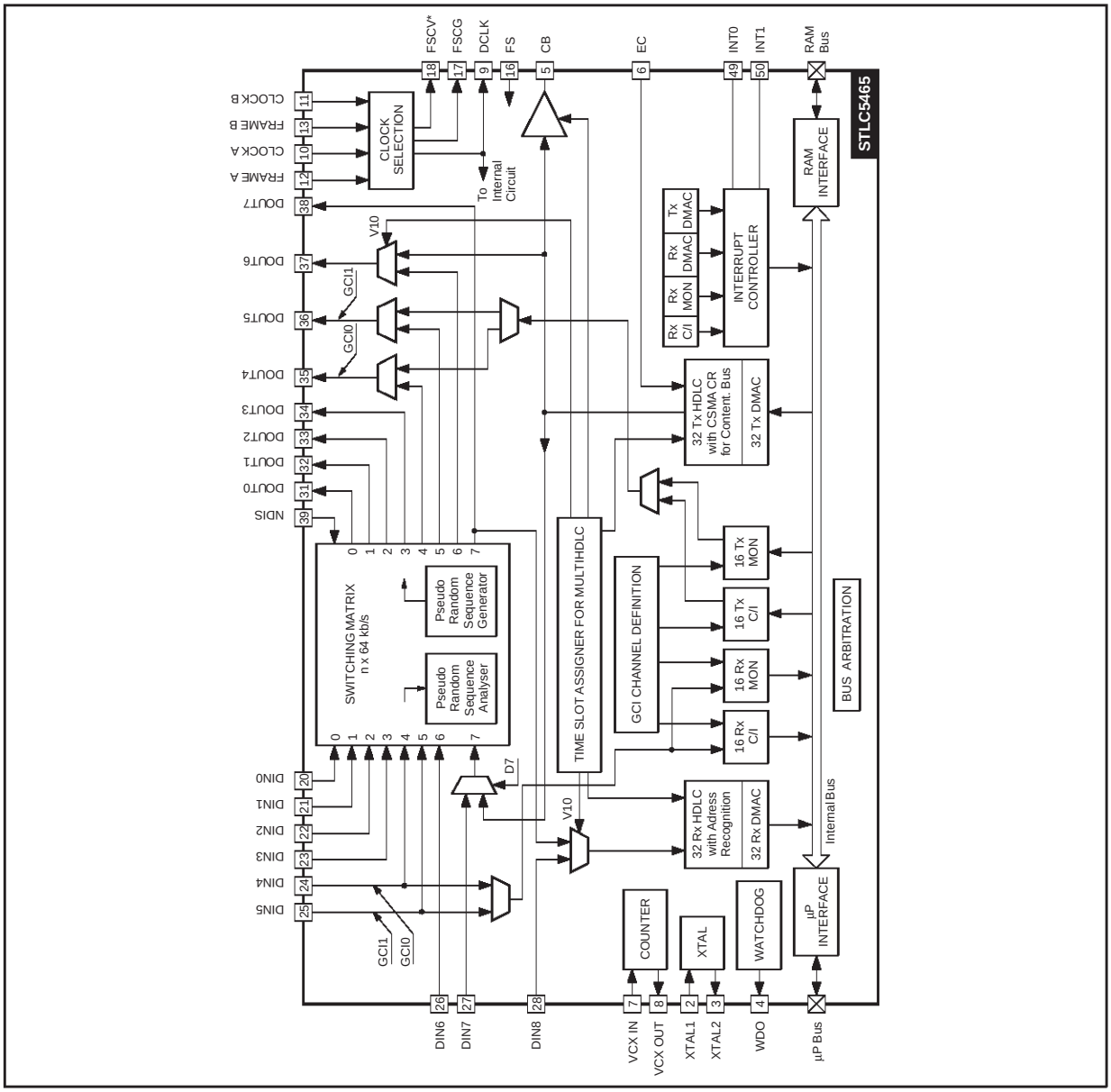
I/O : Input TTL/ Output CMOS 8mA.

N.B. XTAL1 : this input is CMOS.
XTAL2 : NTEST pin at 0 has no effect on this pin.

II - BLOCK DIAGRAM

The top level functionalities of *Multi-HDLC* appear on the general block diagram.

Figure 1 : General Block Diagram



There are :

- The switching matrix,
- The time slot assigner,
- The 32 HDLC transmitters with associated DMA controllers,
- The 32 HDLC receivers with associated DMA controllers,
- The 16 Command/Indicate and Monitor Channel transmitters belonging to two General Component Interfaces (GCI),
- The 16 Command/Indicate and Monitor Channel receivers belonging to two General Component Interfaces (GCI),
- The memory interface,
- The microprocessor interface,
- The bus arbitration,
- The clock selection and time synchronization function,
- The interrupt controller,
- The watchdog,
- The boundary scan.

III - FUNCTIONAL DESCRIPTION

III.1 - The Switching Matrix N x 64 KBits/S

III.1.1 - Function Description

The matrix performs a non-blocking switch of 256 time slots from 8 Input Time Division Multiplex (TDM) at 2 Mbit/s to 8 output Time Division Multiplex. A TDM is composed of 32 Time Slots (TS) at 64 kbit/s. The matrix is designed to switch a 64 kbit/s channel (Variable delay mode) or an hyperchannel of data (Sequence integrity mode). So, it will both provide minimum throughput switching delay for voice applications and time slot sequence integrity for data applications on a per channel basis.

The requirements of the Sequence Integrity (n*64 kbit/s) mode are the following:

All the time slots of a given input frame must be put out during a same output frame.

The time slots of an hyperchannel (concatenation of TS in the same TDM) are not crossed together at output in different frames.

In variable delay mode, the time slot is put out as soon as possible. (The delay is two or three time slots minimum between input and output).

For test facilities, any time slot of an Output TDM (OTDM) can be internally looped back into the same Input TDM number (ITDM) at the same time slot number.

A Pseudo Random Sequence Generator and a Pseudo Random Sequence Analyzer are implemented in the matrix. They allow the generation a sequence on a channel or on a hyperchannel, to analyse it and verify its integrity after several switching in the matrix or some passing of the sequence across different boards.

The Frame Signal (FS) synchronises ITDM and OTDM but a programmable delay or advance can be introduced separately on each ITDM and OTDM (a half bit time, a bit time or two bit times).

An additional pin (PSS) permits the generation of a programmable signal composed of 256 bits per frame at a bit rate of 2048 kbit/s.

An external pin (NDIS) asserts a high impedance on all the TDM outputs of the matrix when active (during the initialization of the board for example).

III.1.2 - Architecture of the Matrix

The matrix is essentially composed of buffer data memories and a connection memory.

The received serial data is first converted to parallel by a serial to parallel converter and stored consecutively in a 256 position Buffer Data Memory (see Figure 2 on Page 16).

To satisfy the Sequence Integrity (n*64 kbit/s) requirements, the data memory is built with an even memory, an odd memory and an output memory. Two consecutive frames are stored alternatively in the odd and even memory. During the time an input frame is stored, the one previously stored is transferred into the output memory according to the connection memory switching orders. A frame later, the output memory is read and data is converted to serial and transferred to the output TDM.

III.1.3 - Connection Function

Two types of connections are offered :
- unidirectional connection and
- bidirectional connection.

An unidirectional connection makes only the switch of an input time slot through an output one whereas a bidirectional connection establishes the link in the other direction too. So a double connection can be achieved by a single command (see Figure 3 on Page 17).

III.1.4 - Loop Back Function

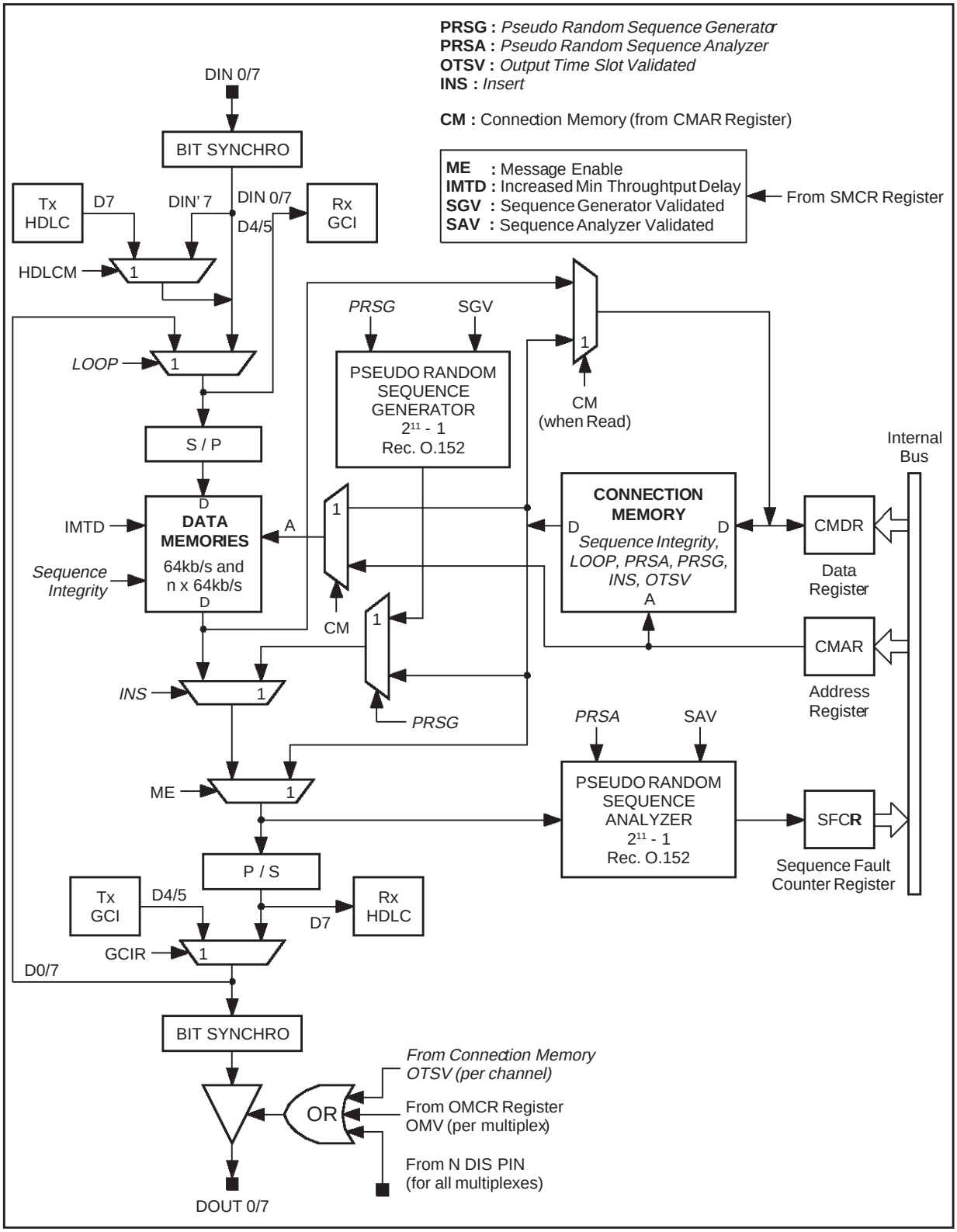
Any time slot of an Output TDM can be internally looped back on the time slot which has the same TDM number and the same TS number

(OTDMi, TSj) ----> (ITDMi, TSj).

In the case of a bidirectional connection, only the one specified by the microprocessor is concerned by the loop back (see Figure 4 on Page 17).

III - FUNCTIONAL DESCRIPTION (continued)

Figure 2 : Switching Matrix Data Path



III - FUNCTIONAL DESCRIPTION (continued)

Figure 3 : Unidirectional and Bidirectional Connections

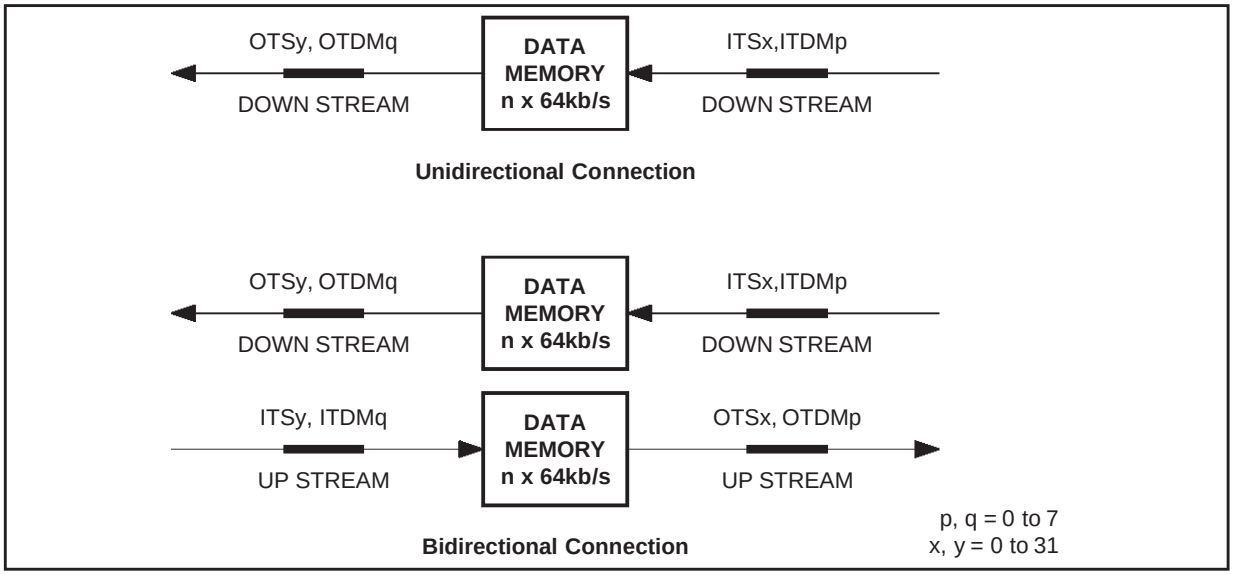
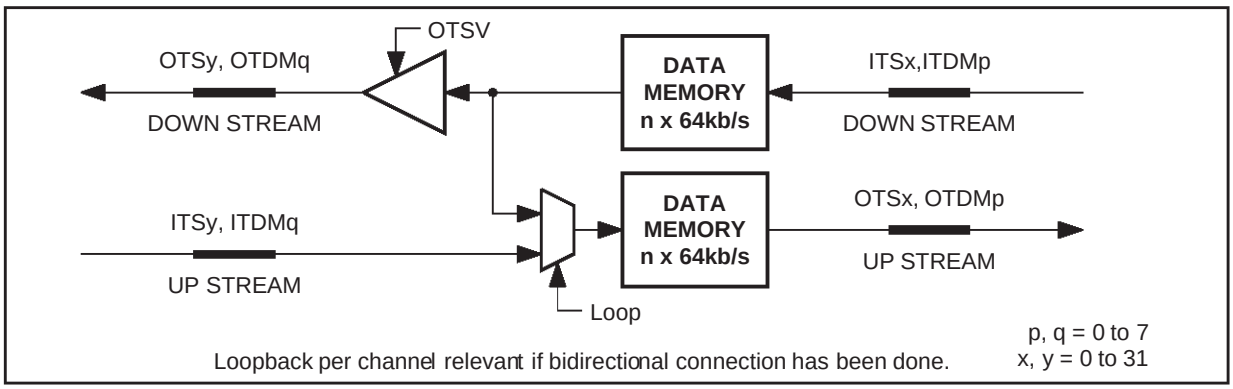


Figure 4 : Loop Back



III.1.5 - Delay through the Matrix

III.1.5.1 - Variable Delay Mode

In the variable delay mode, the delay through the matrix depends on the relative positions of the input and output time slots in the frame.

So, some limits are fixed :

- the maximum delay is a frame + 2 time slots,
- the minimum delay is programmable.
  Three time slots if IMTD = 1, in this case n = 2 in the formula hereafter or two time slots if IMTD = 0, in this case n = 1 in the same formula (see Paragraph "Switching Matrix Configuration Reg SMCR (0C)H" on Page 64).

All the possibilities can be ranked in three cases :

a) If OTSy > ITSx + n then the variable delay is :

OTSy - ITSx Time slots

b) If ITSx < OTSy < ITSx + n then the variable delay is :

OTSy - ITSx + 32 Time slots

c) OTSy < ITSx then the variable delay is :

32 - (ITSx - OTSy) Time slots.

N.B. Rule b) and rule c) are identical.

For n = 1 and n = 2, see Figure 5 on Page 18.

III.1.5.2 - Sequence Integrity Mode

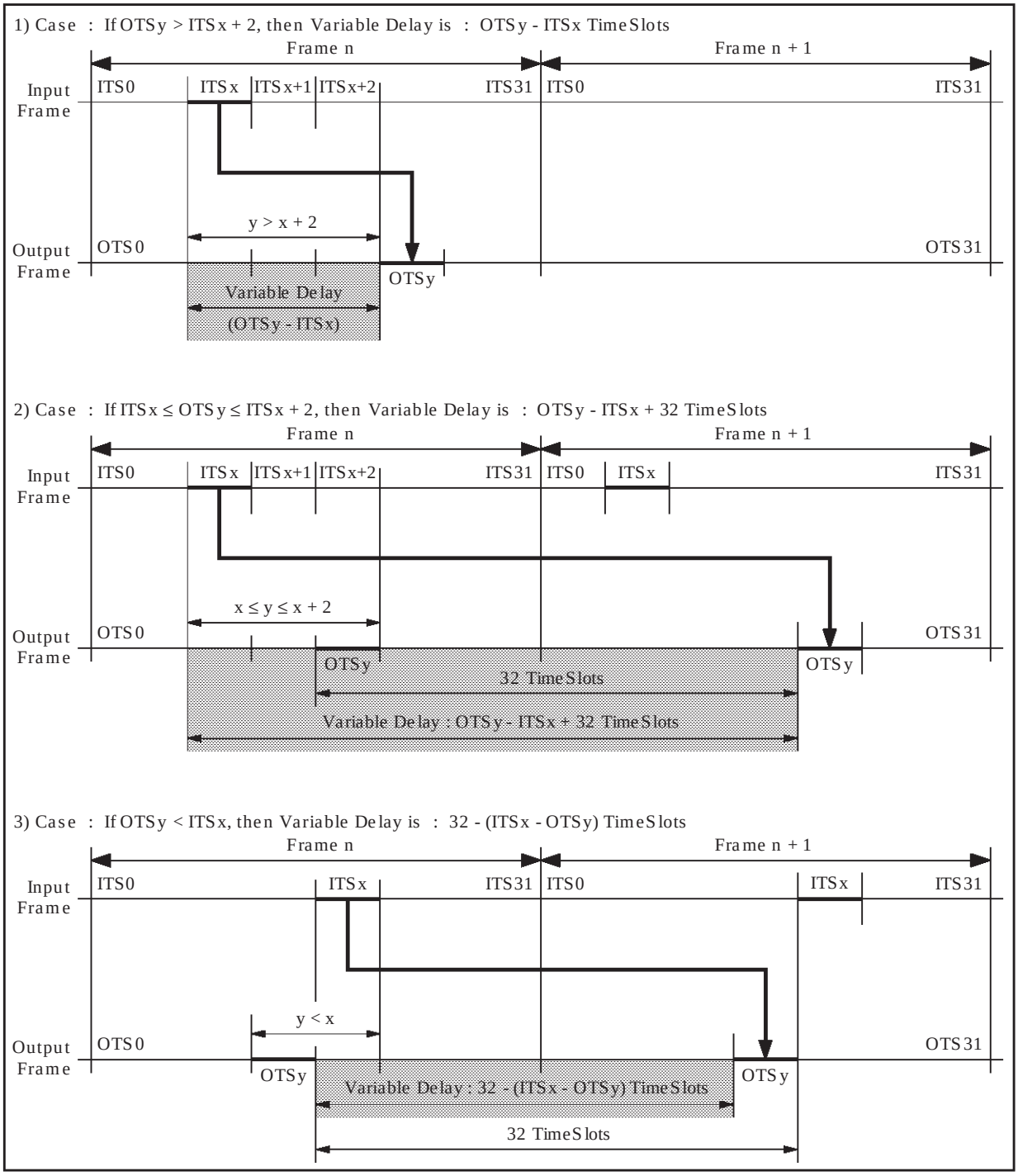
In the sequence integrity mode (SI = 1, bit located in the Connection Memory), the input time slots are put out 2 frames later (fig. 6 - page 19). In this case, the delay is defined by a single expression :

Constant Delay = (32 - ITSx) + 32 + OTSy

So, the delay in sequence integrity mode varies from 33 to 95 time slots.

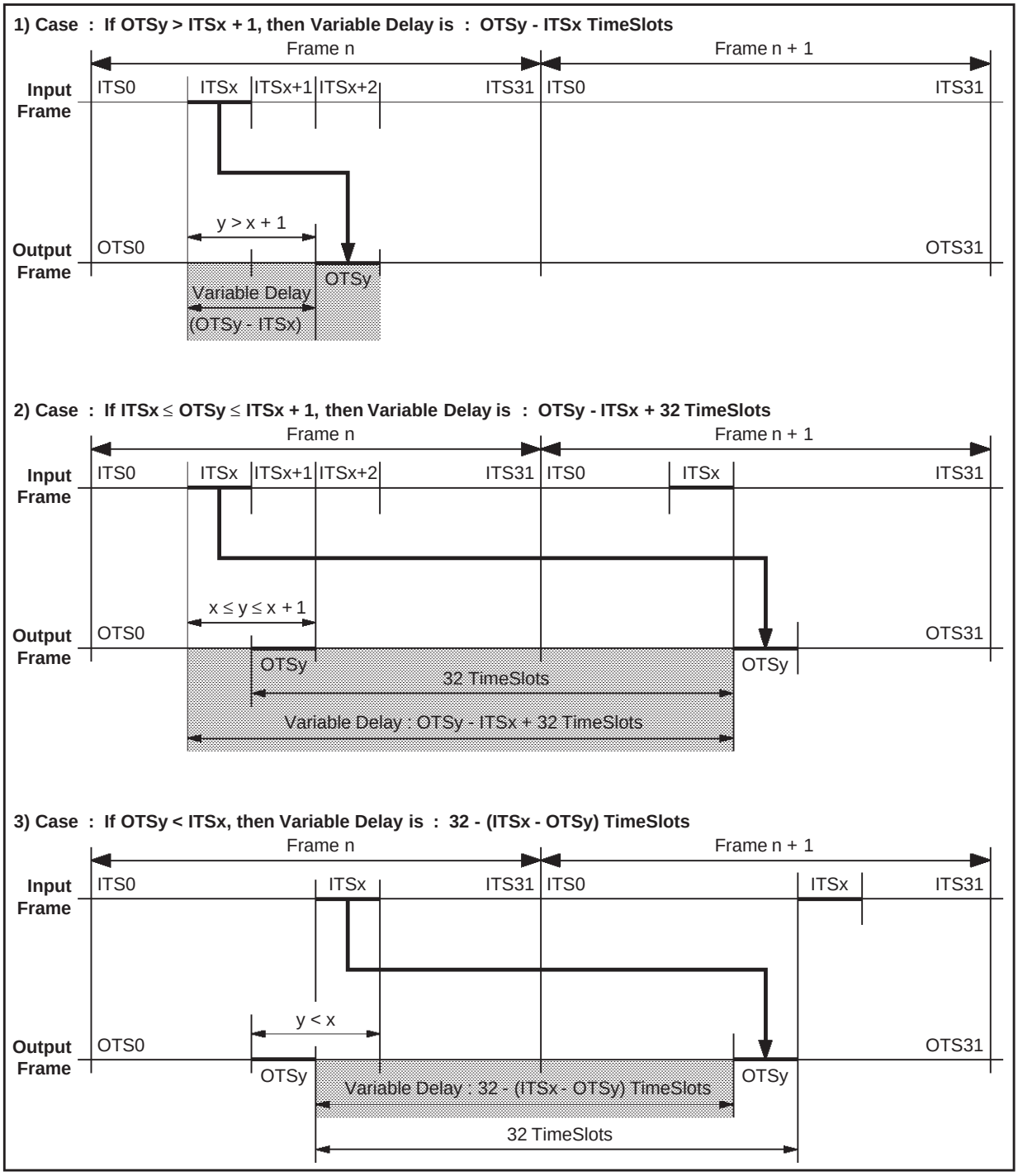
III - FUNCTIONAL DESCRIPTION (continued)

Figure 5 : Variable Delay through the matrix with ITDM = 1



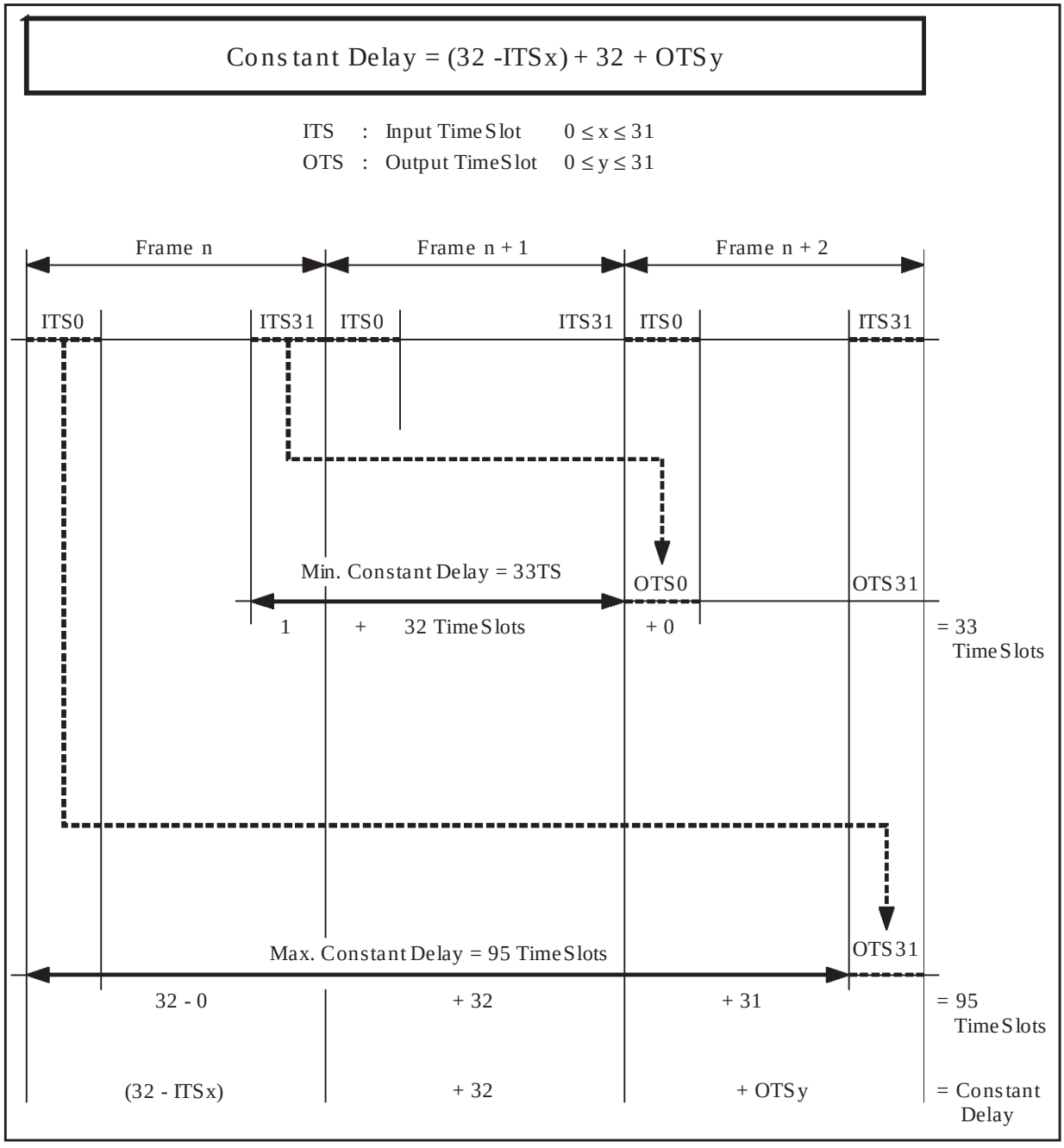
III - FUNCTIONAL DESCRIPTION (continued)

Figure 6: Variable Delay through the matrix with ITDM = 0



III - FUNCTIONAL DESCRIPTION (continued)

Figure 7 : Constant Delay through the matrix with SI = 1



III - FUNCTIONAL DESCRIPTION (continued)

III.1.6 - Connection Memory

III.1.6.1 - Description

The connection memory is composed of 256 locations addressed by the number of OTDM and TS (8x32).

Each location permits :

- to connect each input time slot to one output time slot (If two or more output time slots are connected to the same input time slot number, there is broadcasting).
- to select the variable delay mode or the sequence integrity mode for any time slot.
- to loop back an output time slot. In this case the contents of an input time slot (ITSx, ITDMp) is the same as the output time slot (OTSx,OTDMp).
- to output the contents of the corresponding connection memory instead of the data which has been stored in data memory.
- to output the sequence of the pseudo random sequence generator on an output time slot: a pseudo random sequence can be inserted in one or several time slots (hyperchannel) of the same Output TDM ; this insertion must be enabled by the microprocessor in the configuration register of the matrix.
- to define the source of a sequence by the pseudo random sequence analyzer: a pseudo random sequence can be extracted from one or several time slots (hyperchannel) of the same Input TDM and routed to the analyzer; this extraction can be enabled by the microprocessor in the configuration register of the matrix (SMCR).
- to assert a high impedance level on an output time slot (disconnection).
- to deliver a programmable 256-bit sequence during 125 microseconds on the Programmable synchronization Signal pin (PSS).

III.1.6.2 - Access to Connection Memory

Supposing that the Switching Matrix Configuration Register (SMCR) has been already written by the microprocessor, it is possible to access to the connection memory from microprocessor with the help of two registers :

- Connection Memory Data Register (CMDR) and
- Connection Memory Address Register (CMAR).

III.1.6.3 - Access to Data Memory

To extract the contents of the data memory it is possible to read the data memory from microprocessor with the help of the two registers :

- Connection Memory Data Register (CMDR) and
- Connection Memory Address Register (CMAR).

III.1.6.4 - Switching at 32 Kbit/s

Four TDMs can be programmed individually to carry 64 channels at 32 Kbit/s (only if these TDMs are at 2 Mbit/s).

Two bits (SW0/1) located in SMCR define the type of channels of two couples of TDMs.

SW0 defines TDM0 and TDM4 (GCI0) and SW1 defines TDM1 and TDM5 (GCI1). If TDM0 or/and TDM1 carry 64 channels at 32 Kbit/s then TDM2 or/and TDM3 are not available externally they are used internally to perform the function.

Downstream switching at 32 kb/s on page 22.

Upstream switching at 32 kb/s on page 23.

III.1.6.5 - Switching at 16 kbit/s

The TDM4 and TDM5 can be GCI multipexes. Each GCI multipex comprises 8 GCI channels. Each GCI channel comprises one D channel at 16 Kbit/s. See GCI channel definition GCI Synchro signal delivered by the Multi-HDLC on page 30.

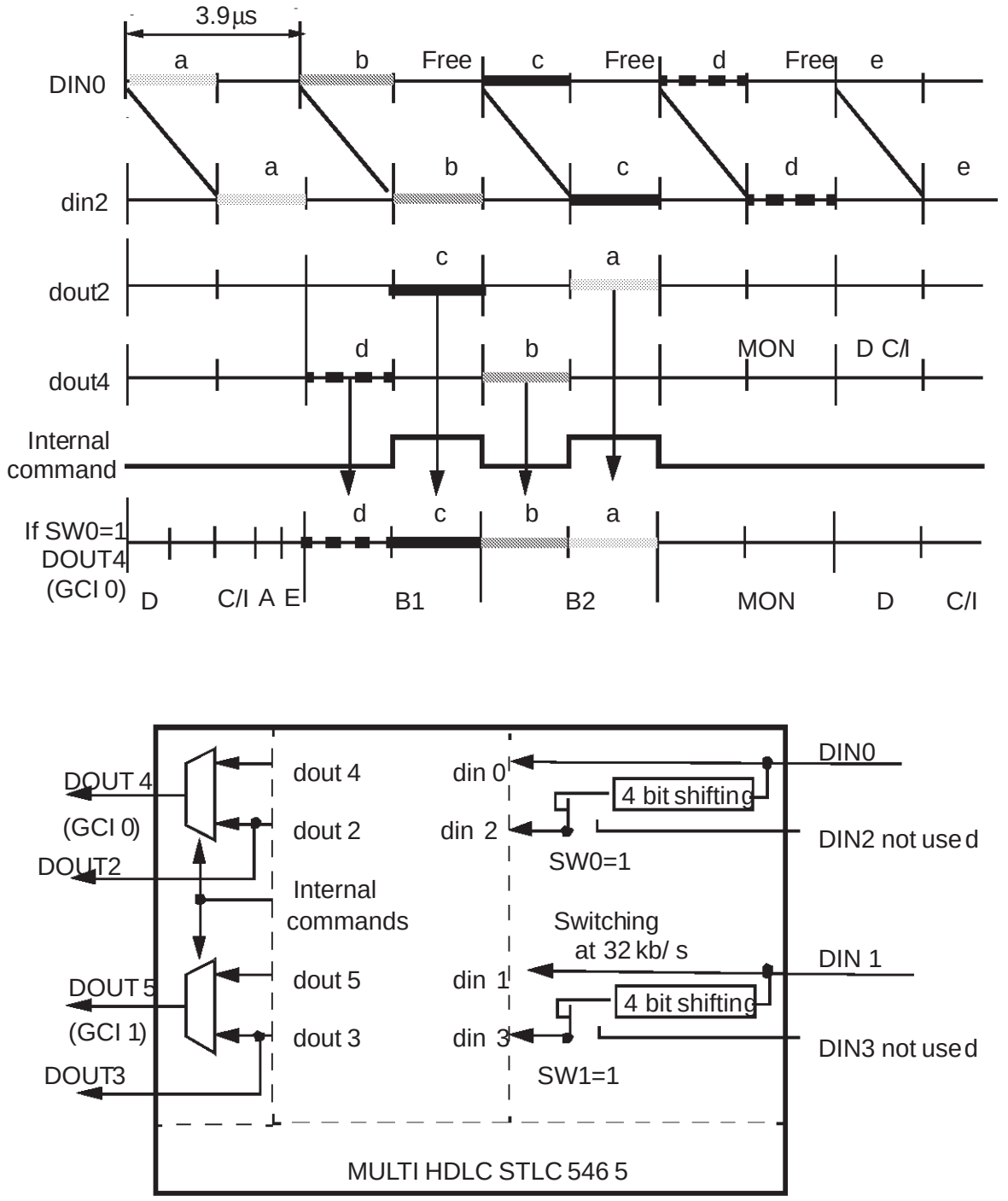
It is possible to switch the contents of 16 D channels from the 16 GCI channels to 4 timeslots of the 256 output timeslots.

In the other direction the contents of an selected timeslot is automatically switched to 4 D channels at 16 Kbit/s.

See Connection Memory Data Register CMDR $(0E)_H$ on page 74

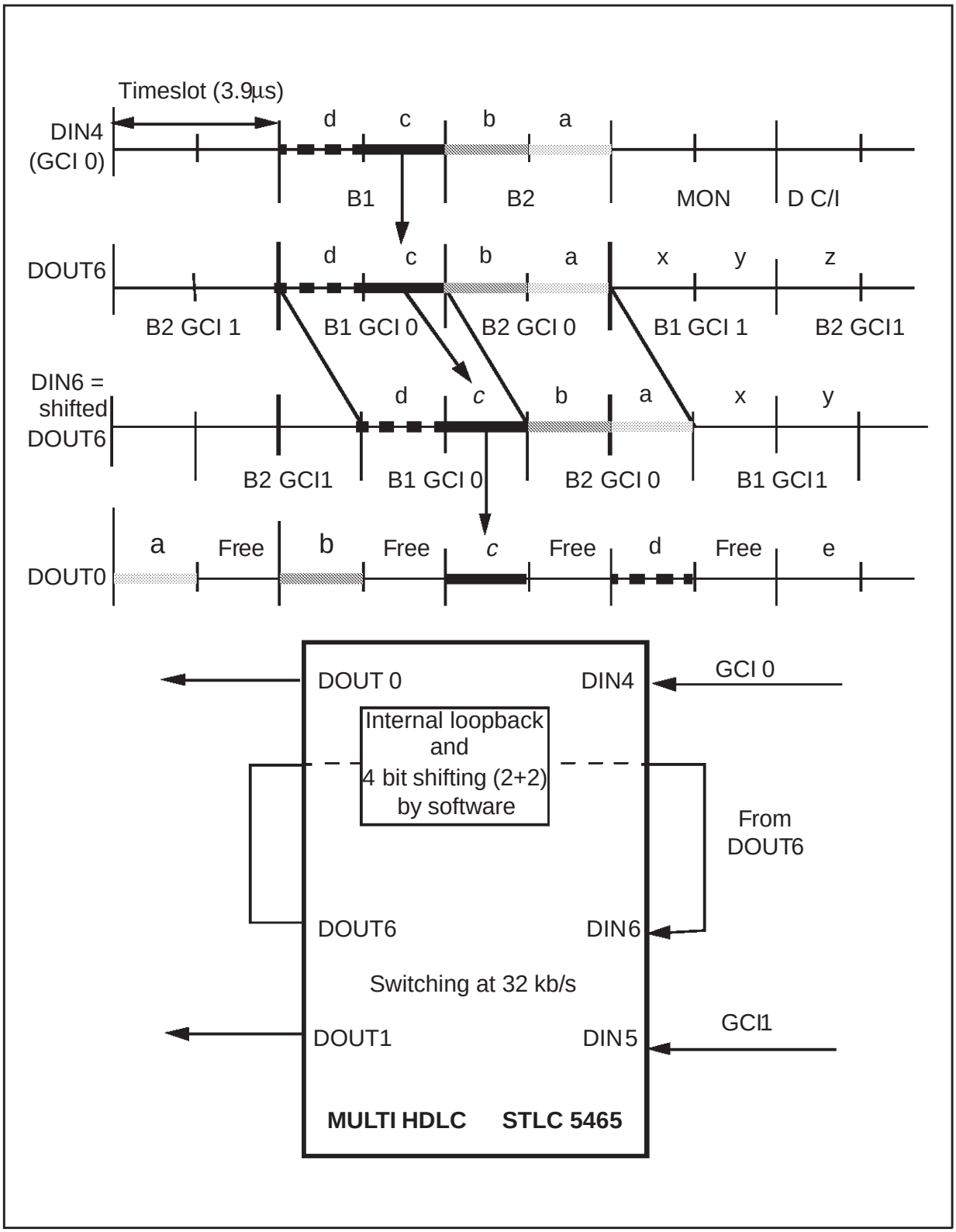
III - FUNCTIONAL DESCRIPTION (continued)

Figure 8: Downstream Switching at 32kb/s



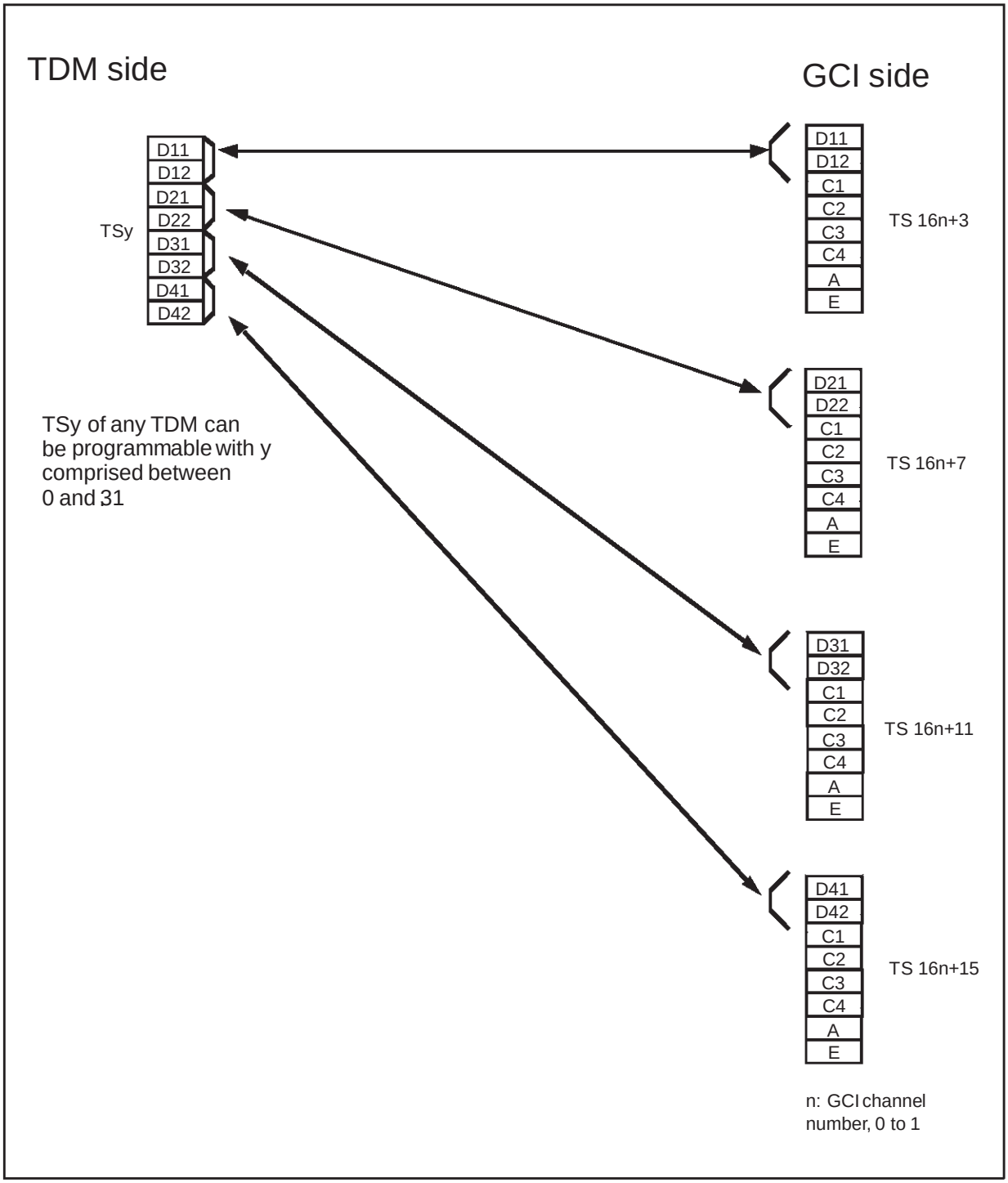
III - FUNCTIONAL DESCRIPTION (continued)

Figure 9: Upstream Switching at 32kb/s



III - FUNCTIONAL DESCRIPTION (continued)

Figure 10: Upstream and Downstream Switching at 16kb/s



III - FUNCTIONAL DESCRIPTION (continued)

III.2 - HDLC Controller

III.2.1 - Function Description

The internal HDLC controller can run up to 32 channels in a conventional HDLC mode or in a transparent (non-HDLC) mode (configurable per channel).

Each channel bit rate is programmable from 4kbit/s to 64kbit/s. All the configurations are also possible from 32 channels (from 4 to 64 kbit/s) to one channel at 2 Mbit/s.

In reception, the HDLC time slots can directly come from the input TDM DIN8 (direct HDLC Input) or from any other TDM input after switching towards the output 7 of the matrix (configurable per time slot).

In transmission, the HDLC frames are sent on the output DOUT6 and on the output CB (with or without contention mechanism), or are switched towards the other TDM output via the input 7 of the matrix (see Figure 11).

III.2.1.1 - Format of the HDLC Frame

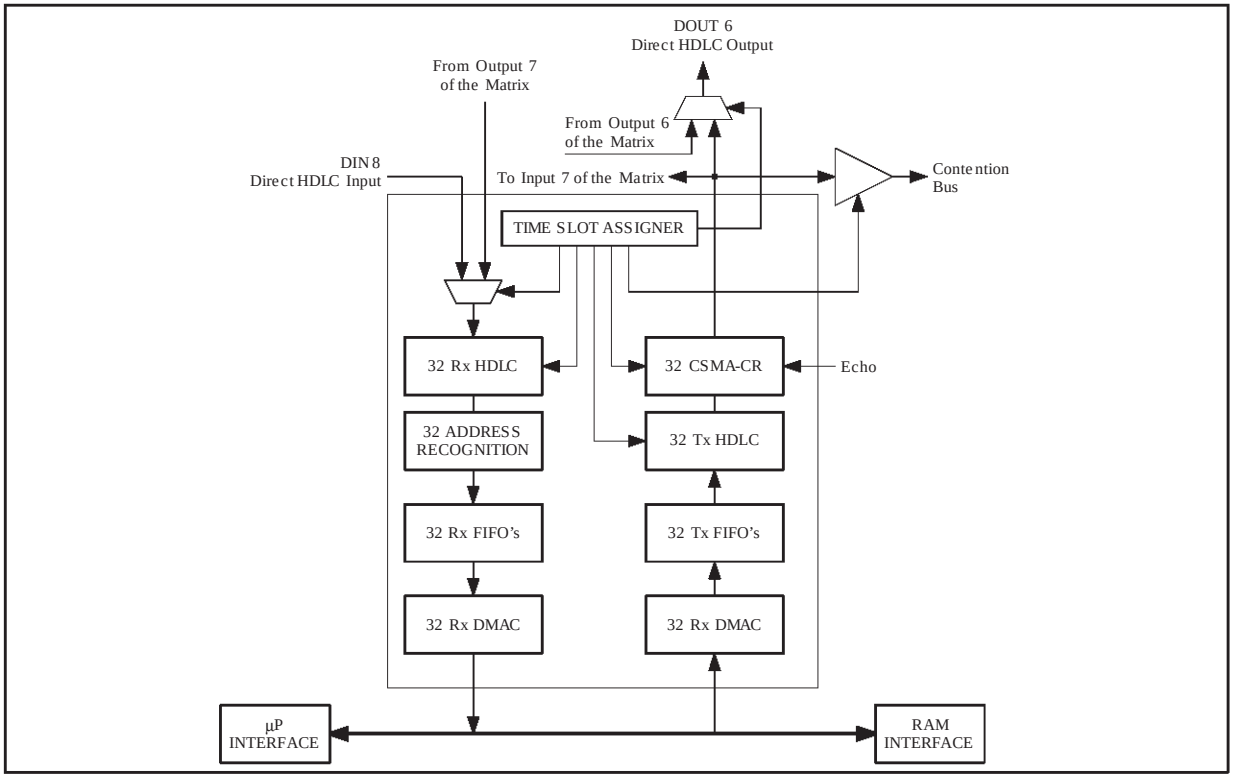
The format of an HDLC frame is the same in receive and transmit direction and shown here after.

III.2.1.2 - Composition of an HDLC Frame

Opening Flag
Address Field (first byte)
Address Field (second byte)
Command Field (first byte)
Command Field (second byte)
Data (first byte) Data (optional)
Data (last byte)
FCS (first byte)
FCS (second byte)
Closing Flag

- Opening Flag
- One or two bytes for address recognition (reception) and insertion (transmission)
- Data bytes with bit stuffing
- Frame Check Sequence: CRC with polynomial $G(x) = x^{16} + x^{12} + x^5 + 1$
- Closing Flag.

Figure 11 : HDLC and DMA Controller Block Diagram



III - FUNCTIONAL DESCRIPTION (continued)

III.2.1.3 - Description and Functions of the HDLC Bytes

- FLAG
  The binary sequence 01111110 marks the beginning and the end of the HDLC Frame.
  Note : In reception, three possible flag configurations are allowed and correctly detected :
  - two normal consecutive flags :
    ...0111111001111110...
  - two consecutive flags with a "0" common :
    ...01111110111111 10...
  - a global common flag : ...01111110...
  this flag is the closing flag for the current frame and the opening flag for the next frame
- ABORT
  The binary sequence 1111111 marks an Abort command.
  In reception, seven consecutive 1's, inside a message, are detected as an abort command and generates an interrupt to the host.
  In transmit direction, an abort is sent upon command of the micro-processor. No ending flag is expected after the abort command.
- BIT STUFFING AND UNSTUFFING
  This operation is done to avoid the confusion of a data byte with a flag.
  In transmission, if five consecutive 1's appear in the serial stream being transmitted, a zero is automatically inserted (bit stuffing) after he fifth "1".
  In reception, if five consecutive "1" followed by a zero are received, the "0" is assumed to have been inserted and is automatically deleted (bit unstuffing).
- FRAME CHECK SEQUENCE
  The Frame Check Sequence is calculated according to the recommendation Q921 of the CCITT.
- ADDRESS RECOGNITION
  In the frame, one or two bytes are transmitted to indicate the destination of the message.
  Two types of addresses are possible :
  - a specific destination address
  - a broadcast address.
  In reception, the controller compares the receive addresses to internal registers, which contain its own address. 4 bits in the receive command register (HRCR) inform the receiver of which registers, it has to take into account for the comparison. The receiver can compare one or two address bytes of the message to the specific board address and/or the broadcast address.
  For the specific destination address only, the receiver can compare or not each bit of the two receive address bytes to the programmable Address Field Recognition register. An Address Field Recognition Mask register is associated to each Address Field Recognition register; so each received address bit can be masked or not individually.
  The programmable Address Field Recognition register is located in the Address Field Recognition Memory and the programmable Address Field Recognition Mask register is located in the Address Field Recognition Mask Memory.
  Upon an address match, the address and the data following are written to the data buffers; upon an address mismatch, the frame is ignored. So, it authorizes the filtering of the messages. If no comparison is specified, each frame is received whatever its address field.
  In Transmission, the whole of the transmit frame is located in shared memory; the controller sends the frame including the destination or broadcast addresses.

III.2.2 - CSMA/CR Capability

An HDLC channel can come in and go out by any TDM input on the matrix. For time constraints, direct HDLC Access is achieved by the input TDM (DIN 8) and the output TDM (DOUT6).
In transmission, a time slot of a TDM can be shared between different sources in Multi-point to point configuration (different subscriber's boards for example). The arbitration system is the CSMA/CR (Carrier Sense Multiple access with Contention Resolution). The contention is resolved by a bus connected to the CB pin (Contention Bus). This bus is a 2Mbit/s wire line common to all the potential sources.
If a *Multi-HDLC* has obtained the access to the bus, the data to transmit is sent simultaneously on the CB line and the output TDM. The result of the contention is read back on the Echo line. If a collision is detected, the transmission is stopped immediately. A contention on a bit basis is so achieved. Each message to be sent with CSMA/CR has a priority class (PRI = 8, 10) indicated by the Transmit Descriptor and some rules are implemented to arbitrate the access to the line. The CSMA/CR Algorithm is given. When a request to send a message occurs, the transmitter determines if the shared channel is free. The *Multi-HDLC* listens to the Echo line. If C or more consecutive "1" are detected (C depending on the message's priority), the *Multi-HDLC* begins to send its message. Each bit sent is sampled back and compared with the original value to send. If a bit is different, the transmission is instantaneously stopped (before the end of this bit time) and will restart as soon as the *Multi-HDLC* will detect that the channel is free without interrupting the microprocessor.
After a successful transmission of a message, a

III - FUNCTIONAL DESCRIPTION (continued)

programmable penalty PEN(1 or 2) is applied to the transmitter (see Paragraph HDLC Transmit Command Register on Page 81). It guarantees that the same transmitter will not take the bus another time before a transmitter which has to send a message of same priority.
In case of a collision, the frame which has been aborted is automatically retransmitted by the DMA controller without warning the microprocessor of this collision. The frame can be located in several buffers in external memory. The collision can be detected from the second bit of the opening frame to the last but one bit of the closing frame.

III.2.3 - Time Slot Assigner Memory

Each HDLC channel is bidirectional and configurate by the Time Slot Assigner (TSA).

The TSA is a memory of 32 words (one per physical Time Slot) where all of the 32 input and output time slots of the HDLC controllers can be associated to logical HDLC channels. Super channels are created by assigning the same logical channel number to several physical time slots.

The following features are configurate for each HDLC time slot :
- Time slot used or not
- One logical channel number
- Its source : (DIN 8 or the output 7 of the matrix)
- Its bit rate and concerned bits (4kbit/s to 64kbit/s). 4kbit/s correspond to one bit transmitted each two frames. This bit must be present in two consecutive frames in reception, and repeated twice in transmission.
- Its destination :
  - direct output on DOUT6
  - direct output on DOUT6 and on the Contention Bus (CB)
  - on another OTDM via input 7 of the matrix and on the Contention Bus (CB)

III.2.4 - Data Storage Structure

Data associated with each Rx and Tx HDLC channel is stored in external memory; The data transfers between the HDLC controllers and memory are ensured by 32 DMAC (Direct Memory Access Controller) in reception and 32 DMAC in transmission.

The storage structure chosen in both directions is composed of one circular queue of buffers per channel. In such a queue, each data buffer is pointed to by a Descriptor located in external memory too. The main information contained in the Descriptor is the address of the Data Buffer, its length and the address of the next Descriptor; so the descriptors can be linked together.

This structure allows to :
- Store receive frames of variable and unknown length
- Read transmit frames stored in external memory by the host
- Easily perform the frame relay function.

III.2.4.1 - Reception

At the initialization of the application, the host has to prepare an Initialization Block memory, which contains the first receive buffer descriptor address for each channel, and the receive circular queues. At the opening of a receive channel, the DMA controller reads the address of the first buffer descriptor corresponding to this channel in the initialization Block. Then, the data transfer can occur without intervention of the processor (see Figure 12 on Page 28).

A new HDLC frame always begins in a new buffer. A long frame can be split between several buffers if the buffer size is not sufficient. All the information concerning the frame and its location in the circular queue is included in the Receive Buffer Descriptor :
- The Receive Buffer Address (RBA),
- The size of the receive buffer (SOB),
- The number of bytes written into the buffer (NBR),
- The Next Receive Descriptor Address (NRDA),
- The status concerning the receive frame,
- The control of the queue.

III.2.4.2 - Transmission

In transmission, the data is managed by a similar structure as in reception (see Figure 13 on Page 28).

By the same way, a frame can be split up between consecutive transmit buffers.

The main information contained in the Transmit Descriptor are :
- transmit buffer address (TBA),
- number of bytes to transmit (NBT) concerning the buffer,
- next transmit descriptor address (NTDA),
- status of the frame after transmission,
- control bit of the queue,
- CSMA/CR priority (8 or 10).

III.2.4.3 - Frame Relay

The principle of the frame relay is to transmit a frame which has been received without treatment. A new heading is just added. This will be easily achieved, taking into account that the queue structure allows the transmission of a frame split between several buffers.

III - FUNCTIONAL DESCRIPTION (continued)

Figure 12 : Structure of the Receive Circular Queue

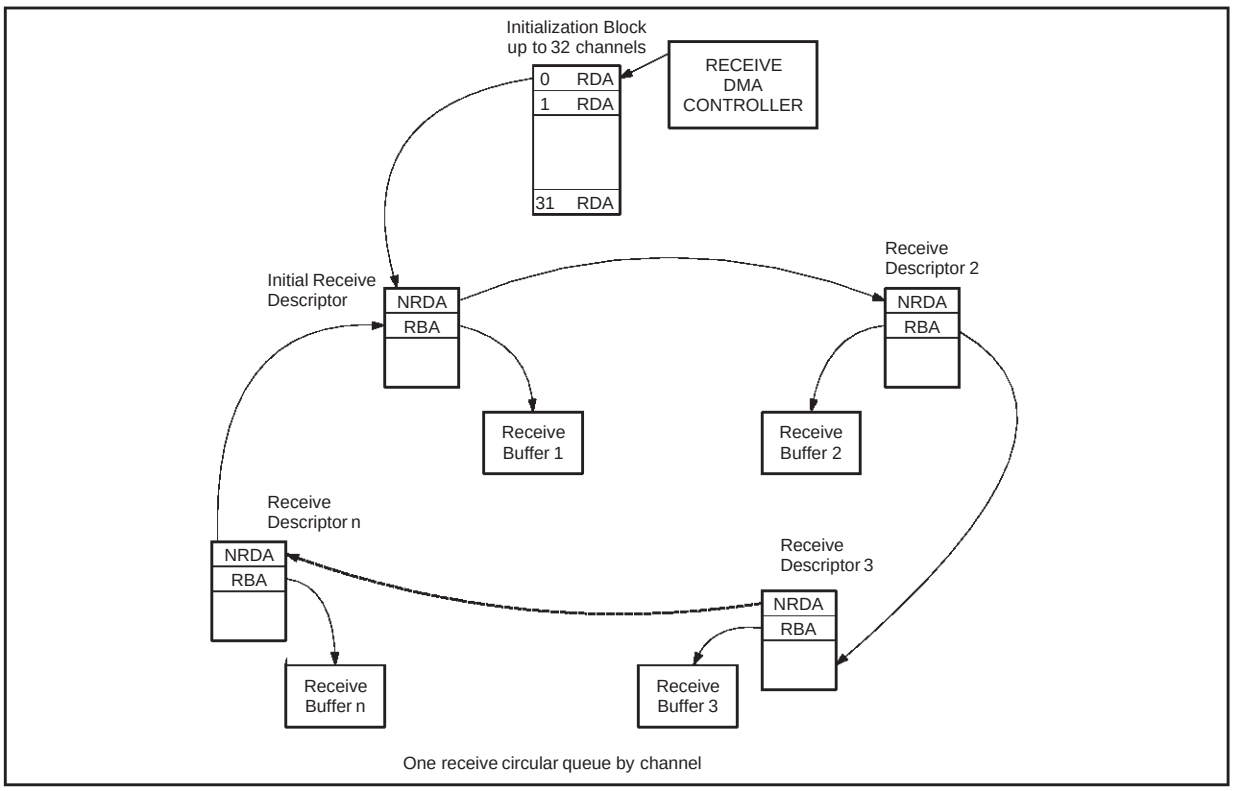
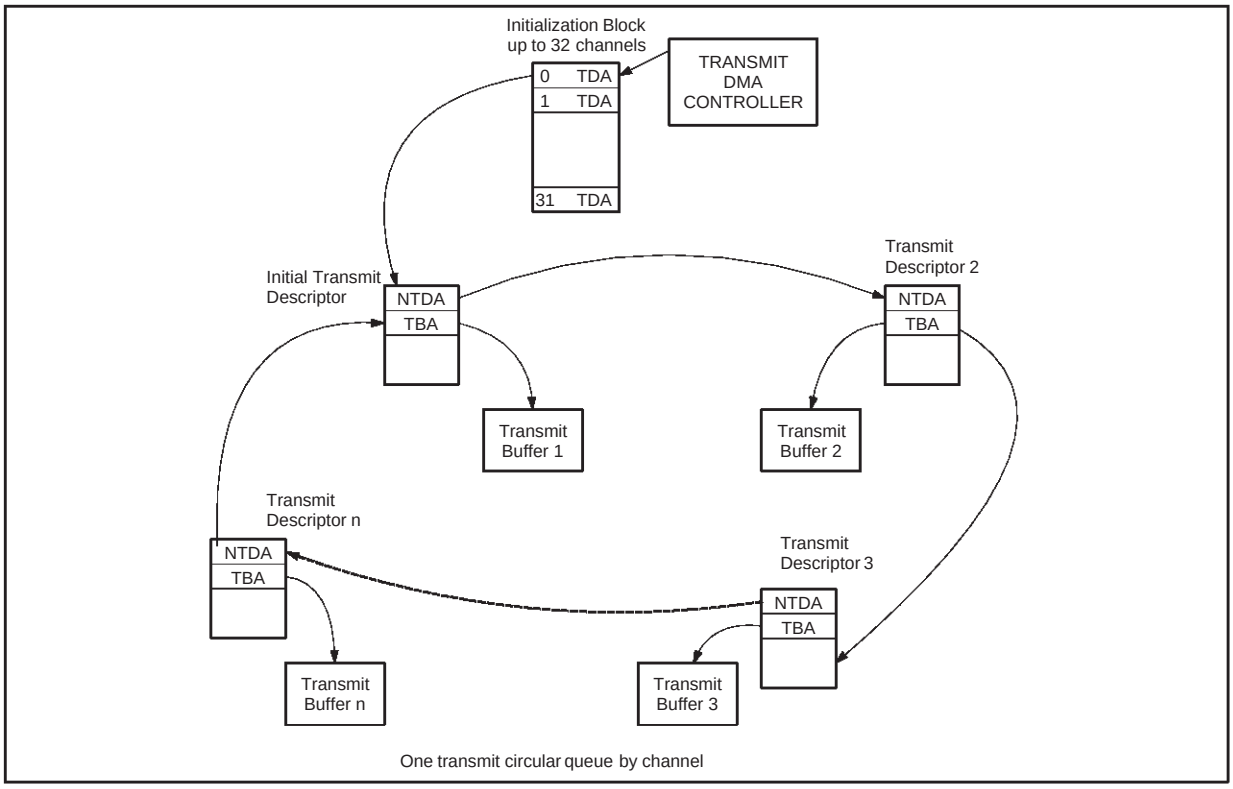


Figure 13 : Structure of the Transmit Circular Queue



III - FUNCTIONAL DESCRIPTION (continued)

III.2.5 - Transparent Modes

In the transparent mode, the *Multi-HDLC* transmits data in a completely transparent manner without performing any bit manipulation or Flag insertion. The transparent mode is per byte function.

Two transparent modes are offered :

- First mode : for the receive channels, the *Multi-HDLC* continuously writes received bytes into the external memory as specified in the current receive descriptor without taking into account the Fill Character Register.
- Second mode : the Fill Character Register specifies the "fill character" which must be taken into account. In reception, the "fill character" will not be transferred to the external memory. The detection of "Fill character" marks the end of a message and generates an interrupt if BINT = 1 (see Transmit Descriptor on Page 95). When the "Fill character" is not detected a new message is receiving.

As for the HDLC mode the correspondence between the physical time slot and the logical channel is fully defined in the Time Slot Assigner memory (Time slot used or not used, logical channel number, source, destination).

III.2.6 - Command of the HDLC Channels

The microprocessor is able to control each HDLC receive and transmit channel. Some of the commands are specific to the transmission or the reception but others are identical.

III.2.6.1 - Reception Control

The configuration of the controller operating mode is: HDLC mode or Transparent mode.

The control of the controller: START, HALT, CONTINUE, ABORT.

- START : On a start command, the RxDMA controller reads the address of the first descriptor in the initialization block memory and is ready to receive a frame.
- HALT : For overloading reasons, the microprocessor can decide to halt the reception. The DMA controller finishes transfer of the current frame to external memory and stops. The channel can be restarted on CONTINUE command.
- CONTINUE : The reception restarts in the next descriptor.
- ABORT: On an abort command, the reception is instantaneously stopped. The channel can be restarted on a START or CONTINUE command.

Reception of FLAG (01111110) or IDLE (11111111) between Frames.
Address recognition. The microprocessor defines the addresses that the Rx controller has to take into account.
In transparent mode: "fill character" register selected or not.

III.2.6.2 - Transmission Control

The configuration of the controller operating mode is : HDLC mode or Transparent mode.

The control of the controller : START, HALT, CONTINUE, ABORT.

- START : On a start command, the Tx DMA controller reads the address of the first descriptor in the initialization block memory and tries to transmit the first frame if End Of Queue is not at "1".
- HALT : The transmitter finishes to send the current frame and stops. The channel can be restarted on a CONTINUE command.
- CONTINUE : if the CONTINUE command occurs after HALT command, the HDLC Transmitter restarts by transmitting the next buffer associated to the next descriptor.
  If the CONTINUE command occurs after an ABORT command which has occurred during a frame, the HDLC transmitter restarts by transmitting the frame which has been effectively aborted by the microprocessor.
- ABORT: On an abort command, the transmission of the current frame is instantaneously stopped, an ABORT sequence "1111111" is sent, followed by IDLE or FLAG bytes. The channel can be restarted on a START or CONTINUE command.

Transmission of FLAG (01111110) or IDLE (111111111) between frames can be selected.
CRC can be generated or not. If the CRC is not generated by the HDLC Controller, it must be located in the shared memory.
In transparent mode: "fill character" register can be selected or not.

III.3 - C/I and Monitor

III.3.1 - Function Description

The *Multi-HDLC* is able to operate both GCI and V* links. The TDM DIN/DOUT 4 and 5 are internally connected to the CI and Monitor receivers/transmitters. Since the controllers handle up to 16 CI and 16 Monitor channels simultaneously, the *Multi-HDLC* can manage up to 16 level 1 circuits.

The *Multi-HDLC* can be used to support the CI and monitor channels based on the following protocols :

- ISDN V* protocol
- ISDN GCI protocol
- Analog GCI protocol.

III - FUNCTIONAL DESCRIPTION (continued)

III.3.2 - GCI and V* Protocol

A TDM can carry 8 GCI channels or V* channels. The monitor and S/C bytes always stand at the same position in the TDM in both cases.

Channel 0				Channel 1 to Channel 30	Channel 31			
TS0	TS1	TS2	TS3		TS28	TS29	TS30	TS31
B1	B2	MON	S/C		B1	B2	MON	S/C

The GCI or V* channels are composed of 4 bytes and have both the same general structure.

B1	B2	MON	S/C

B1, B2 : Bytes of data. Those bytes are not affected by the monitor and CI protocols.
MON : Monitor channel for operation and maintenance information.
S/C : Signalling and control information.

Only Monitor handshakes and S/C bytes are different in the three protocols :

ISDN V* S/C byte

D	C/I 4 bits	T	E

ISDN GCI S/C byte

D	C/I 4 bits	A	E

Analog GCI S/C byte

C/I 6 bits	A	E

CI : The Command/Indicate channel is used for activation/deactivation of lines and control functions.
D : These 2 bits carry the 16 kbit/s ISDN basic access D channel.

In GCI protocol, A and E are the handshake bits and are used to control the transfer of information on monitor channels. The E bit indicates the transfer of each new byte in one direction and the A bit acknowledges this byte transfer in the reverse direction.

In V* protocol, there isn't any handshake mode. The transmitter has only to mark the validity of the Monitor byte by positioning the E bit (T is not used and is forced to "1").

For more information about the GCI and V*, refer to the General Interface Circuit Specification (issue1.0, march 1989) and the France Telecom Specification about ISDN Basic Access second generation (November 1990).

III.3.3 - Structure of the Treatment

GCI/V* TDM's are connected to DIN 4 and DIN 5. The D channels are switched through the matrix towards the output 7 and the HDLC receiver. The Monitor and S/C bytes are multiplexed and sent to the CI and Monitor receivers (see Figure 14 on Page 31).

In transmission, the S/C and Monitor bytes are recombined by multiplexing the information provided by the Monitor, C/I and the HDLC Transmitter. Like in reception, the D channel is switched through the matrix.

III.3.4 - CI and Monitor Channel Configuration

Monitor channel data is located in a time slot ; the CI and monitor handshake bits are in the next time slot.

Each channel can be defined independently. A table with all the possible configurations is presented hereafter (Table 13).

Table 13 : C/I and MON Channel Configuration

C/I validated or not	CI For analog subscriber (6 bits)
	CI For ISDN subscriber (4 bits)
Monitor validated or not	Monitor V*
	Monitor GCI

Note : A mix of V* and GCI monitoring can be performed for two distinct channels in the same application.

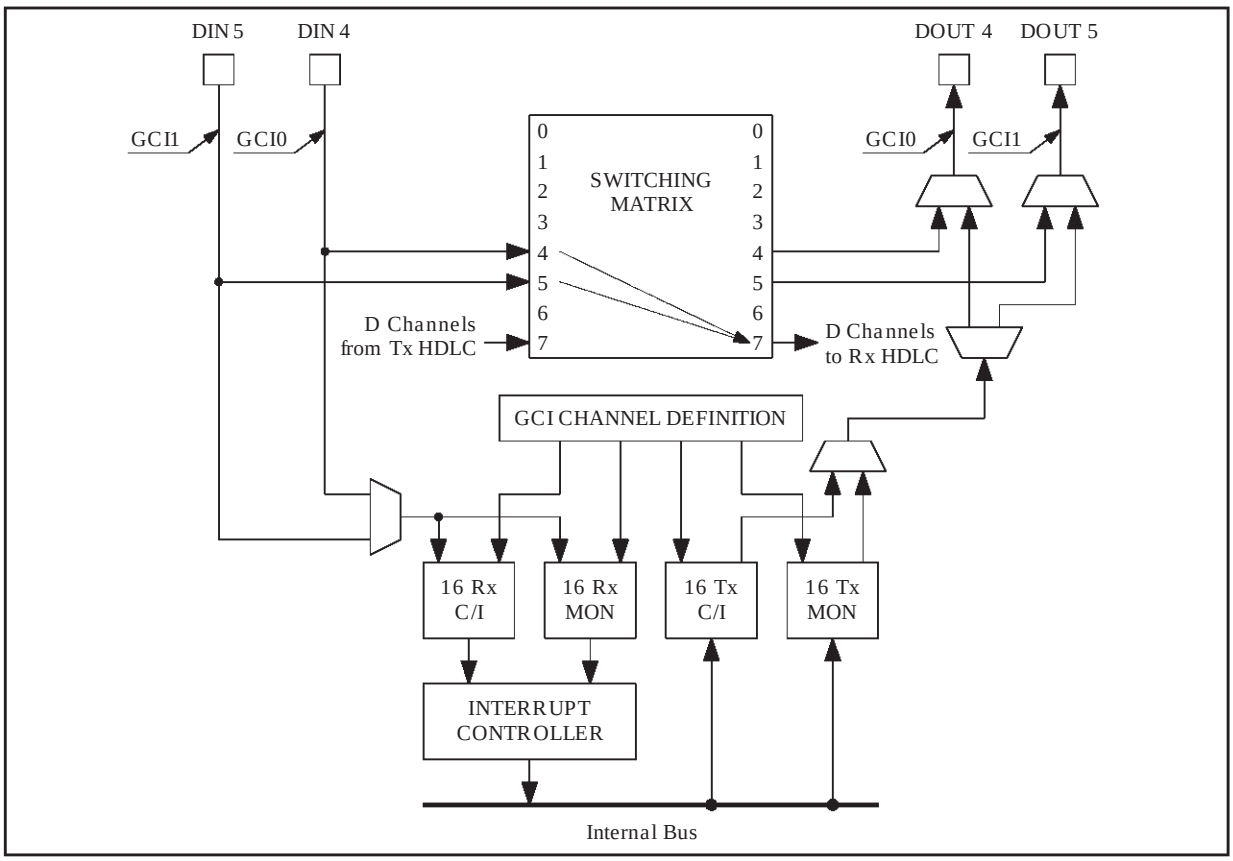
III.3.5 - CI and Monitor Transmission/Reception Command

The reception of C/I and Monitor messages are managed by two interrupt queues.

In transmission, a transmit command register is implemented for each C/I and monitor channel (16 C/I transmit command registers and 16 Monitor transmit command registers). Those registers are accessible in read and write modes by the microprocessor.

III - FUNCTIONAL DESCRIPTION (continued)

Figure 14 : D, C/I and Monitor Channel Path



III.3.6 - Scrambler and Descrambler

The TDM4 and TDM5 can be GCI multipexes. Each GCI multipex comprises 8 GCI channels. Each GCI channel comprises two B channels at 64 Kbit/s.

In reception it is possible to switch and to scramble the contents of 32 B channels of GCI channels to 32 timeslots of the 256 output timeslots. In transmission these 32 timeslots are assigned to 32 B channels.

In the other direction the contents of an selected B channels is automatically switched and descrambled to one B channel of 16 GCI channel.

See Connection Memory Data Register CMDR (0E)H on page 74 (SCR bit).

Connection between “ISDN channels” and GCI channels.

Three timeslots are assigned to one“ISDN channels”. Each “ISDN channels” comprises three channels: B1+B2+B* with B*= D1,D2, A, E, S1, S2, S3, S4. GCI channel to/from ISDN channel on page 32.

Upstream. From GCI channels to ISDN channels on page 33.

- in reception: 16 GCI channels (B1+B2+MON+ D+C/I),
- in transmission: 16 ISDN channels (B1+B2+B*).
  It is possible to switch the contents of B1, B2 and D channelsfrom 16 GCI channels in any 16 “ISDN channels”, TDM side.
  The contents of B1 and/or B2 can be scrambled or not. If scrambled the number of the 32 timeslots (TDM side) are different mandatory.
  Receiving the contents of Monitor and Command / Indicate channels from 16 GCI channels. Primitives and messages are stored automatically in the external shared memory.
  Transmitting “six bit word” (A, E, S1, S2, S3, S4) to any 16 “ISDN channels” TDM side or not. See SBV bit of General Configuration Register GCR (02)H on page 68.

Downstream. From ISDN channels to GCI channels on page 34.

- in reception: ISDN channel (B1+B2+B*)
- in transmission: GCI channel (B1+B2+MON+ D+C/I)
  It is possible to switch the contents of B1, B2 and D channels from 16 “ISDN channels”, TDM side

III - FUNCTIONAL DESCRIPTION (continued)

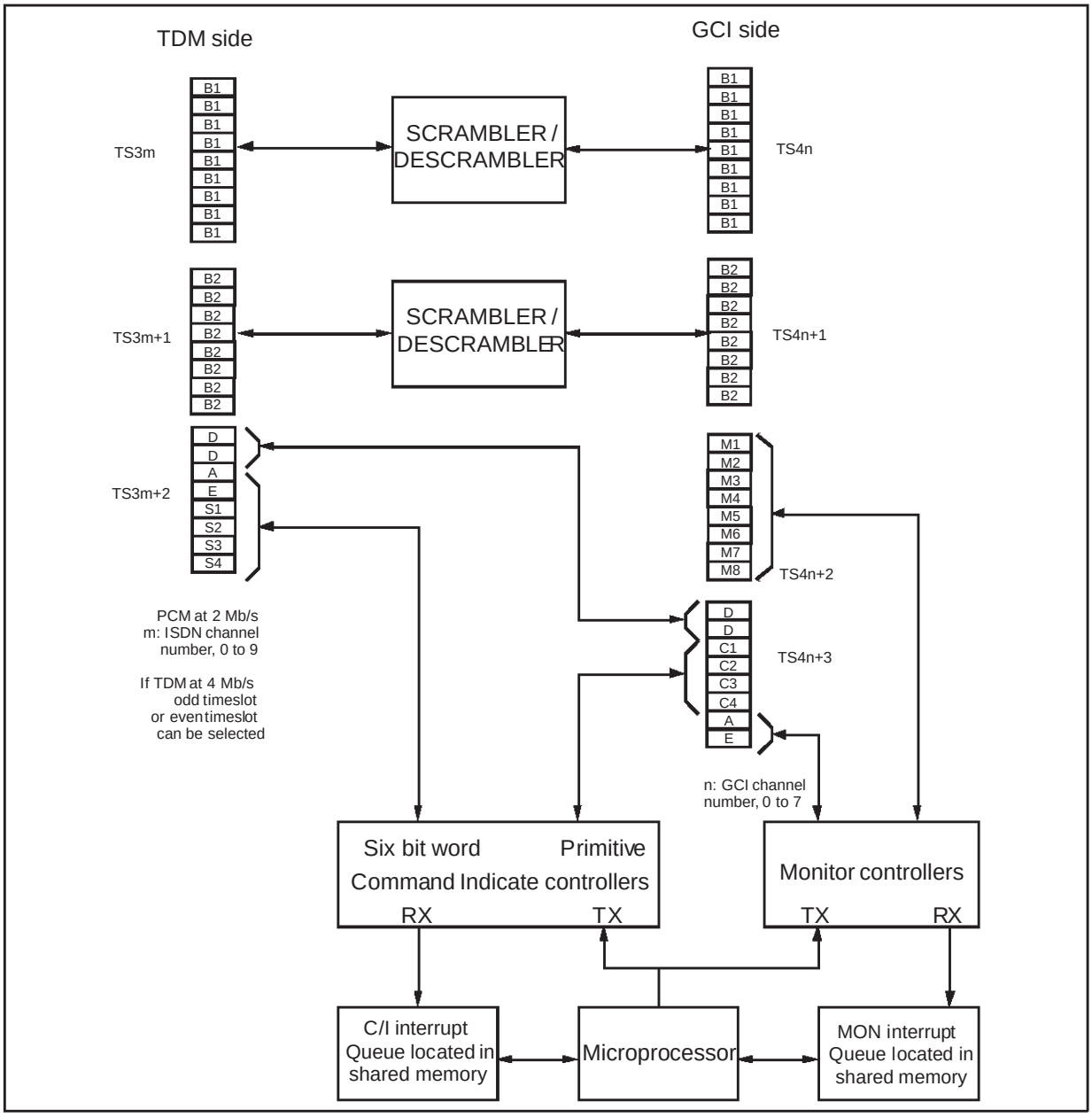
in 16 GCI channels.
The contents of B1 and/or B2 can be descrambled or not. If descrambled the 32 B1/B2 belong to GCI channels mandatory.
Receiving six bit word (A, E, S1, S2, S3, S4) from any 16 “ISDN channels”, TDM side. The 16 “six bit word” are stored automatically in the external shared memory.
Transmitting the contents of Monitor and Command / Indicate channels to 16 GCI channels.

See SBV bit of General Configuration Register GCR (02)H on page 68.

Alarm Indication Signal.

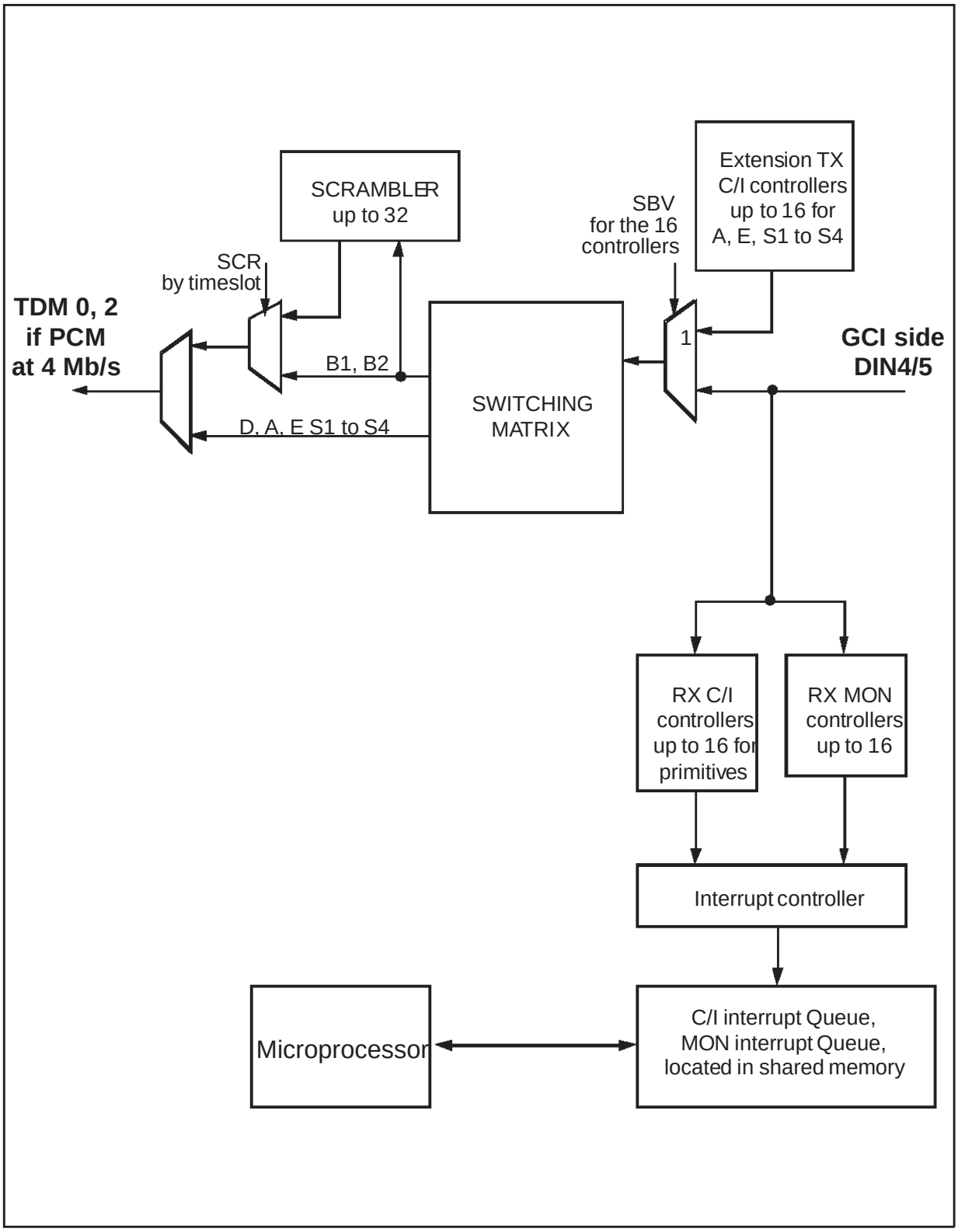
This detection concerns 16 hyperchannels. One hyperchannel comprises 16 bits (B1 and B2 only). The Alarm Indications for the 16 hyperchannels are stored automatically in the external shared memory. See AISD bit of Switching Matrix Configuration Reg SMCR (0C)H on page 71.

Figure 15: GCI channel to/from ISDN Channel



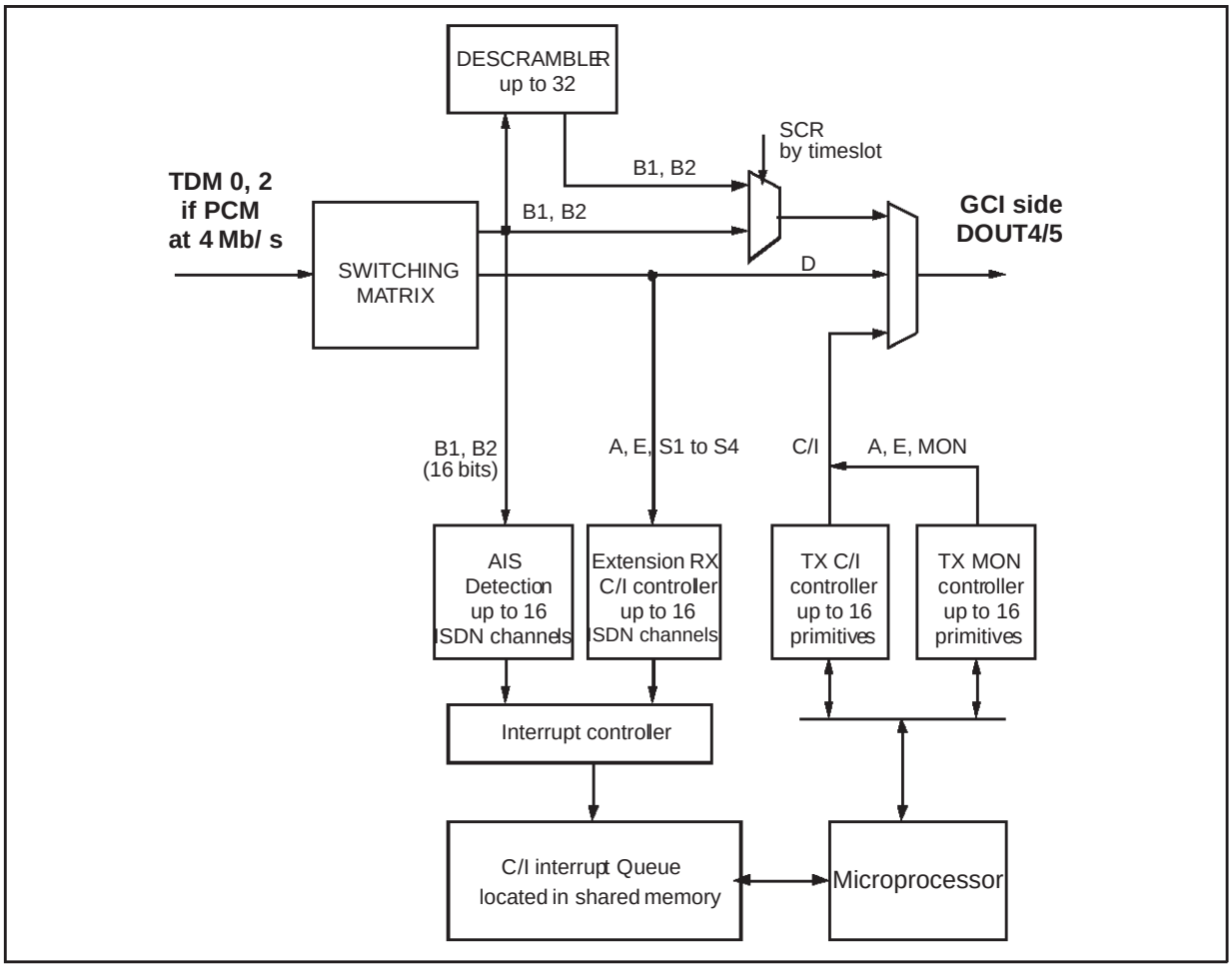
III - FUNCTIONAL DESCRIPTION (continued)

Figure 16: From GCI Channels to ISDN Channels



III - FUNCTIONAL DESCRIPTION (continued)

Figure 17: From ISDN channels to GCI Channels



III.4 - Microprocessor Interface

III.4.1 - Description

The *Multi-HDLC* circuit can be controlled by several types of microprocessors (ST9, Intel/Motorola 8 or 16 data bits interfaces) such as :

- ST9 family
- INTEL 80C188 8 bits
- INTEL 80C186 16 bits
- MOTOROLA 68000 16 bits
- MOTOROLA 68020 16/32 bits
- ST10 family

During the initialization of the *Multi-HDLC* circuit, the microprocessor interface is informed of the type of microprocessor that is connected by polarisation of three external pins MOD 0/2).

Two chip Select (CS0/1) pins are provided. CS0 will select the internal registers and CS1 the external memory.

Table 14 : Microprocessor Interface Selection

MOD2 Pin	MOD1 Pin	MOD0 Pin	Microprocessor
0	1	1	80C188
1	1	1	80C186
1	0	0	68000
0	0	0	68020
0	0	1	ST9
1	0	1	ST10 A/D multiplexed
1	1	0	ST10 A/D not multiplexed
0	1	0	Reserved

III.4.2 - Exchange with the shared memory

A Fetch Buffer located in the microprocessor interface allows to reduce the shared memory access cycle for the microprocessor.

It is used whatever microprocessor selected thanks to MOD0/2 pins.

This Fetch Buffer consists of one Write FIFO and four Read Fetch Memories.

III.4.2.1 - Write FIFO

When the microprocessor delivers the address word named An to write data named [An] in the shared memory in fact it writes data [An] and address word An in the Write FIFO (Deep 4 words). If An is in Fetch Memory, [An] is removed in Fetch Memory.

The number of wait cycles for the microprocessor is strongly reduced.

III.4.2.2 - Read Fetch Memory

When the microprocessor delivers the address word named An to read data named [An] out of the shared memory in fact it reads data [An] from one of four Read Fetch Memories.

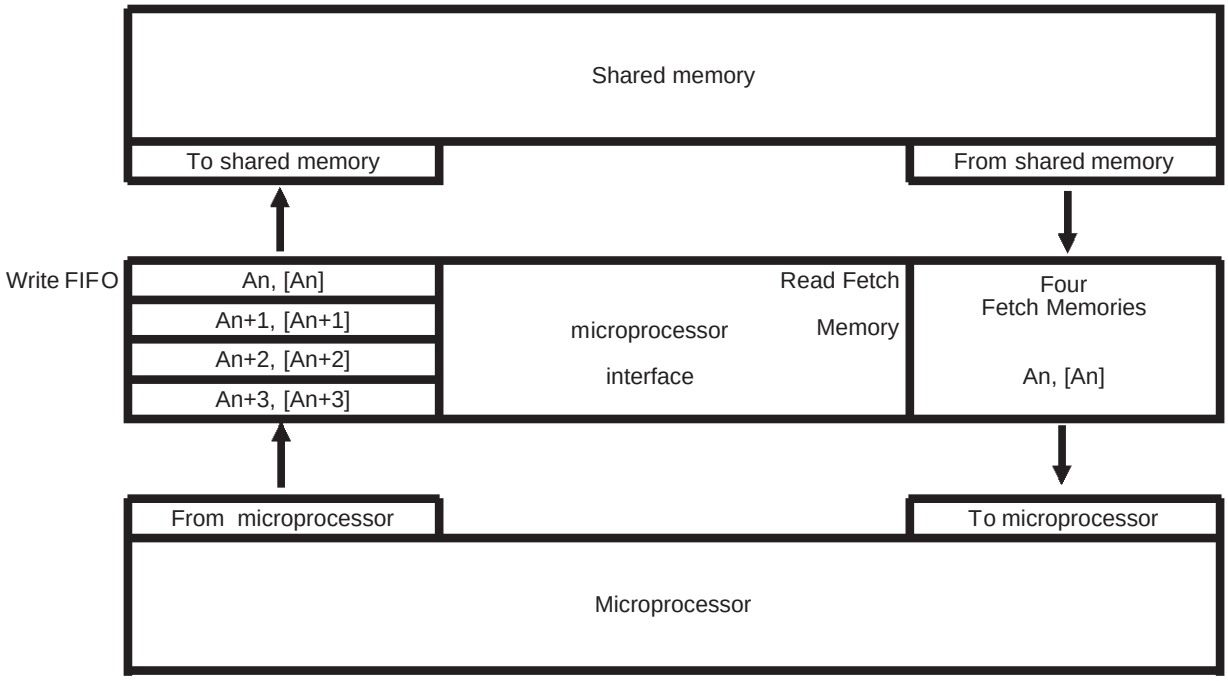
The number of wait cycle for the microprocessor is strongly reduced and can reach zero when An, address word delivered by the microprocessor, and data [An] is already in the Read Fetch Memory and validated.

The source of [An] is truly the shared memory whatever An.

III.4.3 - Definition of the Interface for the different microprocessors

The signals connected to the microprocessor interface are presented on the following figures for the different microprocessor.

Figure 17.1: Write FIFO and Fetch Memories.



III - FUNCTIONAL DESCRIPTION (continued)

Figure 18 : *Multi-HDLC* connected to µP with multiplexed buses

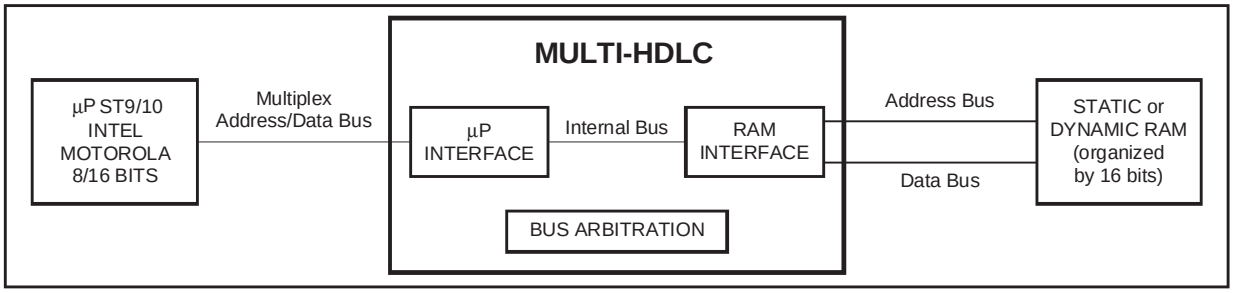


Figure 19 : *Multi-HDLC* connected to µP with non-multiplexed buses

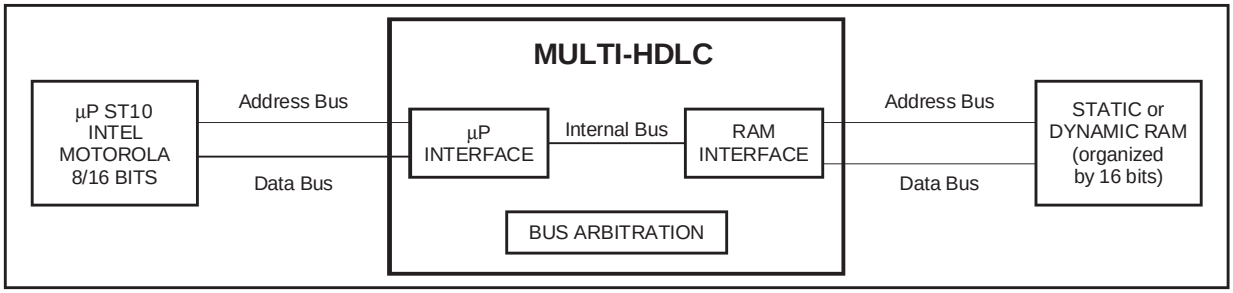


Figure 20 : Microprocessor Interface for INTEL 80C188

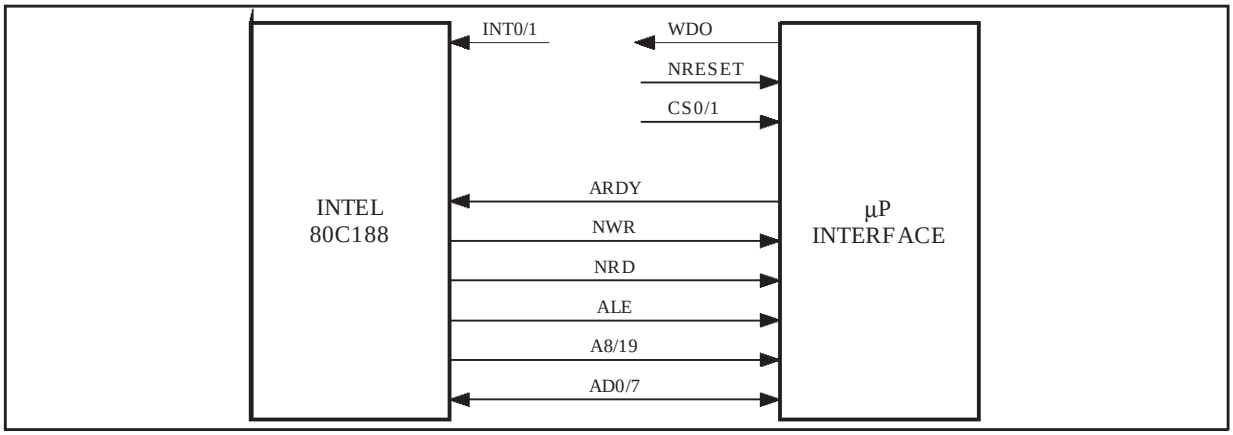
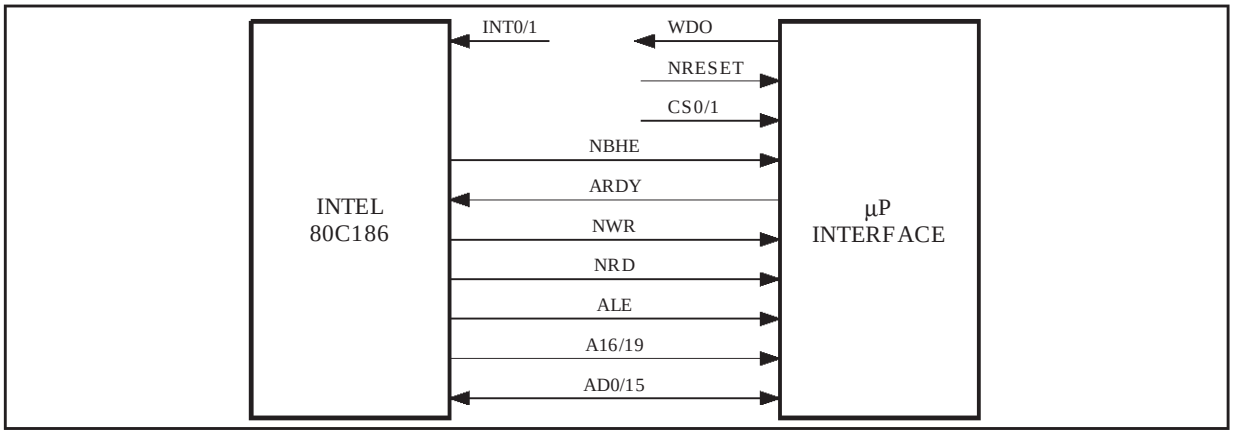


Figure 21 : Microprocessor Interface for INTEL 80C186



III - FUNCTIONAL DESCRIPTION (continued)

Figure 22 : Microprocessor Interface for MOTOROLA 68000

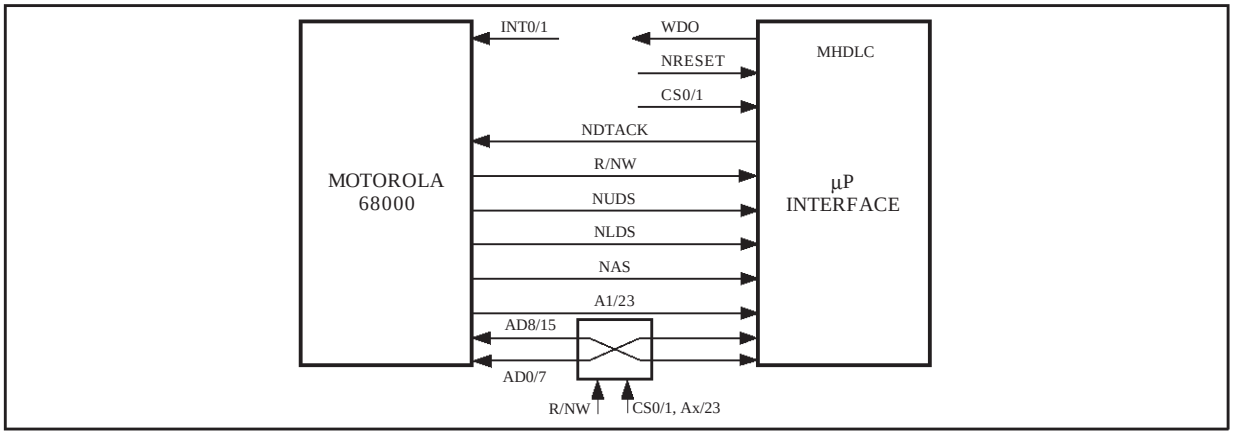


Figure 23 : Microprocessor Interface for MOTOROLA 68020

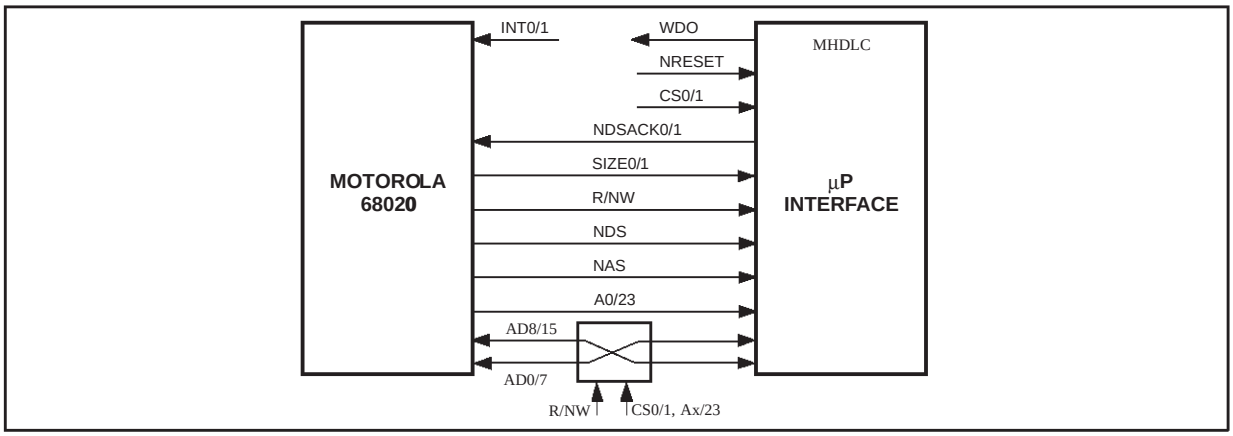
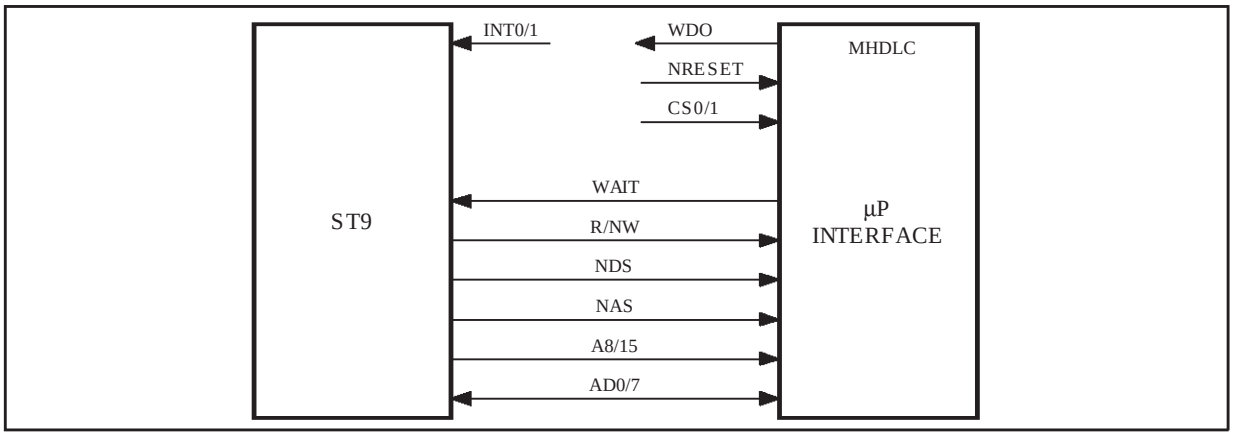


Figure 24 : Microprocessor Interface for ST9



III - FUNCTIONAL DESCRIPTION (continued)

III.5 - Memory Interface

III.5.1 - Function Description

The memory interface allows the connection of Static or Dynamic RAM. The memory space addressable in the two configurations is not the same. In the case of dynamic memory (DRAM), the memory interface will address up to 16 Megabytes. In case of static memory (SRAM) only 1 Megabyte will be addressed. The memory location is always organized in 16 bits.

The memory is shared between the *Multi-HDLC* and the microprocessor. The access to the memory is arbitrated by an internal function of the circuit: the bus arbitration.

III.5.2 - Choice of memory versus microprocessor and capacity required

The memory interface depends on the memory chips which are connected. As the memory chips will be chosen versus the microprocessor and the wanted memory space, the following table presents the different configurations DRAM and SRAM selection versus µP.

Example 1 : if the application requires 16 bit mProcessor and 1 Megaword Shared memory size, three capabilities are offered :
- 4 DRAM Circuits (256Kx16) or
- 4 DRAM Circuits (1Mx4) or
- 1 DRAM Circuit (1Mx16).

Example 2 : if the application requires 8 bit mProcessor and 1 Megabyte Shared memory size, three capabilities are offered:
- 2 DRAM Circuits (256Kx16) or
- 8 SRAM Circuits (128Kx8) or
- 2 SRAM Circuits (512kx8).

Example 3 : for small applications it is possible to connect 2 SRAM Circuits (128Kx8) to obtain 256 Kilobytes shared memory.

III.5.3 - Memory Cycle

For SRAM and DRAM, the different cycles are programmable. See Memory Interface Configuration Regist. MICR $(32)_H$ on Page 88.

Each cycle is equal to : p x 1/f
with f the frequency of signal applied to the Crystal 1 input and p selected by the user. See page 9.

Table 22 : DRAM and SDRAM Selection versus µP

Microprocessor and shared memory		**Shared memory size required by the application**					
8 bits µProcessor	Number of Megabytes	0.5	1	2	4	8	16
16/32 bits µProcessor	Number of Megawords	0.25	0.5	1	2	4	8
DRAM Circuits proposed							
Capacity	Organization						
4 Megabits	256Kx16	1(256Kx16)	2(256Kx16)	4(256Kx16)			
	1Mx4			4(1Mx4)	8(1Mx4)	16(1Mx4)	
16 Megabits	1Mx16			1(1Mx16)	2(1Mx16)	4(1Mx16)	
	4Mx4					4(4Mx4)	8(4Mx4)
64 Megabits	4Mx16					1(4Mx16)	2(4Mx16)
SRAM Circuits proposed				Not possible			
Capacity	Organization						
1 Megabits	128Kx8	4(128Kx8)	8(128Kx8)				
4 Megabits	512kx8		2(512kx8)				

III - FUNCTIONAL DESCRIPTION (continued)

III.5.4 - SRAM interface

The SRAM space achieves 1 Mbyte max. It is always organized in 16 bits. The structure of the memory plane is shown in the following figures.
Because of the different chips usable, 19 address wires and 8 NCE (Chip Enable) are necessary to address the 1 Mbyte. The NCE selects the Most or Least Significant Byte versus the value of A0 delivered by the µP and the location of chip in the memory space.

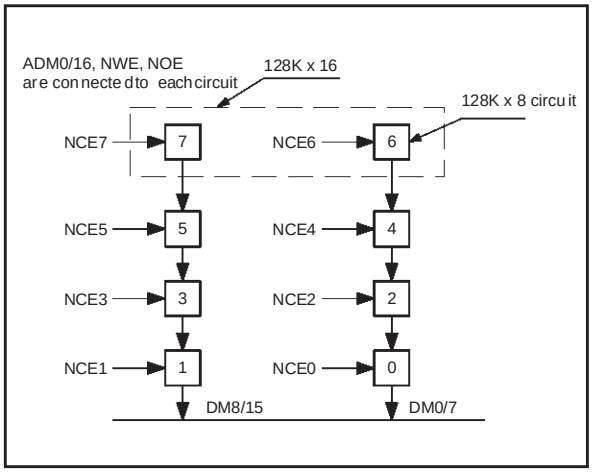
III.5.4.1 - 128K x 16 (up to 512K x 16) SRAM

This memory can be obtained with two 128K x 8 SRAM circuits (up to eight circuits)

Signals	A19	A18	A0 or equiv.
NCE7	1	1	1
NCE6	1	1	0
NCE5	1	0	1
NCE4	1	0	0
NCE3	0	1	1
NCE2	0	1	0
NCE1	0	0	1
NCE0	0	0	0

The Address bits delivered by the *Multi-HDLC* for 128K x 8 SRAM circuits are :
ADM0/14 and ADM15/16 (17 bits) corresponding with A1/17 delivered by the µP.

Figure 25 :n x 128K x 16 SRAM Memory Organization

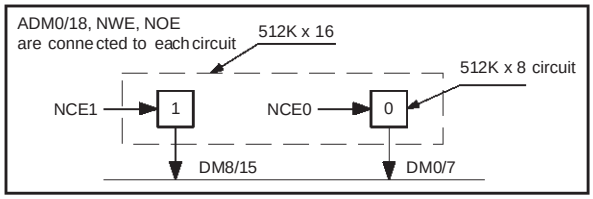


III.5.4.2 - 512K x n SRAM

Signals	A0 or equiv.
NCE1	1
NCE0	0

The Address bits delivered by the *Multi-HDLC* for 512K x n SRAM circuits are :
ADM0/14 and ADM15/18 (19 bits) corresponding with A1/19 delivered by the µP.

Figure 26 :512K x 8 SRAM Circuit Memory Organization



III.5.5 - DRAM Interface

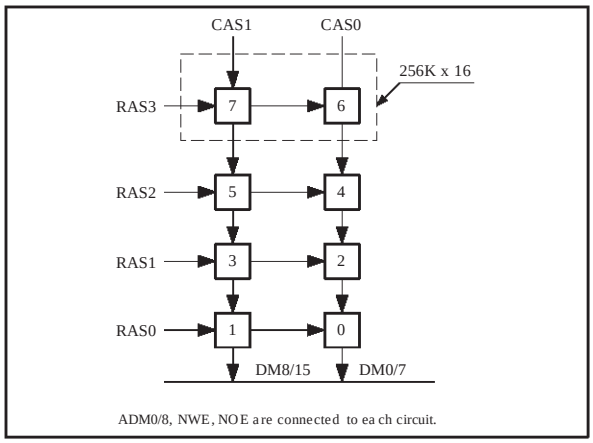
In DRAM, the memory space can achieve up to 16 megabytes organized by 16 bits. Eleven address wires, four NRAS and two NCAS are needed to select any byte in the memory. One NRAS signal selects 1 bank of 4 and the NCAS signals select the bytes concerned by the transfer (1 or 2 selecting a byte or a word). The DRAM memory interface is then defined. The "RAS only" refresh cycles will refresh all memory locations. The refresh is programmable. The frequency of the refresh is fixed by the memory requirements.

III.5.5.1 - 256K x n DRAM Signals

Signals	A20	A19	A0	6800
NRAS3	1	1		
NRAS2	1	0		
NRAS1	0	1		
NRAS0	0	0		
NCAS1			1	UDS
NCAS0			0	LDS

The Address bits delivered by the *Multi-HDLC* for 256K x n DRAM circuits are :
ADM0/8 (2 x 9 = 18 bits) corresponding with A1/18 delivered by the µP.

Figure 27 : 256K x 16 DRAM Circuit Organization



5464-22.EPS

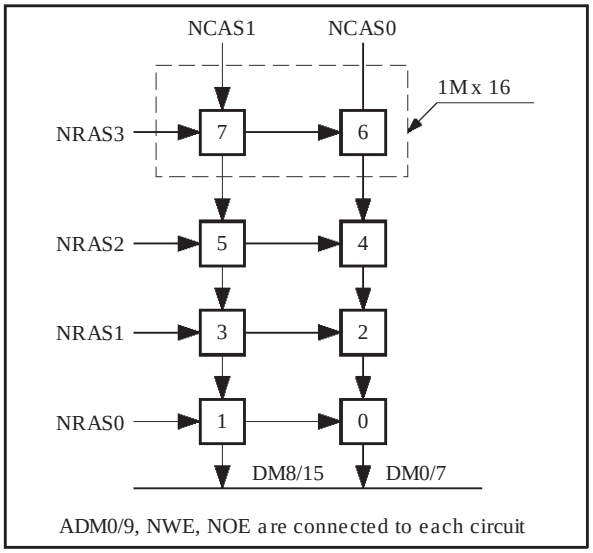
III - FUNCTIONAL DESCRIPTION (continued)

III.5.5.2 - 1M x n DRAM Signals

Signals	A22	A20	A0	6800
NRAS3	1	1		
NRAS2	1	0		
NRAS1	0	1		
NRAS0	0	0		
NCAS1			1	UDS
NCAS0			0	LDS

The Address bits delivered by the *Multi-HDLC* for 1M x n DRAM circuits are :
ADM0/9 (2 x 10 = 18 bits) corresponding with A1/20 delivered by the µP.

Figure 28 : 1M x 16 DRAM Circuit Organization



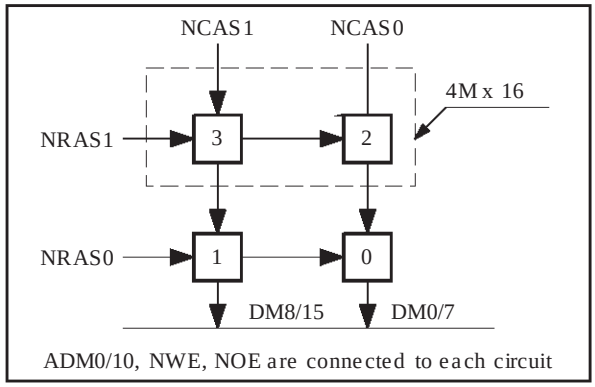
5464-23.EPS

III.5.5.3 - 4M x n DRAM Signals

Signals	A23	A0 or equiv.
NRAS1	1	
NRAS0	0	
NCAS1		1
NCAS0		0

The Address bits delivered by the *Multi-HDLC* for 4M x n DRAM circuits are :
ADM0/10 (2 x 11 = 22 bits) corresponding with A1/22 delivered by the µP.

Figure 29 : 4M x 16 DRAM Circuit Organization



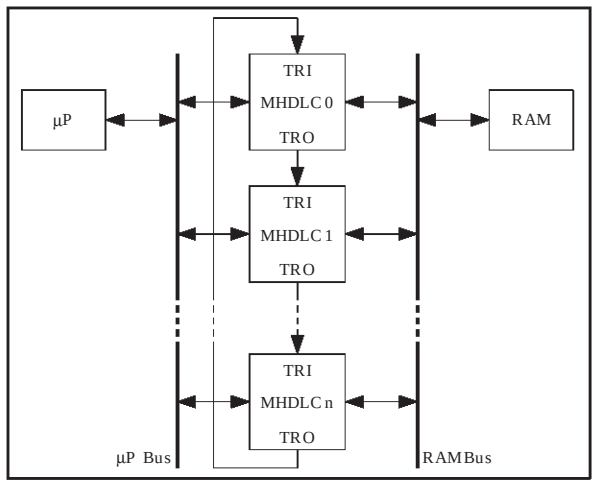
5464-24.EPS

III.6 - Bus Arbitration

The Bus arbitration function arbitrates the access to the bus between different entities of the circuit. Those entities which can call for the bus are the following :
- The receive DMA controller,
- The microprocessor,
- The transmit DMA controller,
- The Interrupt controller,
- The memory interface for refreshing the DRAM.

This list gives the memory access priorities per default.
If the treatment of more than 32 HDLC channels is required by the application, it is possible to chain several *Multi-HDLC* components. That is done with two external pins (TRI, TRO) and a token ring system.
The TRI, TRO signals are managed by the bus arbitration function too. When a chip has finished its tasks, it sends a pulse of 30 ns to the next chip.

Figure 30 : Chain of n *Multi-HDLC* Components



5464-25.EPS

III - FUNCTIONAL DESCRIPTION (continued)

III.7 - Clock Selection and Time Synchronization

III.7.1 - Clock Distribution Selection and Supervision

Two clock distributions are available: Clock at 4.096 MHz or 8.192 MHz and a synchronization signal at 8 KHz. The component has to select one of these two distributions and to check its integrity. See Fig. 31 MHDLC clock generation.

Two other clock distributions are allowed: Clock at 3072 MHz or 6144 MHz and a synchronization signal at 8 KHz. See General Configuration Register GCR (02)H on page 61 DCLK, FSC GCI and FSC V* are output on three external pins of the Multi-HDLC. DCLK is the clock selected between Clock A and Clock B. FSC, GCI and FSC V* are functions of the selected distribution and respect the GCI and V* frame synchronization specifications.

The supervision of the clock distribution consists of verifying its availability. The detection of the clock absence is done in a less than 250 microseconds. In case the clock is absent, an interrupt is generated with a 4 kHz recurrence. Then the clock distribution is switched automatically up to detection of couple A or couple B. When a couple is detected the change of clock occurs on a falling edge of the new selected distribution. Moreover the clock distribution can be controlled by the microprocessor thanks to SELB, bit of General Configuration Register.

Depending on the applications, three different signals of synchronization (GCI, V* or Sy) can be provided to the component. The clock A/B frequency can be a 4096 or 8192kHz clock. The component is informed of the synchronization and clocks that are connected by software. The timings of the different synchronization are given page 45.

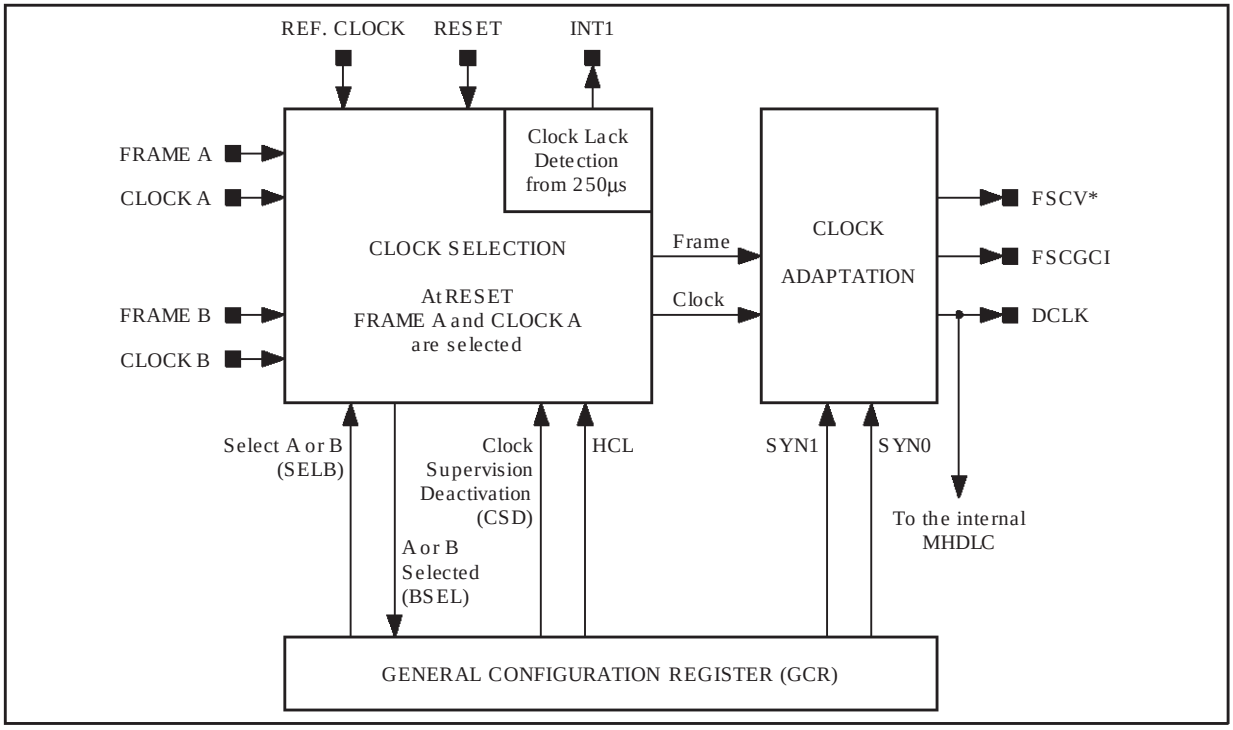
III.7.2 - VCXO Frequency Synchronization

An external VCXO can be used to provide a clock to the transmission components. This clock is controlled by the main clock distribution (Clock A or Clock B at 4096kHz). As the clock of the transmission component is 15360 or 16384kHz, a configurable function is necessary.

The VCXO frequency is divided by P (30 or 32) to provide a common sub-multiple (512kHz) of the reference frequency CLOCKA or CLOCKB (4096kHz). The comparison of these two signals gives an error signal which commands the VCXO.

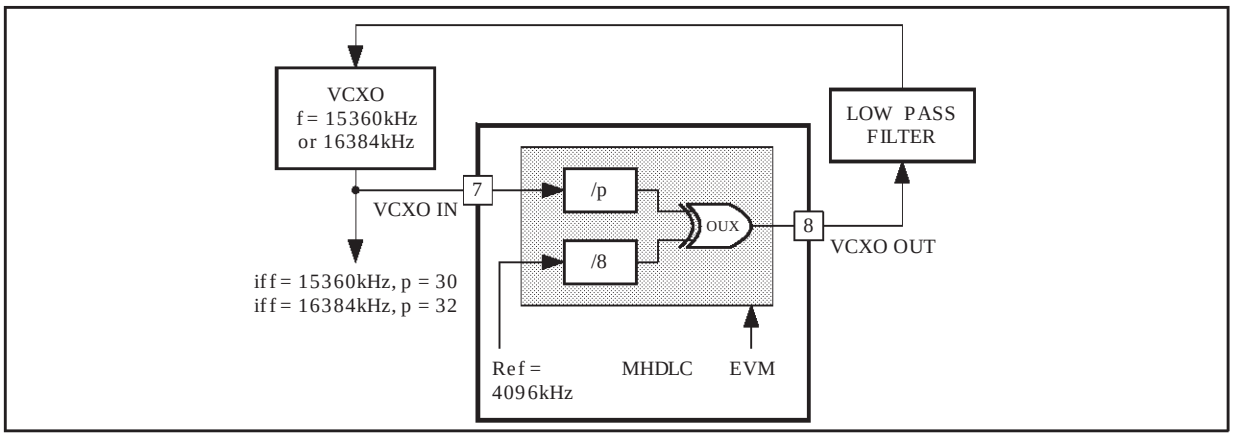
Two external pins are needed to perform this function : VCXO-IN and VCXO-OUT (see Figure 32 on Page 42).

Figure 31 : MHDLC Clock Generation



III - FUNCTIONAL DESCRIPTION (continued)

Figure 32 : VCXO Frequency Synchronization



III.8 - Interrupt Controller

III.8.1 - Description

Three external pins are used to manage the interrupts generated by the *Multi-HDLC*. The interrupts have three main sources :

- The operating interrupts generated by the HDLC receivers/transmitters, the CI receivers and the monitor transmitters/receivers. INT0 Pin is reserved for this use.
- The interrupt generated by an abnormal working of the clock distribution. INT1 Pin is reserved for this use.
- The non-activity of the microprocessor (Watchdog). WDO Pin is reserved for this use.

III.8.2 - Operating Interrupts (INT0 Pin)

There are five main sources of operating interrupts in the *Multi-HDLC* circuit :

- The HDLC receiver,
- The HDLC transmitter,
- The CI receiver,
- The Monitor receiver,
- The Monitor transmitter.

When an interrupt is generated by one of these functions, the interrupt controller :

- Collects all the information about the reasons of this interrupt,
- Stores them in external memory,
- Informs the microprocessor by positioning the INT0 pin in the high level.

Three interrupt queues are built in external memory to store the information about the interrupts :

- A single queue for the HDLC receivers and transmitters,
- One for the CI receivers,
- One for the monitor receivers.

The microprocessor takes the interrupts into account by reading the Interrupt Register (IR) of the interrupt controller.

This register informs the microprocessor of the interrupt source. The microprocessor will have information about the interrupt source by reading the corresponding interrupt queue (see Paragraph "Interrupt Register IR $(38)_H$" on Page 91).

On an overflow of the circular interrupt queues and an overrun or underrun of the different FIFO, the INT0 Pin is activated and the origin of the interrupt is stored in the Interrupt Register.

A 16 bits register is associated with the Tx Monitor interrupt. It informs the microprocessor of which transmitter has generated the interrupt (see Paragraph "Transmit Monitor Interrupt Register TMIR $(30)_H$" on Page 88).

III.8.3 - Time Base Interrupts (INT1 Pin)

The Time base interrupt is generated when an absence or an abnormal working of clock distribution is detected. The INT1 Pin is activated.

III.8.4 - Emergency Interrupts (WDO Pin)

The WDO signal is activated by an overflow of the watchdog register.

III.8.5 - Interrupt Queues

There are three different interrupt queues :

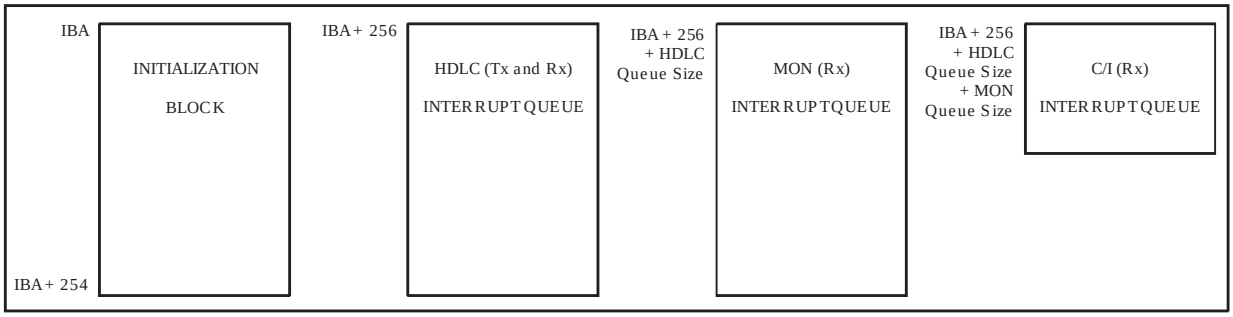
- Tx and Rx HDLC interrupt queue,
- Rx C/I interrupt queue,
- Rx Monitor interrupt queue.

Their length can be defined by software.

For debugging function, each interrupt word of the CI interrupt queue and monitor interrupt queue can be followed by a time stamped word. It is composed of a counter which runs in the range of 250µs. The counter is the same as the watchdog counter. Consequently, the watchdog function isn't available at the same time.

III - FUNCTIONAL DESCRIPTION (continued)

Figure 33 : The Three Circular Interrupt Memories



III.9 - Watchdog

This function is used to control the activity of the application. It is composed of a counter which counts down from an initial value loaded in the Timer register by the microprocessor.

If the microprocessor doesn't reset this counter before it is totally decremented, the external Pin WDO is activated ; this signal can be used to reset the microprocessor and all the application.

The initial time value of the counter is programmable from 0 to 15s in increments of 0.25ms.

At the reset of the component, the counter is automatically initialized by the value corresponding to 512ms which are indicated in the Timer register. The microprocessor must put WDR (IDCR Register) to"1" to reset this counter and to confirm that the application started correctly.

In the reverse case, the WDO signal could be used to reset the board a second time.

The FS signal (8kHz) divided by two or the XTAL1 signal (typically 32768kHz) divided by 8192 can be selected to increment the counter. At reset the watchdog is incremented by the XTAL1 signal.

III.10 - Reset

There are two possibilities to reset the circuit :

- by software,
- by hardware.

Each programmable register receives its default value. After that, the default value of each data register is stored in the associated memory except for Time slot Assigner memory.

III.11 - Boundary Scan

The Multi-HDLC is equipped with an IEEE Standard Test Access Port (IEEE Std 1149.1). The boundary scan technique involves the inclusion of a shift register stage adjacent to each component pin so that signals at component boundaries can be controlled and observed using scan testing principle. Its intention is to enable the test of on board interconnections and ASIC production tests.

The external interface of the Boundary Scan is composed of the signals TDI, TDO, TCK, TMS and TRST as defined in the IEEE Standard.

The values indicated in the tables from pag. 44 to pag. 67 are referred to V_{DD} ***= 5V if not otherwise specificated.***

IV - DC SPECIFICATIONS

IV.1 - Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{DD}	5V Power Supply Voltage	-0.5, 6.5	V
	Input or Output Voltage	-0.5, V_{DD} + 0.5	V
T_{stg}	Storage Temperature	-55, +125	°C

IV.2 - Power Dissipation

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
P	Power Dissipation	V_{DD} = 5V V_{DD} = 3.3V		300 100	400 130	mW mW

IV.3 - Recommended DC Operating Conditions

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{DD}	5V Power Supply Voltage		4.75		5.25	V
	3.3V Power Supply Voltage		3		3.6	V
T_{oper}	Operating Temperature		-40		+85	°C

Note 1 : All the following specifications are valid only within these recommended operating conditions.

IV.4 - TTL Input DC Electrical Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Low Level Input Voltage	V_{DD} = 5V; V_{DD} = 3.3V			0.8	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V; V_{DD} = 3.3V	2.0			V
I_{IL}	Low Level Input Current	V_I = 0V			1	µA
I_{IH}	High Level Input	V_I = V_{DD}			-1	µA
Vhyst	Schmitt Trigger hysteresis	V_{DD} = 5V V_{DD} = 3.3V	0.4 0.3	0.7 0.5	1 0.8	V V
VT+	Positive Trigger Voltage	V_{DD} = 5V V_{DD} = 3.3V		2 1.4	2.4 2	V V
VT-	Negative Trigger Voltage	V_{DD} = 5V V_{DD} = 3.3V	0.6 0.6	0.8 0.9		V V
C_{IN}	Input Capacitance (see Note 2)	f = 1MHz @ 0V		2	4	pF
C_{OUT}	Output Capacitance			4		
$C_{I/O}$	Bidirextional I/O Capacitance		4	8		

Note 2 : Excluding package

IV.5 - CMOS Output DC Electrical Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{OL}	Low Level Output Voltage	I_{OL} = X mA (see Note 3)			0.4	V
V_{OH}	High Level Output Voltage	I_{OH} = -X mA (see Note 3)	V_{DD}-0.4			V

Note 3 : X is the source/sink current under worst case conditions and is reflected in the name of the I/O cell according to the drive capability. X = 4 or 8mA.

IV.6 - Protection

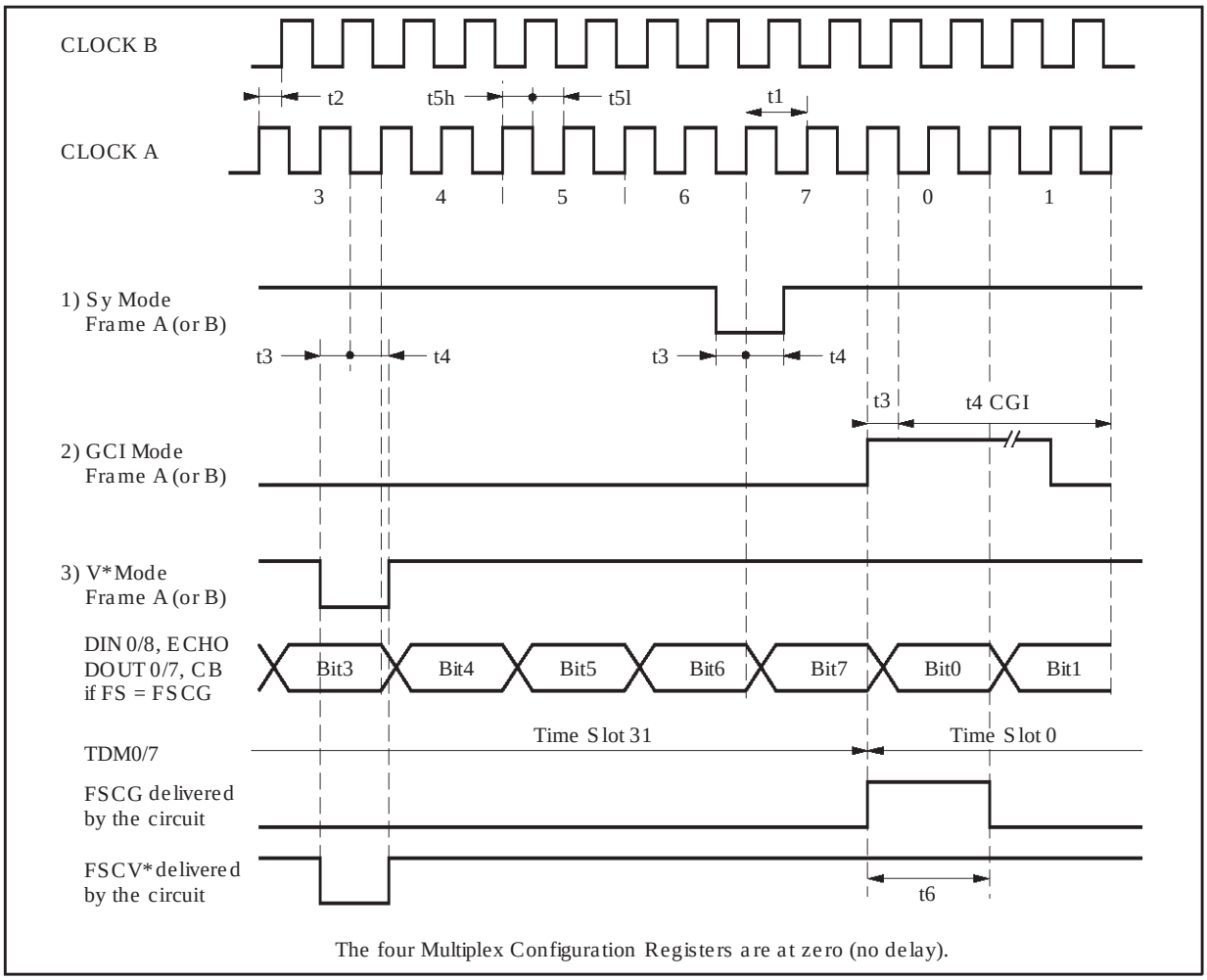
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VESD	Electrostatic Protection	C = 100pF, R = 1.5kΩ	2000			V

V - CLOCK TIMING

V.1 - Synchronization Signals delivered by the system

For one of three different input synchronizations which is programmed, FSCG and FSCV* signals delivered by the *Multi-HDLC* are in accordance with the figure hereafter.

Figure 34 : Clocks received and delivered by the *Multi-HDLC*



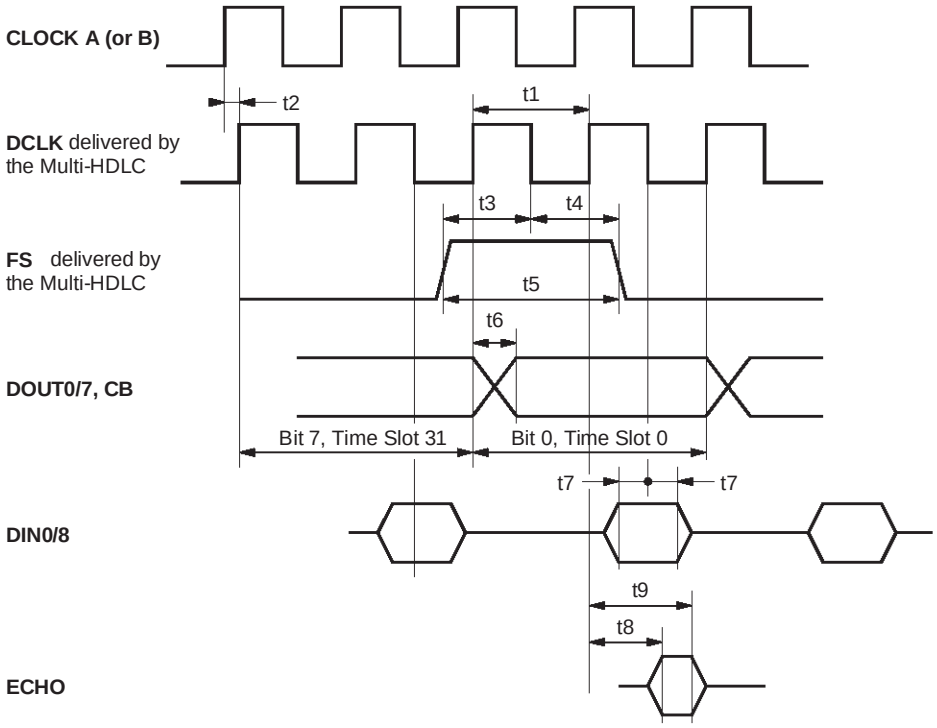
The four Multiplex Configuration Registers are at zero (no delay).

Symbol	Parameter	Min.	Typ.	Max.	Unit
t1	Clock Period if 4096kHz (3072) Clock Period if 8192kHz (6144)	239 (320) 120 (158)	244 (325) 122 (162)	249 (330) 125 (165)	ns ns
t2	Delay between Clock A and Clock B	- 60	0	+60	ns
t3	Set up time Frame A (or B)/CLOCK A (or B)	10		t1-10	ns
t4 t4GCI	Hold time Frame A (or B)/CLOCK A (or B)	10 10		t1-10 125000 - (t1 - 10)	ns
t5	Clock ratio t5h/t5l	75	100	125	%
t6	Duration of FSCG		488		ns

V - CLOCK TIMING (continued)

V.2 - TDM Synchronization

Figure 35 : Synchronization Signals received by the *Multi-HDLC*



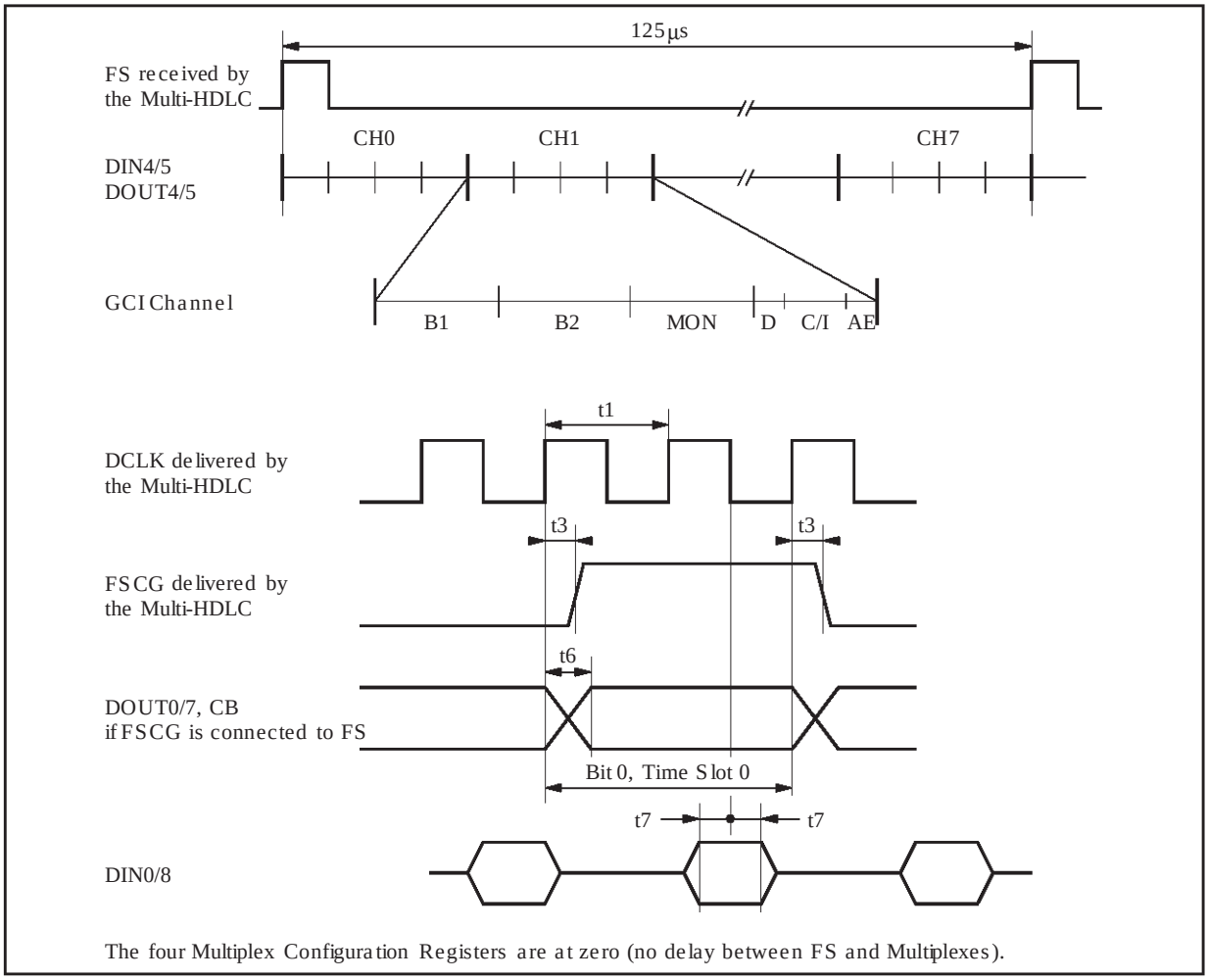
The four Multiplex Configuration Registers are at zero (no delay between FS and Multiplexes).

Symbol	Parameter	Min.	Typ.	Max.	Unit
t1	DCLK Clock Period if 4096kHz (3072) DCLK Clock Period if 2048kHz (1536)	Id CLOCKA or B	244 (325) 488 (651)	Id CLOCKA or B	ns ns
t2	Delay between CLOCK A or B and DCLK (30pF) V_{DD} = 5V V_{DD} = 3.3V		 5 20	 30 32	 ns ns
t3	Set-up Time FS/DCLK	20		t1-20	ns
t4	Hold Time FS/DCLK	20			ns
t5	Duration FS	244 (325)		125000-244	ns
t6	DCLK to Data 50pF DCLK to Data 100pF			50 100	ns
t7	Set-up Time Data/DCLK	20			ns
t7	Hold Time Data/DCLK	20			ns
t8	Set-up Echo/DCLK (rising edge)			155	ns
t9	Hold Time Echo/DCLK (rising edge)	205			ns

V - CLOCK TIMING (continued)

V.3 - GCI Interface

Figure 36 : GCI Synchro Signal delivered by the *Multi-HDLC*



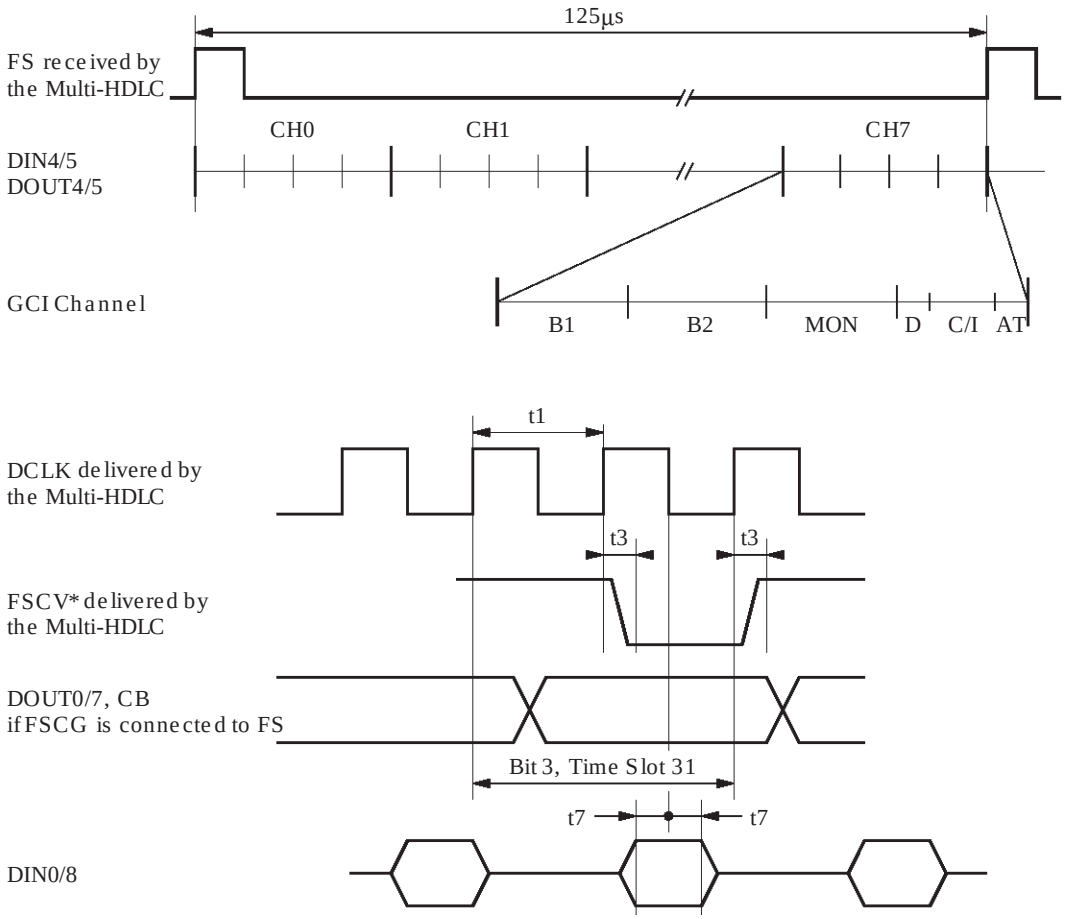
The four Multiplex Configuration Registers are at zero (no delay between FS and Multiplexes).

Symbol	Parameter	Min.	Typ.	Max.	Unit
t1	DCLK Clock Period if 4096kHz (3072) DCLK Clock Period if 2048kHz (1536)	Id CLOCK A or B	244 (325) 488 (651)	Id CLOCK A or B	ns ns
t3	DCLK to FSCG			20	ns
t5	Duration FS		244	125000-244	ns
t6	DCLK to Data 50pF DCLK to Data 100pF			50 100	ns ns
t7	Set-up Time Data/DCLK	20			ns
t7	Hold Time Data/DCLK	20			ns

V - CLOCK TIMING (continued)

V.4 - V* Interface

Figure 37 : V* Synchronization Signal delivered by the *Multi-HDLC*



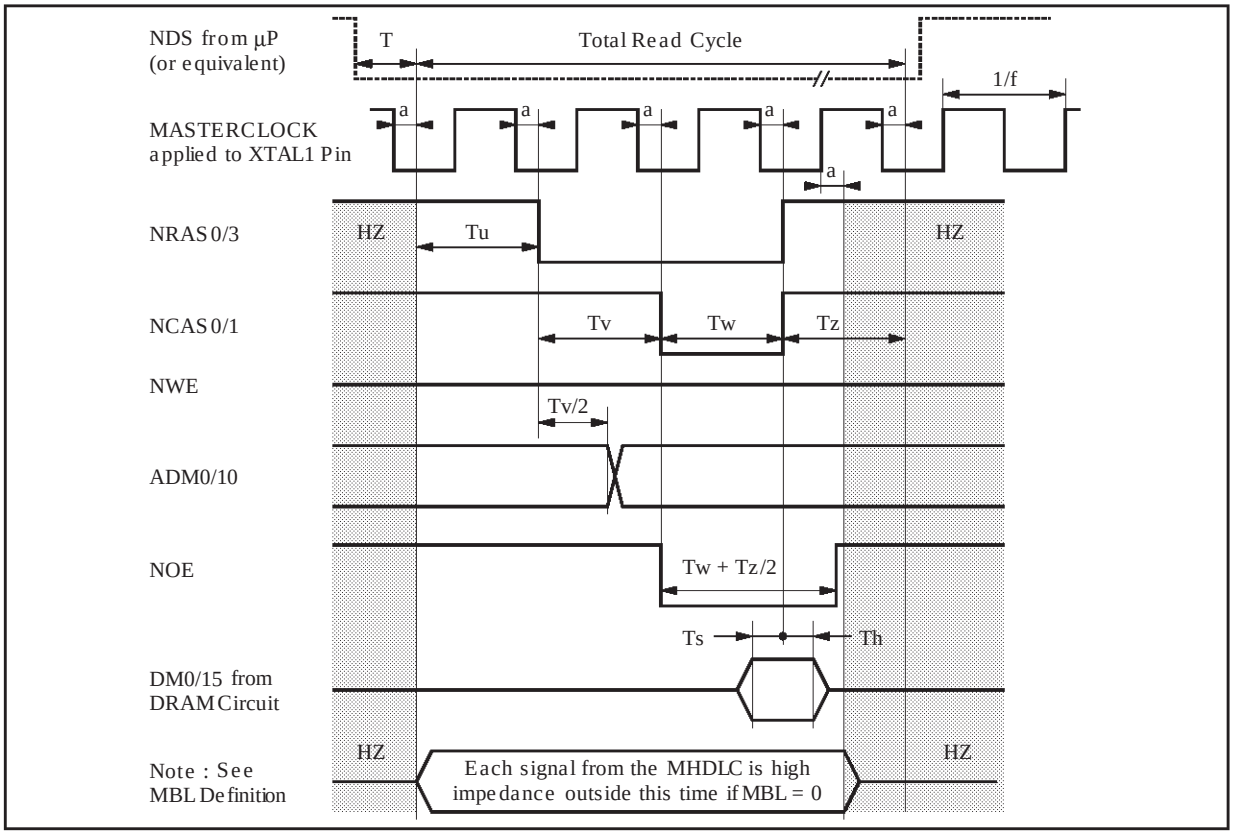
The four Multiplex Configuration Registers are at zero (no delay between FS and Multiplexes).

Symbol	Parameter	Min.	Typ.	Max.	Unit
t1	Clock Period 4096kHz		244		ns
t3	DCLK to FSCV*			20	ns
t5	Duration FSCV*		244		ns
t6	Clock to Data 50pF Clock to Data 100pF			50 100	ns nS
t7	Set-up Time Data/DCLK	20			ns
t7	Hold Time Data/DCLK	20			ns

V1 - MEMORY TIMING

VI.1 - Dynamic Memories

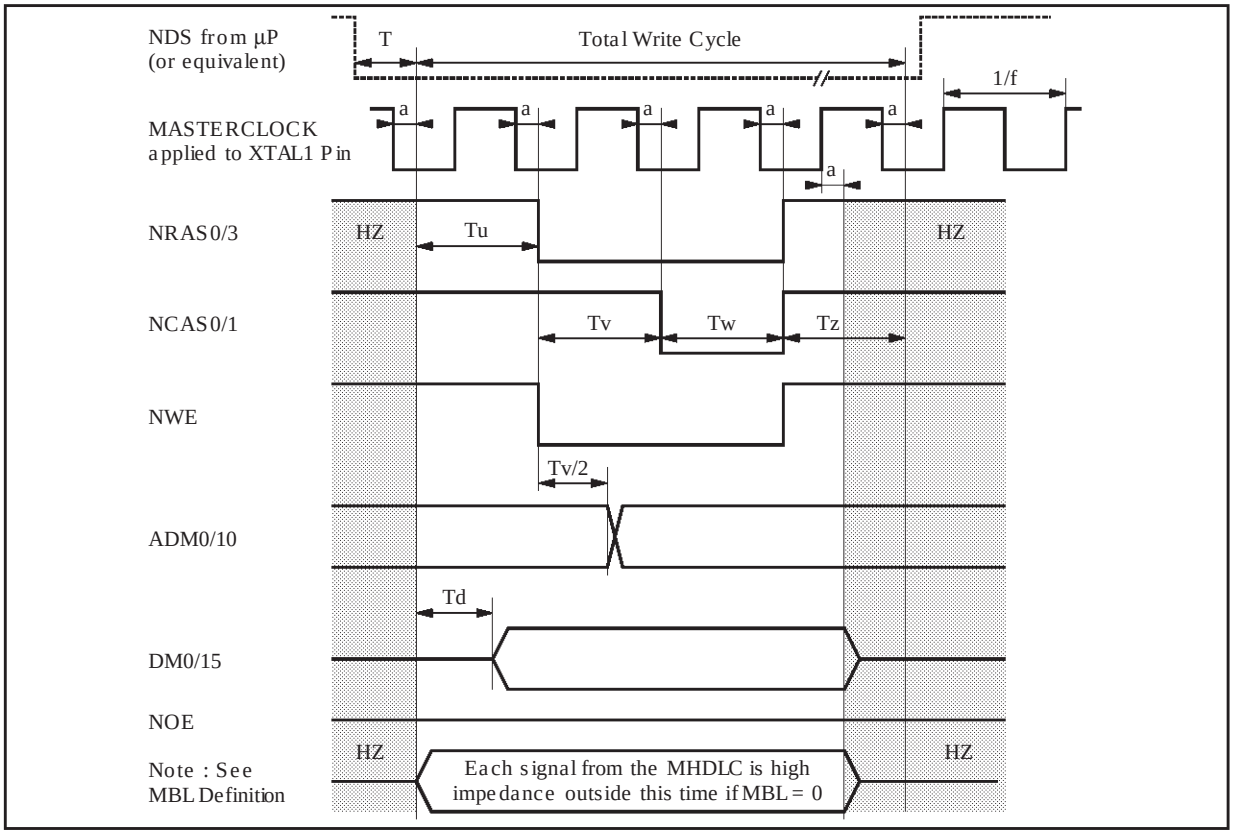
Figure 38 : Dynamic Memory Read Signals from the *Multi-HDLC*



Symbol	Parameter	Min.	Typ.	Max.	Unit
T	Delay between Data Strobe from the mP and beginning of cycle	2/f			
a	Delay between Masterclock and Edge of each signal delivered by the MHDLC (30pF) V_{DD} = 5V V_{DD} = 3.3V		 20 30	 40	 ns ns
Tw	Delay between NCAS Falling Edge and NCAS rising Edge	1/f		2/f	ns
Tz	Delay between NCAS Rising Edge and end of cycle	1/f		2/f	ns
Ts	Set-up Time Data /NCAS Rising Edge	20			ns
Th	Hold Time Data/NCAS Rising Edge	0			ns

VI - MEMORY TIMING (continued)

Figure 39 : Dynamic Memory Write Signals from the *Multi-HDLC*



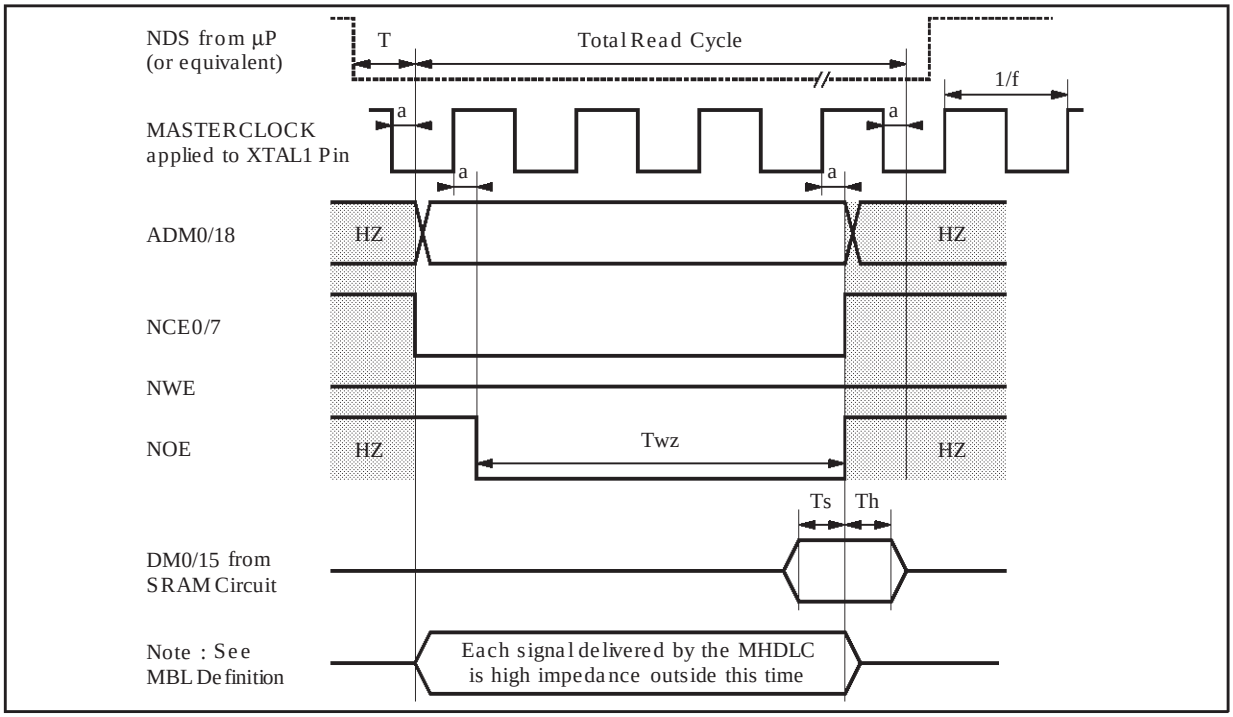
Symbol	Parameter	Min.	Typ.	Max.	Unit
f	f : Masterclock Frequency	32		33	MHz
Tu	Delay between beginning of cycle and NRAS Falling Edge	1/f		2/f	ns
Tv	Delay between NRAS Falling Edge and NCAS Falling Edge	1/f		2/f	ns
Tw	Delay between NCAS Falling Edge and NWE Rising Edge	1/f		2/f	ns
Tz	Delay between NWE Rising Edge and end of cycle	1/f		2/f	ns
Tv/2	Delay between NRAS Falling Edge and address change	1/2f		1/f	ns
Td	Data Valid after beginning of cycle (30 pF)	1/f		1/f	ns

Note : Total Cycle : Tu + Tv + Tw + Tz

VI - MEMORY TIMING (continued)

VI.2 - Static Memories

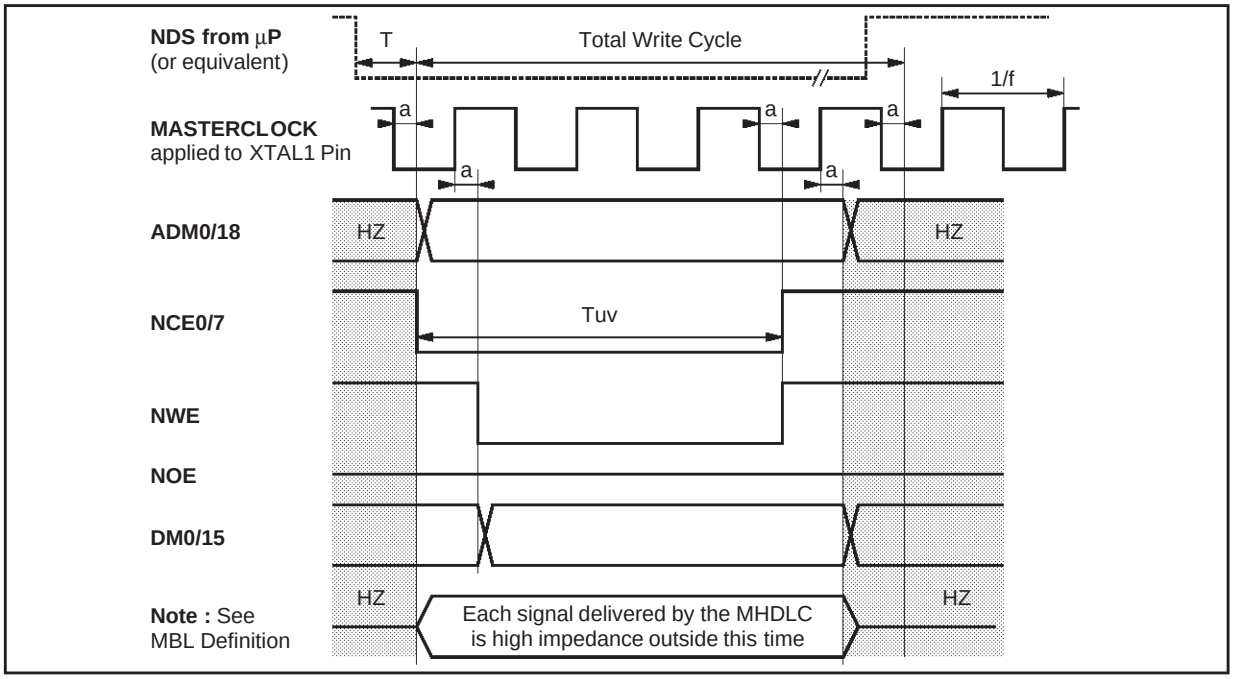
Figure 40 : Static Memory Read Signals from the *Multi-HDLC*



Symbol	Parameter	Min.	Typ.	Max.	Unit
T	Delay between Data Strobe delivered by the mP and beginning of cycle	2/f			
1/f	f: Masterclock frequency				
	Total read cycle: Twz + 1/f				
a	Delay between Masterclock and Edge of each signal delivered by the MHDLC (30pF) V_{DD} = 5V V_{DD} = 3.3V		 20 30	 40	 ns ns
Twz	NOE width	1/f		4/f	ns
Ts	Set-up Time Data /NOE Rising Edge	20			ns
Th	Hold Time Data /NOE Rising Edge	0			ns

VI - MEMORY TIMING (continued)

Figure 41 : Static Memory Write Signals from the *Multi-HDLC*



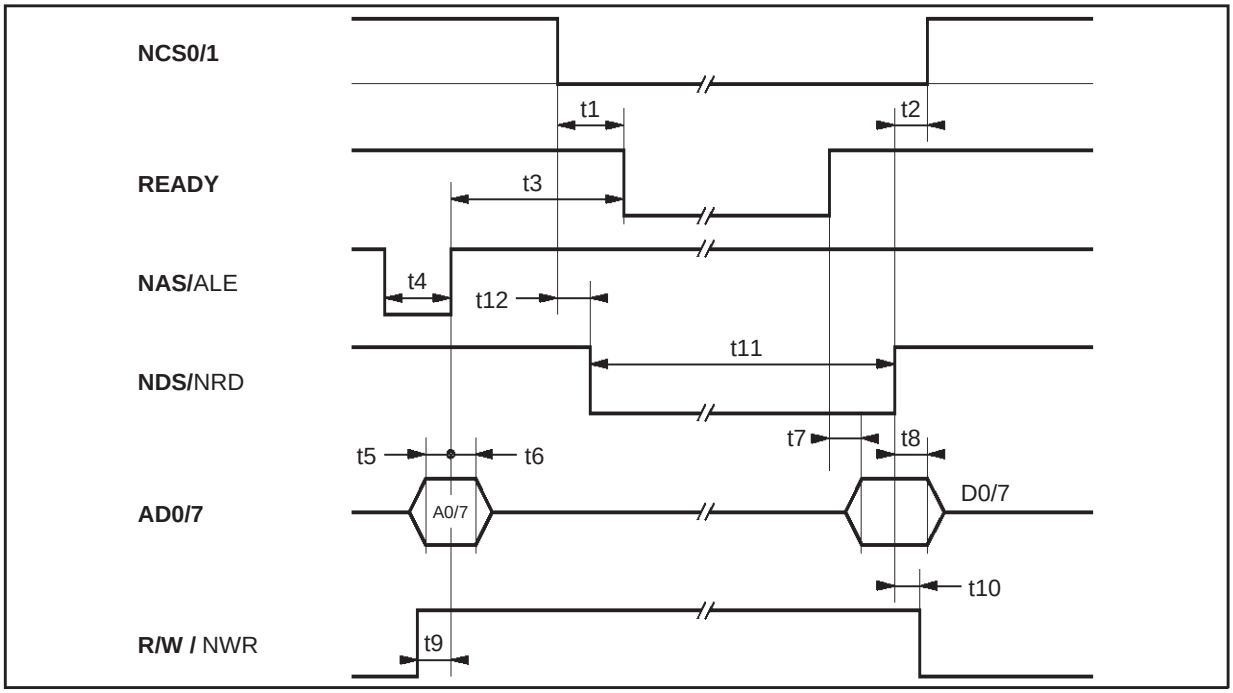
Symbol	Parameter	Min.	Typ.	Max.	Unit
T	Delay between Data Strobe delivered by the µP and beginning of cycle	2/f			
1/f	f : Masterclock frequency				
a	Delay between Masterclock and Edge of each signal delivered by the MHDLC (30pF) V_{DD} = 5V V_{DD} = 3.3V		 30	 20 40	 ns ns
Tuv	NCE width	1/f		4/f	ns

Note : Total Write Cycle : Tuv + 1/f

VII - MICROPROCESSOR TIMING

VII.1 - ST9 Family MOD0=1, MOD1=0, MOD2=0

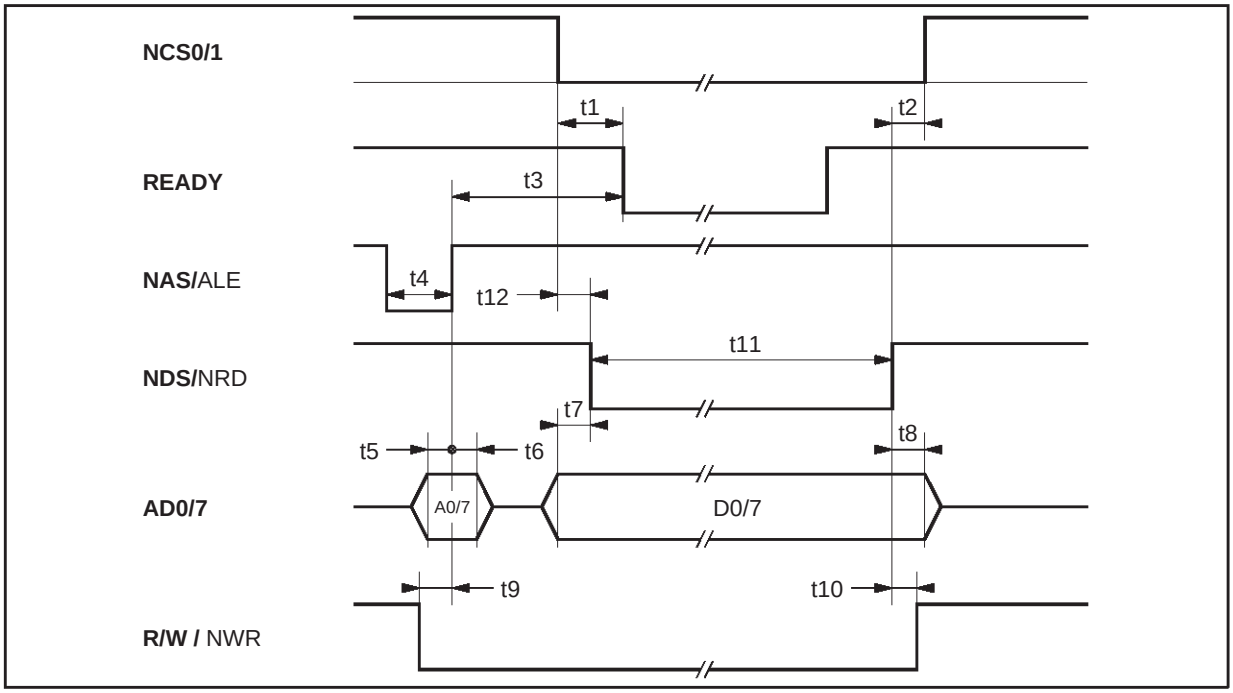
Figure 42 : ST9 Read Cycle



Symbol	Parameter	Min.	Typ.	Max.	Unit
t1	Delay Ready / Chip Select (if t3 > t1), (30pF) Delay when immediate access	0		 98	ns ns
t2	Hold Time Chip Select /Data Strobe	14			ns
t3	Delay Ready / NAS (if t1 > t3), (30pF) Delay when immediate access	0		 98	ns ns
t4	Width NAS	20			ns
t5	Set-up Time Address / NAS	9			ns
t6	Hold Time Address / NAS	9			ns
t7	Data Valid after Ready	0		15	ns
t8	Data Valid after Data Strobe (30pF)	0		15	ns
t9	Set-up Time R/W /NAS	15			ns
t10	Hold Time R/W / Data Strobe	15			ns
t11	Width NDS when immediate access	50			ns
t12	Delay NDS / NCS	5			ns

VII - MICROPROCESSOR TIMING (continued)

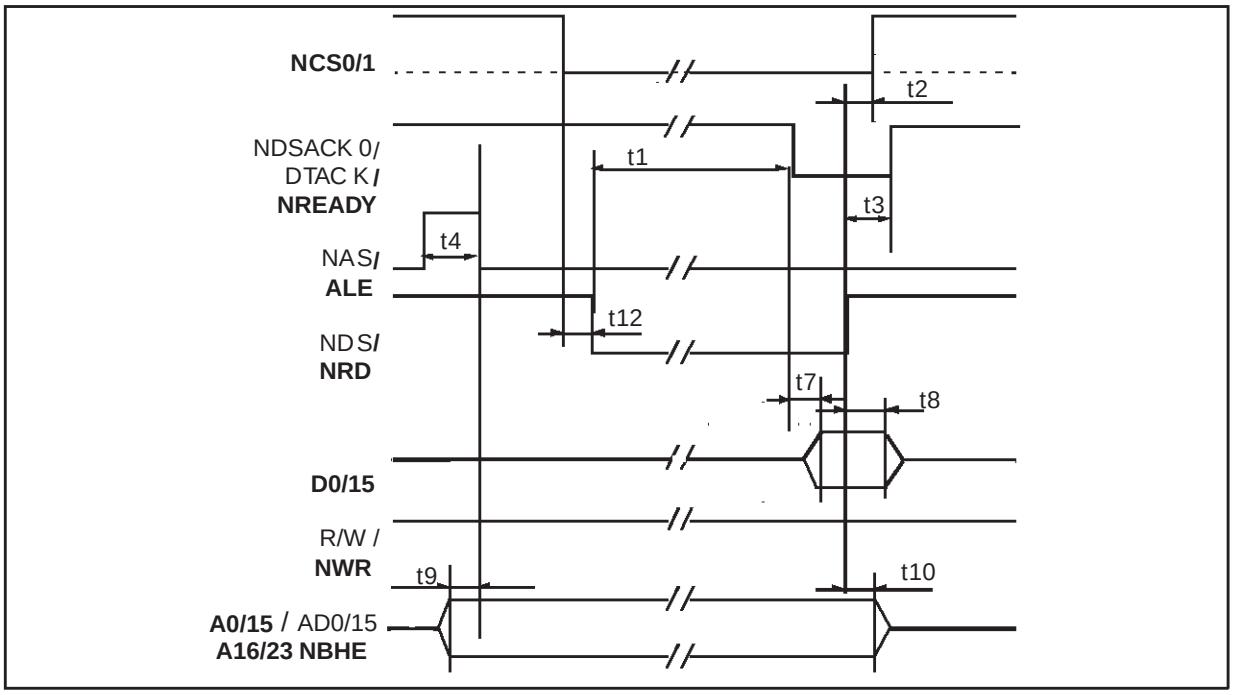
Figure 43 : ST9 Write Cycle



Symbol	Parameter	Min.	Typ.	Max.	Unit
t1	Delay Ready / Chip Select (if t3 > t1), (30pF) Delay when immediate access	0		 98	ns NS
t2	Hold Time Chip Select / Data Strobe	14			ns
t3	Delay Ready / NAS (if t1 > t3), (30pF) Delay when immediate access	0		 98	ns NS
t4	Width NAS	20			ns
t5	Set-up Time Address / NAS	9			ns
t6	Hold Time Address / NAS	9			ns
t7	Set-up Time Data / Data Strobe	-15			ns
t8	Hold Time Data / Data Strobe	15			ns
t9	Set-up Time R/W / NAS	15			ns
t10	Hold Time R/W / Data Strobe	15			ns
t11	Width NDS when immediate access	50			ns
t12	Delay NDS / NCS	5			ns

VII - MICROPROCESSOR TIMING (continued)
VII.2 - ST10/C16x mult. A/D, MOD0 = 1, MOD1 = 0, MOD2 = 1

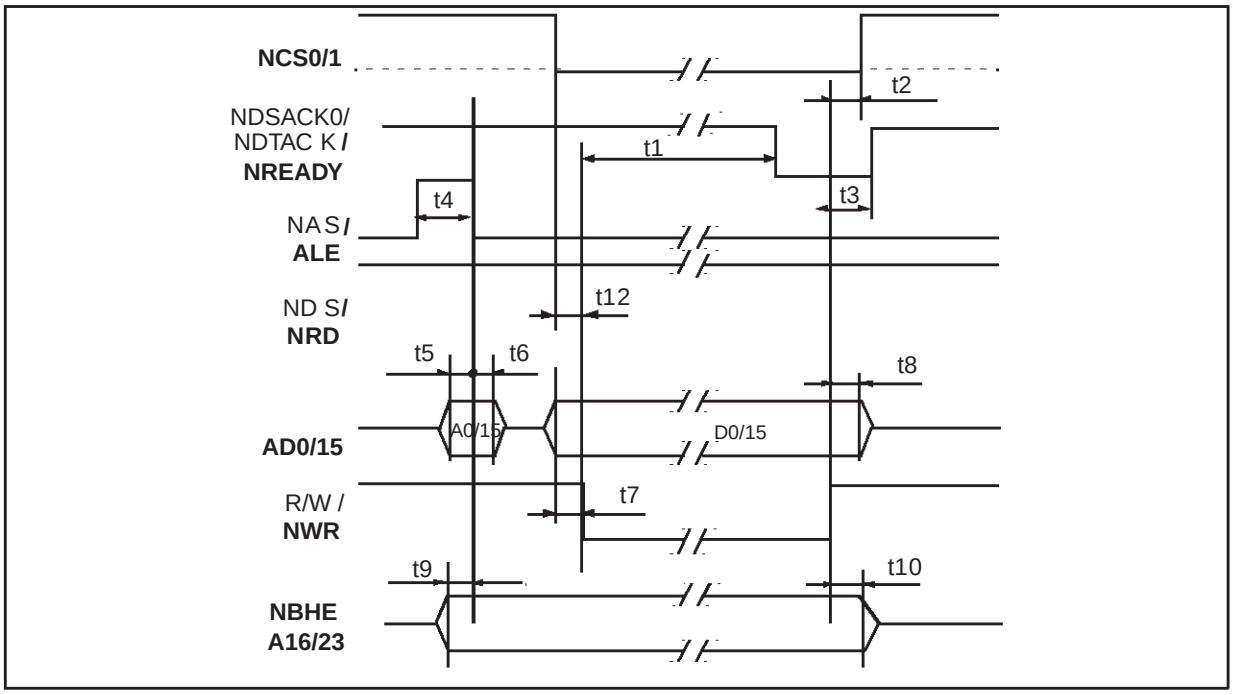
Figure 44 : ST10 (C16x) Read Cycle; Multiplexed A/D



Symbol	Parameter	Min.	Typ.	Max.	Unit
t1	Delay Not Ready/NRD (if NCS0/1 = 0), (30pF) Delay when immediate access V_{DD} = 5V V_{DD} = 3.3V	0		 98 108	ns ns ns
t2	Hold Time Chip Select / NRD	10			ns
t3	Delay Not Ready / NRD rising edge Delay when immediate access V_{DD} = 5V V_{DD} = 3.3V	0		 98 108	ns ns ns
t4	Width ALE	20			ns
t5	Set-up Time Address / ALE	5			ns
t6	Hold Time Address /ALE V_{DD} = 5V V_{DD} = 3.3V	 5 10			 ns ns
t7	Data valid after ready	0		15	ns
t8	Data bus at high impedance after NRD (30pF)	0	15		ns
t9	Set-up Time NBHE, Address A 16/23/ALE	5			ns
t10	Hold Time NBHE / NRD	10			ns
t12	Delay NRD / NCS	0			ns

VII - MICROPROCESSOR TIMING (continued)

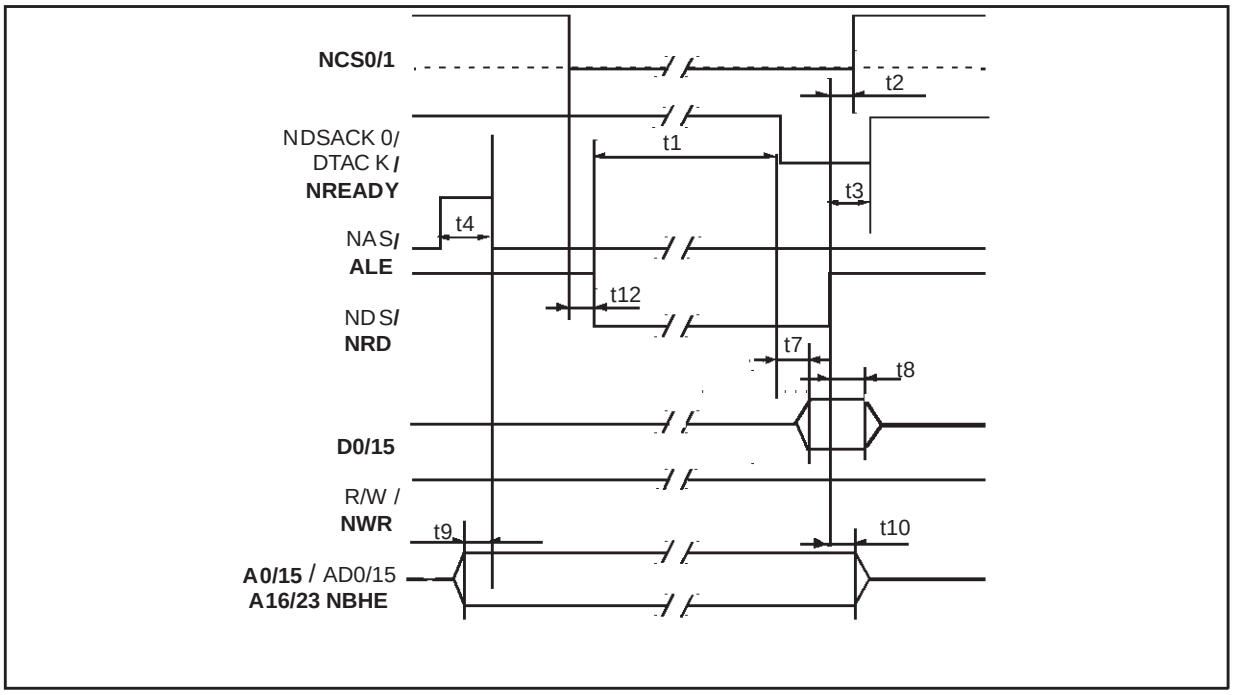
Figure 45 : ST10 (C16x) Write Cycle; Multiplexed A/D



Symbol	Parameter	Min.	Typ.	Max.	Unit
t1	Delay Not Ready/ALE (if NCS0/1 = 0), (30pF) Delay when immediate access V_{DD} = 5V V_{DD} = 3.3V	0		 98 108	ns ns ns
t2	Hold Time Chip Select / NWR	10			ns
t3	Delay Not Ready / NRD rising edge Delay when immediate access V_{DD} = 5V V_{DD} = 3.3V	0		 98 108	ns ns ns
t4	Width ALE	20			ns
t5	Set-up Time Address / ALE	5			ns
t6	Hold Time Address /ALE V_{DD} = 5V V_{DD} = 3.3V	 5 10			 ns ns
t7	Set up time Data/NWR	-15			ns
t8	Set up time NBHE-Address A 16/23/ALE	0			ns
t9	Set-up Time NBHE, Address A 16/23/ALE	5			ns
t10	Hold Time NBHE / NWR	10			ns
t12	Delay NWR / NCS	0			ns

VII - MICROPROCESSOR TIMING (continued)
VII.3 - ST10/C16x demult. A/D, MOD0 = 0, MOD1 = 1, MOD0 = 1

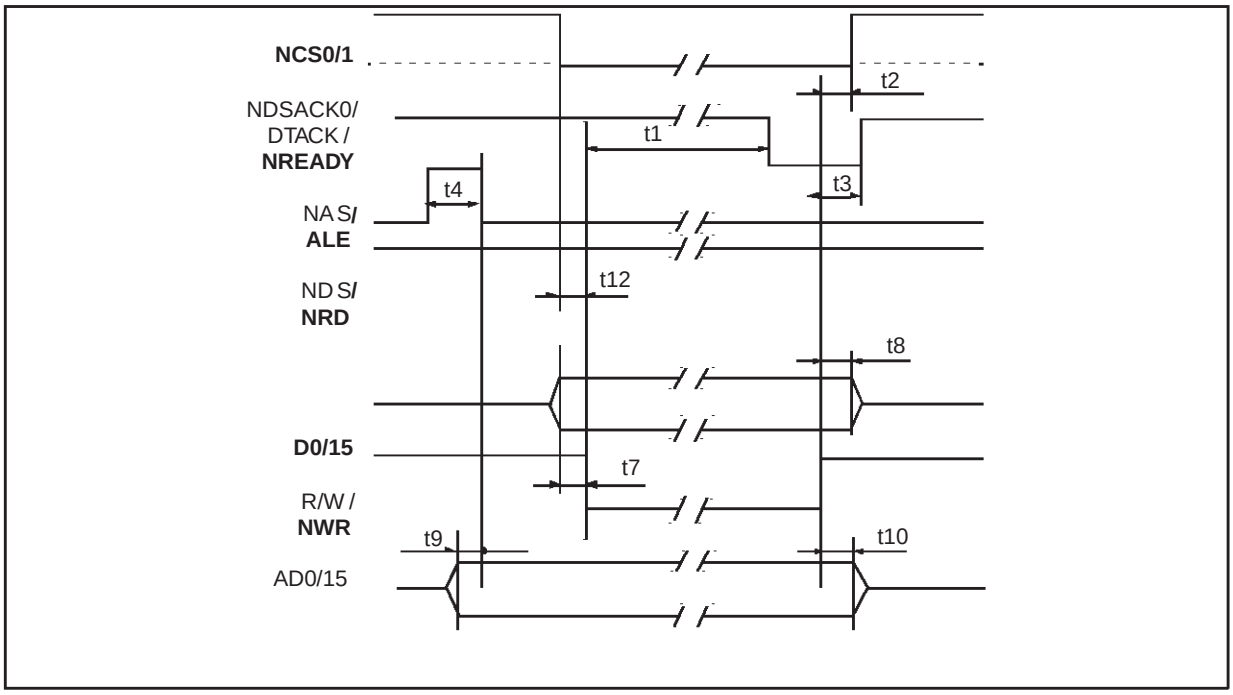
Figure 46 : ST10 (C16x) Read Cycle; Demultiplexed A/D



Symbol	Parameter	Min.	Typ.	Max.	Unit
t1	Delay Not Ready/NRD (if NCS0/1 = 0), (30pF) Delay when immediate access V_{DD} = 5V V_{DD} = 3.3V	0		 98 108	ns ns ns
t2	Hold Time Chip Select / NRD	10			ns
t3	Delay Not Ready / NRD rising edge Delay when immediate access V_{DD} = 5V V_{DD} = 3.3V	0		 98 108	ns ns ns
t4	Width ALE	20			ns
t7	Data valid after NOTREADY falling efge (30pF)	0		15	ns
t8	Data bus at high impedance after NRD (30pF)	0		15	ns
t9	Set-up Time NBHE, Address AD0/15, A16/ALE	5			ns
t10	Hold Time NBHE / Address ADO/15, A16/23/NRD	10			ns
t12	Delay NRD / NCS	0			ns

VII - MICROPROCESSOR TIMING (continued)

Figure 47 : ST10 (C16x) Write Cycle; Demultiplexed A/D

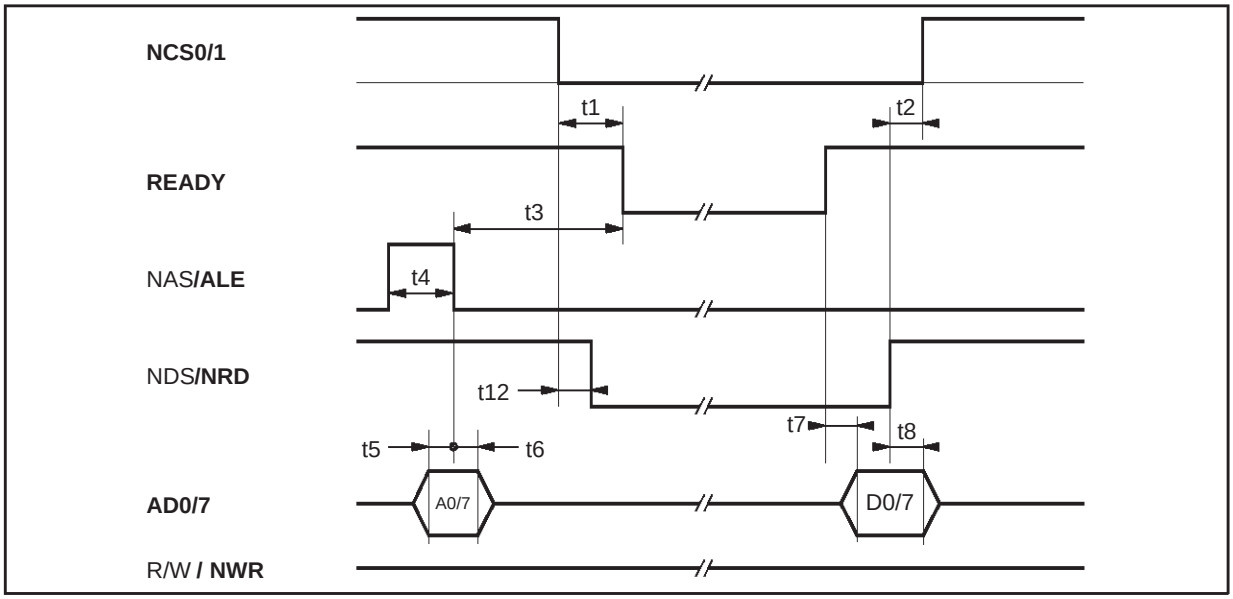


Symbol	Parameter	Min.	Typ.	Max.	Unit
t1	Delay Not Ready/NWR (if NCS0/1 = 0), (30pF) Delay when immediate access V_{DD} = 5V V_{DD} = 3.3V	0		 98 108	ns ns ns
t2	Hold Time Chip Select / NRD	10			ns
t3	Delay Not Ready / NWR rising edge Delay when immediate access V_{DD} = 5V V_{DD} = 3.3V	0		 98 108	ns ns ns
t4	Width ALE	20			ns
t7	Set up time Data/NWR	-15			ns
t8	Hold time Data/NWR	15			ns
t9	Set-up Time NBHE, Address AD0/15, A16/23/ALE	5			ns
t10	Hold Time NBHE, Address AD0/15, A16/23 NWR	10			ns
t12	Delay NWR / NCS	0			ns

VII - MICROPROCESSOR TIMING (continued)

VII.4 - 80C188 MOD0=1, MOD1=1, MOD2=0

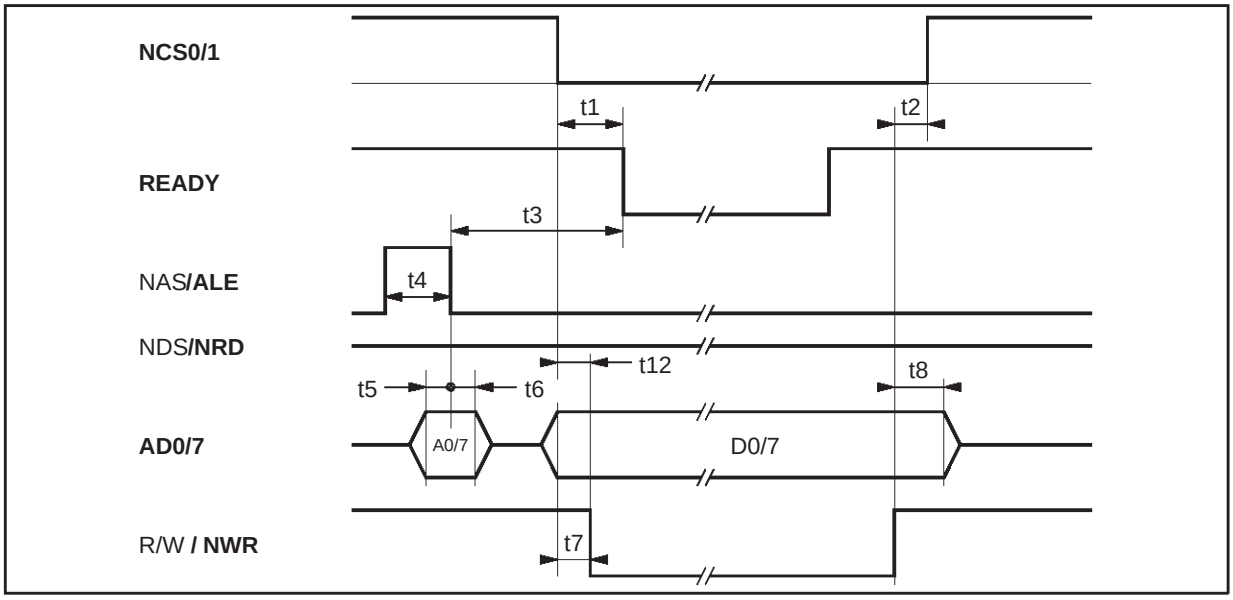
Figure 48 : 80C188 Read Cycle



Symbol	Parameter	Min.	Typ.	Max.	Unit
t1	Delay Ready / Chip Select (if t3 > t1), (30pF) Delay when immediate access V_{DD} = 5V V_{DD} = 3.3V	0		 98 108	ns ns ns
t2	Hold Time Chip Select / NRD	10			ns
t3	Delay Ready / ALE (if t1 > t3), (30pF) Delay when immediate access V_{DD} = 5V V_{DD} = 3.3V	0		 98 108	ns ns ns
t4	Width ALE	20			ns
t5	Set-up Time Address / ALE	5			ns
t6	Hold Time Address / ALE V_{DD} = 5V V_{DD} = 3.3V	 5 10			 ns ns
t7	Data Valid after Ready	0		15	ns
t8	Data Valid after NRD (30pF)	0			ns
t12	Delay NDS / NCS	0			ns

VII - MICROPROCESSOR TIMING (continued)

Figure 49 : 80C188 Write Cycle

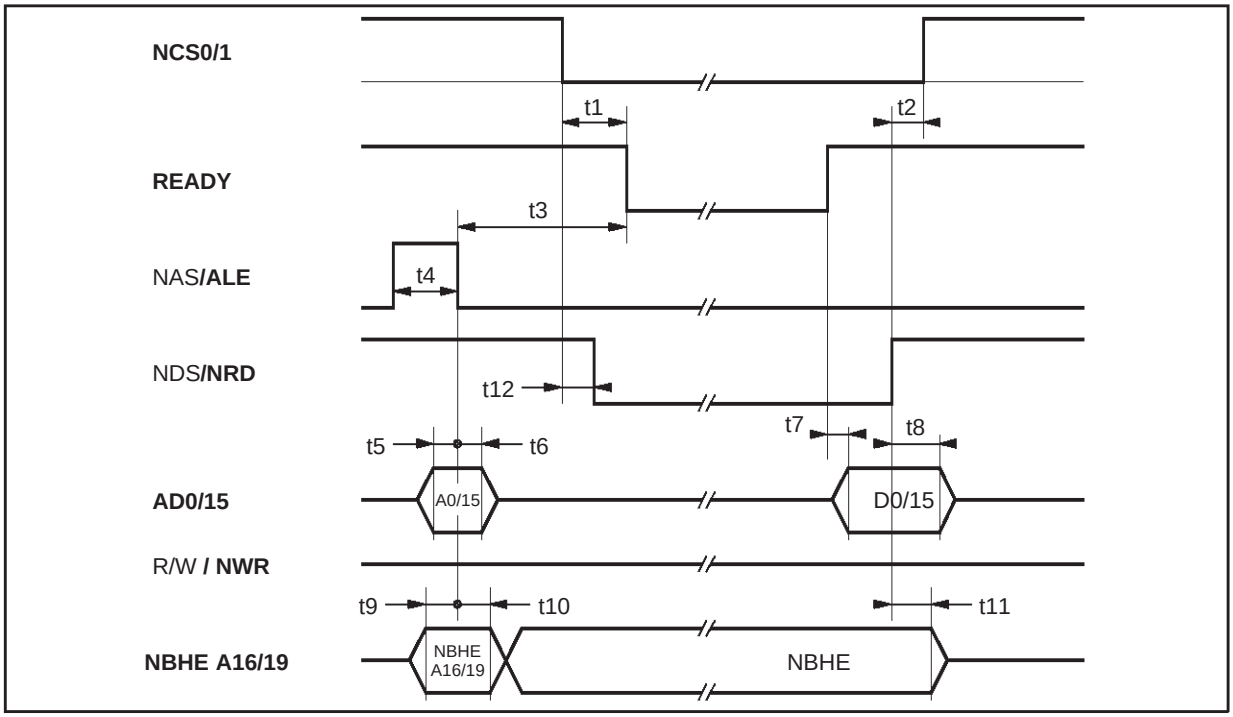


Symbol	Parameter	Min.	Typ.	Max.	Unit
t1	Delay Ready / Chip Select (if t3 > t1), (30pF) Delay when immediate access V_{DD} = 5V V_{DD} = 3.3V	0		 98 108	ns ns ns
t2	Hold Time Chip Select / NWR	10			ns
t3	Delay Ready / ALE (if t1 > t3), (30pF) Delay when immediate access V_{DD} = 5V V_{DD} = 3.3V	0		 98 108	ns ns ns
t4	Width ALE	20			ns
t5	Set-up Time Address / ALE	5			ns
t6	Hold Time Address / ALE V_{DD} = 5V V_{DD} = 3.3V	 5 10			 ns ns
t7	Set-up Time Data / NWR	-15			ns
t8	Hold Time Data / NWR	15			ns
t12	Delay NWR / NCS	0			ns

VII - MICROPROCESSOR TIMING (continued)

VII.5 - 80C186 MOD0=1, MOD1=1, MOD2=1

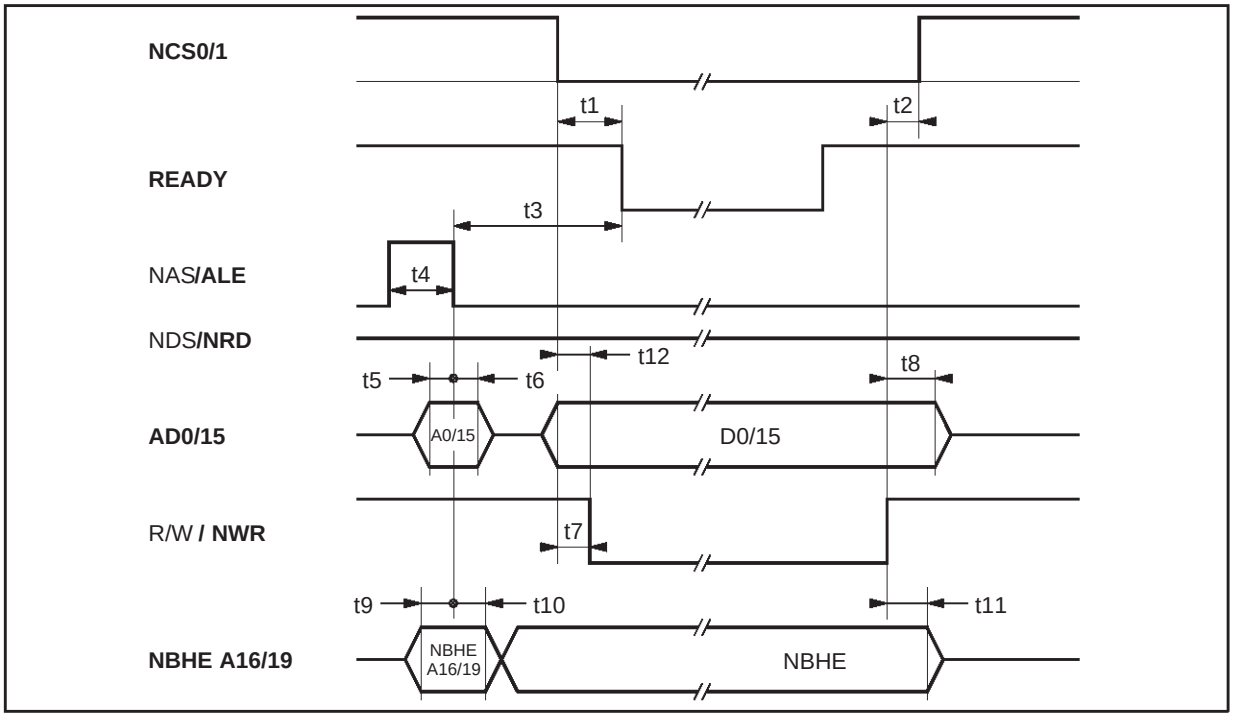
Figure 50 : 80C186 Read Cycle



Symbol	Parameter	Min.	Typ.	Max.	Unit
t1	Delay Ready / Chip Select (if t3 > t1), (30pF) Delay when immediate access V_{DD} = 5V V_{DD} = 3.3V	0		 98 108	 ns ns
t2	Hold Time Chip Select / NRD	10			ns
t3	Delay Ready / ALE (if t1 > t3), (30pF) Delay when immediate access V_{DD} = 5V V_{DD} = 3.3V	0		 98 108	 ns ns
t4	Width ALE	20			ns
t5	Set-up Time Address / ALE	5			ns
t6	Hold Time Address / ALE V_{DD} = 5V V_{DD} = 3.3V	 5 10			 ns ns
t7	Data Valid after Ready	0		15	ns
t8	Data Valid after NRD (30pF)	0		15	ns
t9	Set-up Time NBHE-Address A16/19 / ALE	5			ns
t10	Hold Time Address A1619 / NRD	10			ns
t11	Hold Time NBHE- / NRD	10			ns
t12	Delay NRD / NCS	0			ns

VII - MICROPROCESSOR TIMING (continued)

Figure 51 : 80C186 Write Cycle

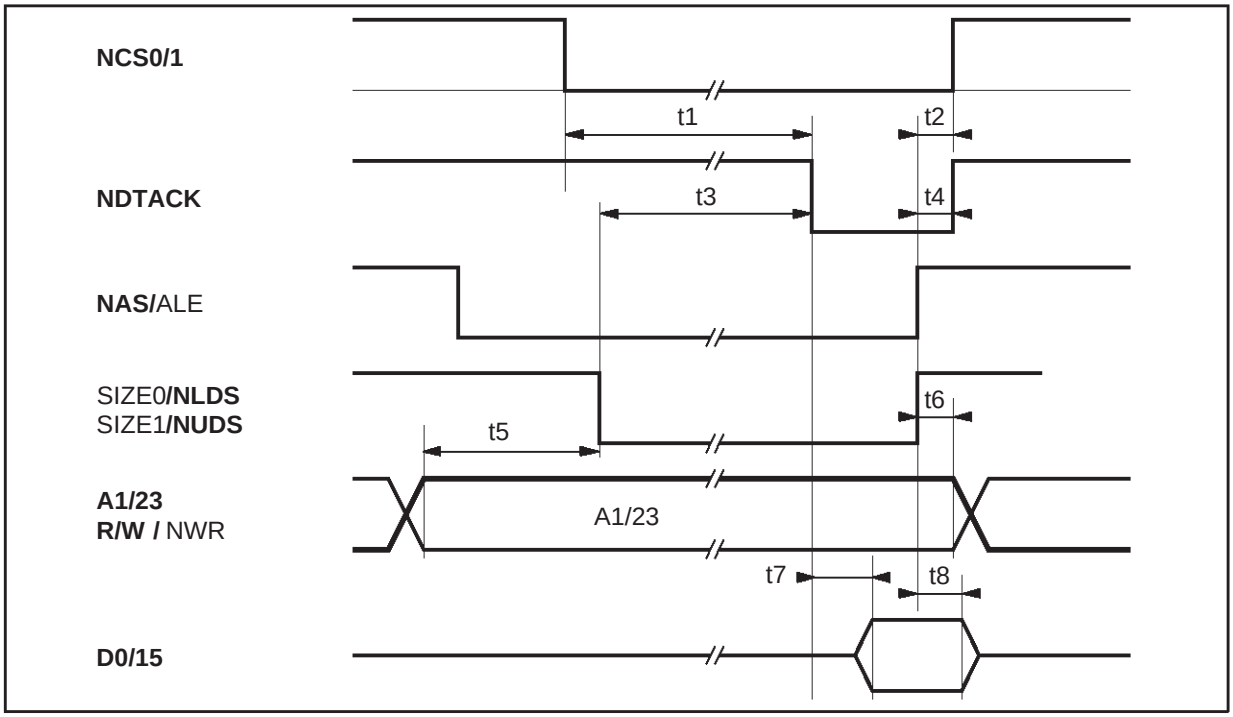


Symbol	Parameter	Min.	Typ.	Max.	Unit
t1	Delay Ready / Chip Select (if t3 > t1), (30pF) Delay when immediate access V_{DD} = 5V V_{DD} = 3.3V	0		 98 108	ns ns ns
t2	Hold Time Chip Select / NWR	10			ns
t3	Delay Ready / ALE (if t1 > t3), (30pF) Delay when immediate access V_{DD} = 5V V_{DD} = 3.3V	0		 98 108	ns ns ns
t4	Width ALE	20			ns
t5	Set-up Time Address / ALE	5			ns
t6	Hold Time Address / ALE V_{DD} = 5V V_{DD} = 3.3V	 5 10			 ns ns
t7	Set-up Time Data / NWR	-15			ns
t8	Hold Time Data / NWR	15			ns
t9	Set-up Time NBHE-Address A16/19 / ALE	5			ns
t10	Hold Time Address 16/19 / ALE	10			ns
t11	Hold Time NBHE- / NWR	10			ns
t12	Delay NWR / NCS	0			ns

VII - MICROPROCESSOR TIMING (continued)

VII.6 - 68000 MOD0=0, MOD1=0, MOD2=1

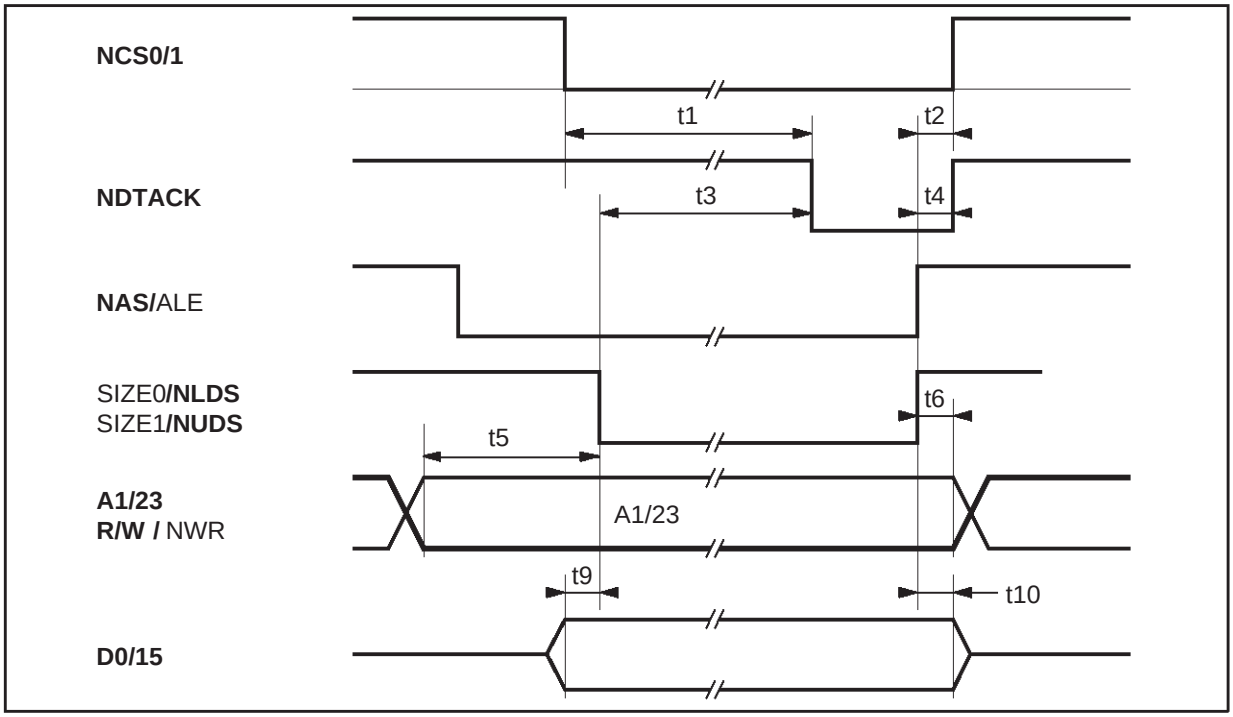
Figure 52 : 68000 Read Cycle



Symbol	Parameter	Min.	Typ.	Max.	Unit
t1	Delay NDTACK / NCS0/1 (if t3 > t1), (30pF) Delay when immediate access V_{DD} = 5V V_{DD} = 3.3V	 0 0		 98 108	 ns ns
t2	Hold Time Chip Select / NLDS-NUDS	0			ns
t3	Delay NDTACK / NLDS-NUDS Falling Edge (if t1> t3), (30pF) Delay when immediate access V_{DD} = 5V V_{DD} = 3.3V	 0 0		 98 108	 ns ns
t4	Delay NDTACK / NLDS-NUDS Rising Edge V_{DD} = 5V V_{DD} = 3.3V	 0 0		 20 30	 ns ns
t5	Set-up Time Address and R/W / last NLDS-NUDS or NCS	0			ns
t6	Hold Time Address and R/W / NLDS-NUDS	0			ns
t7	Data Valid after NDTACK Falling Edge (30pF)	0		15	ns
t8	Data High Impedance after NLDS-NUDS Rising Edge (30pF)	0		15	ns

VII - MICROPROCESSOR TIMING (continued)

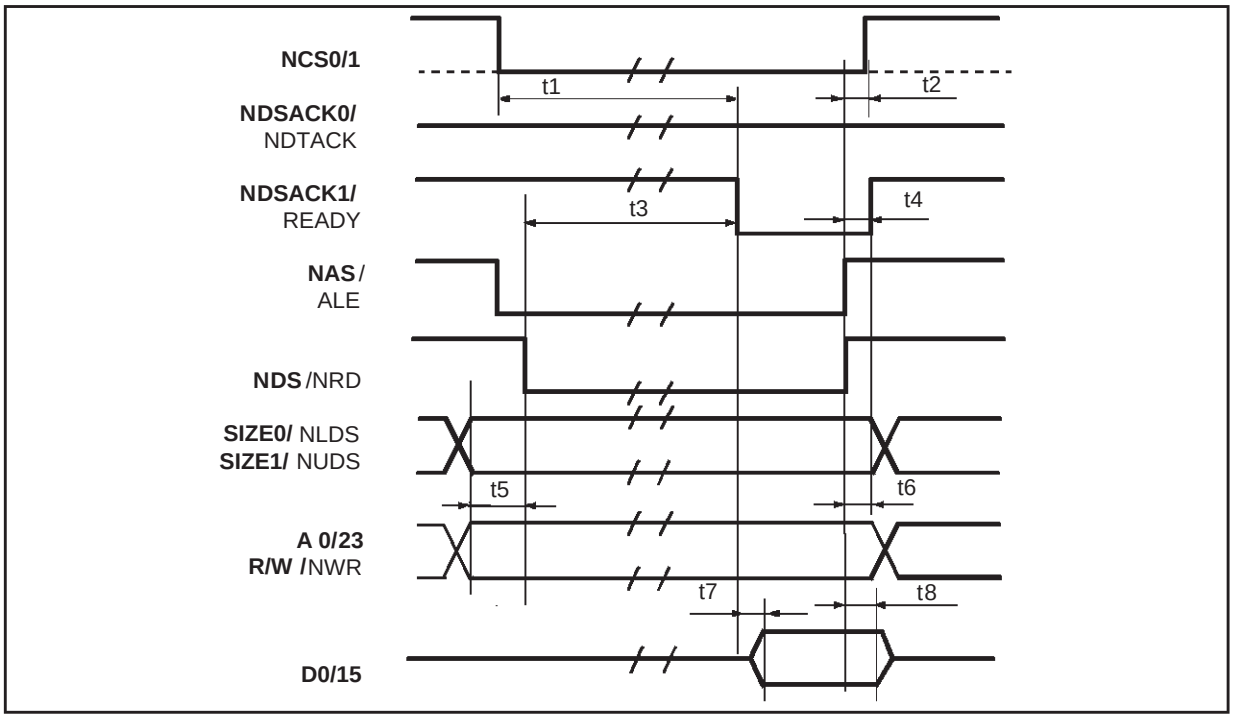
Figure 53 : 68000 Write Cycle



Symbol	Parameter	Min.	Typ.	Max.	Unit
t1	Delay NDTACK / NCS0/1 (if t3 > t1), (30pF) Delay when immediate access V_{DD} = 5V V_{DD} = 3.3V	 0 0		 98 108	 ns ns
t2	Hold Time Chip Select / NLDS-NUDS	0			ns
t3	Delay NDTACK / NLDS-NUDS Falling Edge (if t1> t3), (30pF) Delay when immediate access V_{DD} = 5V V_{DD} = 3.3V	 0 0		 98 108	 ns ns
t4	Delay NDTACK / NLDS-NUDS Rising Edge V_{DD} = 5V V_{DD} = 3.3V			 20 30	 ns ns
t5	Set-up Time Address and R/W / last NLDS-NUDS or NCS	0			ns
t6	Hold Time Address / NLDS-NUDS	0			ns
t9	Set-up Time Data / NLDS-NUDS	15			ns
t10	Hold Time Data / NLDS-NUDS	7			ns

VII - MICROPROCESSOR TIMING (continued)
VII.7 - 68020 MOD0=0, MOD1=0, MOD2=0

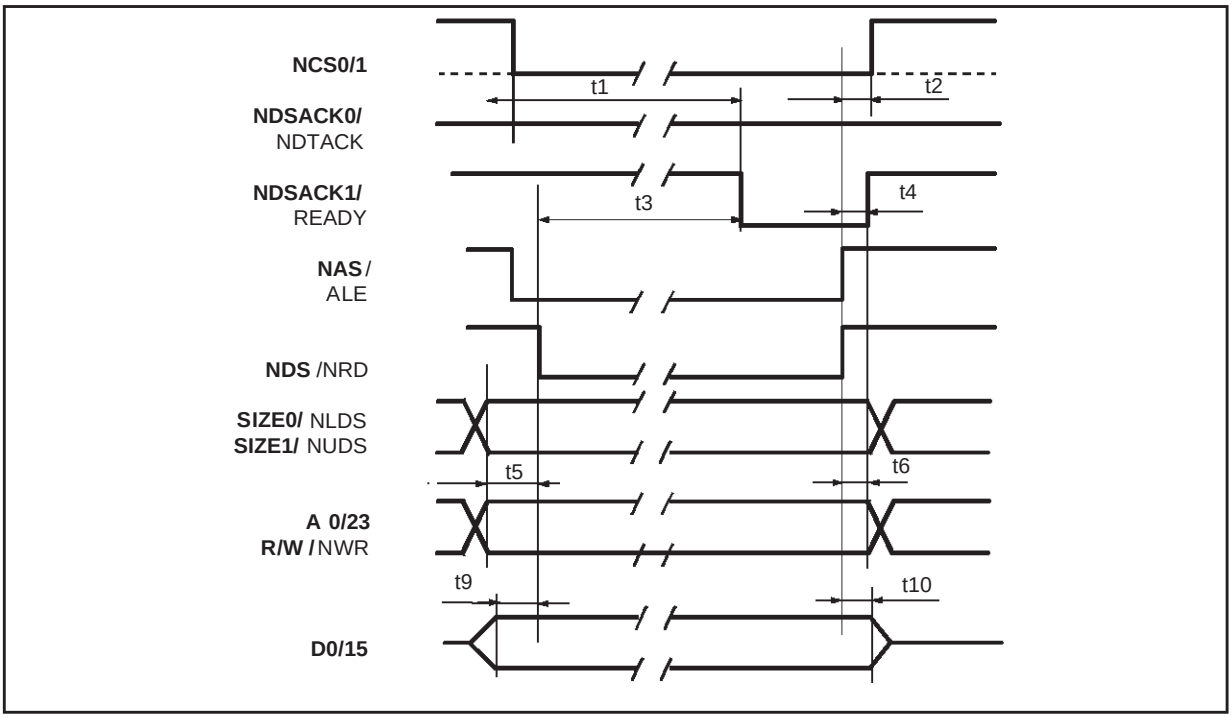
Figure 54 : 68020 Read Cycle



Symbol	Parameter	Min.	Typ.	Max.	Unit
t1	Delay NDTACK / NCS0/1 (if t3 > t1), (30pF) Delay when immediate access V_{DD} = 5V V_{DD} = 3.3V	 0 0		 98 108	 ns ns
t2	Hold Time Chip Select / NDS rising edge	0			ns
t3	Delay NDSACK1 / NDS Falling Edge (if t1> t3), (30pF) Delay when immediate access V_{DD} = 5V V_{DD} = 3.3V	 0 0		 98 108	 ns ns
t4	Delay NDSACK1 / NDS Rising Edge V_{DD} = 5V V_{DD} = 3.3V			 20 30	 ns ns
t5	Set-up Time Address and R/W/last NDS or NCS	0			ns
t6	Hold Time Address / NDS	0			ns
t7	Data valid before NDSACK1 falling edge (30pF)	0		15	ns
t8	Data High Impedance after NDS (30pF)	0		15	ns

VII - MICROPROCESSOR TIMING (continued)

Figure 55 : 68020 Write Cycle

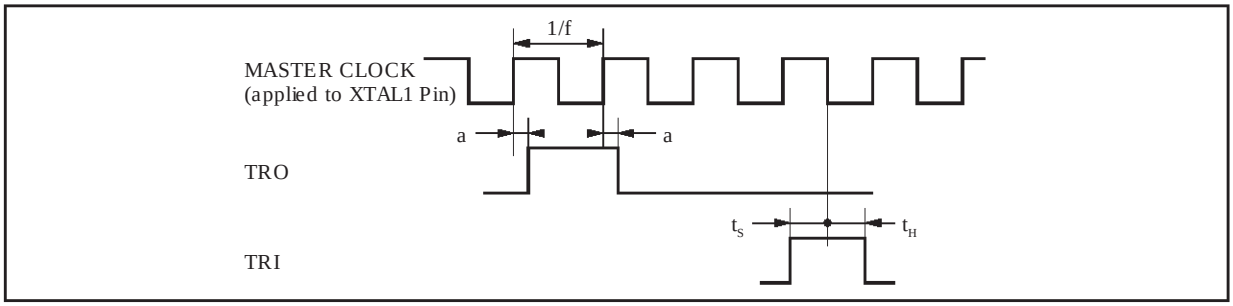


Symbol	Parameter	Min.	Typ.	Max.	Unit
t1	Delay NDTACK / NCS0/1 (if t3 > t1), (30pF) Delay when immediate access V_{DD} = 5V V_{DD} = 3.3V	 0 0		 98 108	 ns ns
t2	Hold Time Chip Select / NDS rising edge	0			ns
t3	Delay NDSACK1 / NDS Falling Edge (if t1> t3), (30pF) Delay when immediate access V_{DD} = 5V V_{DD} = 3.3V	 0 0		 98 108	 ns ns
t4	Delay NDSACK 1/ NDS Rising Edge V_{DD} = 5V V_{DD} = 3.3V			 20 30	 ns ns
t5	Set-up Time Address and R/W/last NDS or NCS	0			ns
t6	Hold Time Address / NDS	0			ns
t9	Set-up Time Data / NDS	0			ns
t10	Hold Time Data / NDS	7			ns

VII - MICROPROCESSOR TIMING (continued)

VII.8 - Token Ring Timing

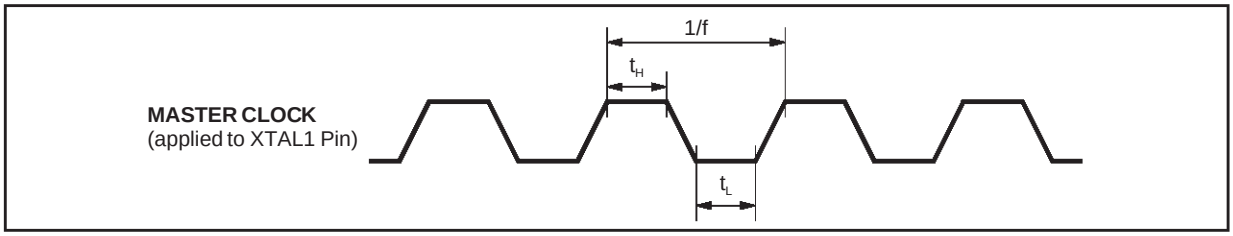
Figure 56 : Token Ring



Symbol	Parameter	Min.	Typ.	Max.	Unit
f	f : Masterclock frequency		32.768		MHz
a	Delay between Masterclock Rising Edge and Edges of TRO Pulse delivered by the MHDLC (10pF) V_{DD} = 5V V_{DD} = 3.3V			25 30	ns ns
t_S	Set-up Time TRI/Masterclock Masterclock Falling Edge	5			ns
t_H	Hold Time TRI/Masterclock Falling Edge	5		0	ns

VII.9 - Master Clock Timing

Figure 57 : Master Clock



Symbol	Parameter	Min.	Typ.	Max.	Unit
f	Masterclock Frequency	30	32.768	33	MHz
1/f	Masterclock Period	30.3	30.5	33.3	ns
tH	Masterclock High	12			ns
tL	Masterclock Low	12			ns

Crystal parameters:

a) frequency f (typically 32768.00 kHz)

b) Mode fundamental

c) Resonance parallel

d) Load Capacity Cl= 30pF

in accordance with 2 capacitors (47 pF each of them) the first capacitor is soldered nearest pin 2 (XTAL1) and nearest the ground, the second capacitor is soldered nearest pin 3 (XTAL2) and nearest the ground.

e) Serial resistor 40 Ohms max

To reduce the drive level, the Crystal parameters can be:

a) frequency f (typically 32768.00 kHz)

b) Mode fundamental

c) Resonance parallel

d) Load Capacity Cl = 20pF

in accordance with 2 capacitors (33 pF each of them)

e) Serial resistor 40 Ohms max

N.B It is not necessary to add an external bias resistor between XTAL1 pin and XTAL2 pin. This resistor is inside the circuit.

VIII - INTERNAL REGISTERS

'Not used' bits (Nu) are accessible by the microprocessor but the use of these bits by software is not recommended.

'Reserved' bits are not implemented in the circuit. However, it is not recommended to use this address.

VIII.1 - Identification and Dynamic Command Register - IDCR (00)H

bit15							bit8	bit7							bit 0
C15	C14	C13	C12	C11	C10	C9	C8	C7	C6	C5	C4	C3	C2	C1	C0

When this register is read by the microprocessor, the circuit code C0/15 is returned. Reset has no effect on this register.
C0/3 indicates the version.
C4/7 indicates the revision.
C8/11 indicates the foundry.
C12/15 indicates the type.
Example : this code is (0010)H for the first sample.

When this register is written by the microprocessor then :

bit15							bit8	bit7							bit 0
Nu	Nu	Nu	Nu	Nu	Nu	Nu	Nu	Nu	Nu	Nu	Nu	Nu	RSS	WDR	TL

TL : TOKEN LAUNCH
When TL is set to 1 by the microprocessor, the token pulse is launched from the TRO pin (Token Ring Output pin). This pulse is provided to the TRI pin (Token Ring Input pin) of the next circuit in the applications where several *Multi-HDLC*s are connected to the same shared memory.

WDR : WATCHDOG RESET.
When the bit 1 (WDR) of this register is set to 1 by the microprocessor, the watchdog counter is reset.

RSS : RESET SOFTWARE
When the bit 2 (RSS) of this register is set to 1 by the microprocessor, the circuit is reset (Same action as reset pin).

After writing this register, the values of these three bits return to the default value.

VIII.2 - General Configuration - GCR (02)H

bit15							bit8	bit7							bit 0
SBV	MBL	AFAB	SCL	BSEL	SELB	CSD	HCL	SYN1	SYN0	D7	EVM	TSV	TRD	PMA	WDD
After reset $(0000)_H$															

WDD : Watch Dog Disable
WDD = 1, the Watch Dog is masked : WDO pin stays at "0".
WDD = 0, the Watch Dog generates an "1" on WDO pin if the microprocessor has not reset the Watch Dog during the duration programmed in Timer Register.

PMA : Priority Memory Access
PMA = 1, if the token ring has been launched it is captured and kept in order to authorize memory accesses.
PMA = 0, memory is accessible only if the token is present; after one memory access the token is re-launched from TRO pin of the current circuit to TRI pin of the next circuit.

TRD : Token Ring Disable
TRD = 1, if the token has been launched, the token ring is stopped and destroyed ; memory accesses are not possible. The token will not appear on TRO pin.
TRD = 0, the token ring is authorized ; when the token will be launched, it will appear on TRO pin.

VIII - INTERNAL REGISTERS (continued)

TSV : Time Stamping Validated
TSV = 1, the time stamping counter becomes a free binary counter and counts down from 65535 to 0 in step of 250ms (Total = 16384ms). So if an event occurs when the counter indicates A and if the next event occurs when the counter indicates B then : t = (A-B) x 250ms is the time which has passed between the two events which have been stored in memory by the Interrupt Controller (for Rx C/I and Rx MON CHANNEL only).
TSV = 0, the counter becomes a decimal counter. The Timer Register and this decimal counter constitute a Watch Dog or a Timer.

EVM : EXTERNAL VCXO MODE
EVM=1, VCXO Synchronization Counter is divided by 32.
EVM=0, VCXO Synchronization Counter is divided by 30.

D7 : HDLC connected to MATRIX
D7 = 1, the transmit HDLC is connected to matrix input 7, the DIN7 signal is ignored.
D7 = 0, the DIN7 signal is taken into account by the matrix, the transmit HDLC is ignored by the matrix.

SYN0/1: SYNCHRONIZATION
SYN0/1 : these two bits define the signal applied on FRAMEA/B inputs. For more details, see "Synchronization signals delivered by the system. V.1.

SYN1	SYN0	Signal applied on FRAMEA/B inputs
0	0	SYIinterface
0	1	GCI Interface (the signal defines the first bit of the frame)
1	0	Vstar Interface (the signal defines thrid bit of the frame)
1	1	Not used

HCL : HIGH BIT CLOCK
This bit defines the signal applied on CLOCKA/B inputs.
HCL = 1, bit clock signal is at 8192kHz
HCL= 0, bit clock signal is at 4096kHz

CSD : Clock Supervision Deactivation
CSD = 1, the lack of selected clock is not seen by the microprocessor; INT1 is masked.
CSD = 0, when the selected clock disappears the INT1 pin goes to 5V, 250ms after this disappearance.

SELB : SELECT B
SELB = 1, FRAME B and CLOCK B must be selected.
SELB = 0, FRAME A and CLOCK A must be selected.

BSEL : B SELECTED (this bit is read only)
BSEL = 1, FRAME B and CLOCK B are selected.
BSEL = 0, FRAME A and CLOCK A are selected.

SCL : Single Clock
This bit defines the signal delivered by DCLK output pin.
SCL = 1, Data Clock is at 2048kHz.
SCL = 0, Data Clock is at 4096kHz.

AFAB : Advanced Frame A/B Signal
AFAB = 1, the advance of Frame A Signal and Frame B Signal is 0.5 bit time versus the signal frame A (or B) drawn in Figure 34.
AFAB = 0, Frame A Signal and Frame B Signal are in accordance with the clock timing (see : Synchronization signals delivered by the Figure 45).

VIII - INTERNAL REGISTERS (continued)

MBL : Memory Bus Low impedance
MBL = 1, the shared memory bus is at low impedance between two memory cycles.
The memory bus includes Control bits, Data bits, Address bits. One *Multi-HDLC* is connected to the shared memory.
MBL = 0, the shared memory bus is at high impedance between two memory cycles.
Several Muti-HDLCs can be connected to the shared memory. One pull up resistor is recommended on each wire.

SBV : Six Bit Validation (A, E, S1/S4 bits). Global validation for 16 channels (Upstream and downstream).
SBV = 1, in reception, the six bit word (A, E, S1/S4) located in the same timeslot as D channel can be received from any input timeslot; when this word is received identical twice consecutively, it is stored in the external shared memory and an interrupt is generated if not masked (like the reception of primitive from C/I channel). See "RECEIVE Command/Indicate INTERRUPT" on page 97.
Sixteen independent detections are performed if the contents of any input timeslot is switched in the timeslot 4n+3 of two GCI multiplexes (corresponding to DOUT4 and DOUT5) with (0 £ n £ 7). Only the contents of D channel will be transmitted from input timeslot to GCI multiplexes. From ISDN channels to GCI channels on page 34.
In transmission a six bit word (A, E, S1/S4) can be transmitted continuously to any output timeslot via the TCIR. See "Transmit Command/Indicate Register TCIR (2A)H" on page 76. This word (A, E, S1/S4) is set instead of primitive (C1, C2, C3, C4) and A, E bits received from the timeslot 4n+3 of two GCI multiplexes and the new contents of this timeslot 4n+3 must be switched on the selected output timeslot.
SBV=0, the 16 six bit detections are not validated.

VIII.3 - Input Multiplex Configuration Register 0 - IMCR0 (04)H

bit15							bit8	bit7							bit 0
LP3	DEL3	ST(3)1	ST(3)0	LP2	DEL2	ST(2)1	ST(2)0	LP1	DEL1	ST(1)1	ST(1)0	LP0	DEL0	ST(0)1	ST(0)0
After reset $(0000)_H$															

See definition in next Paragraph.

VIII.4 - Input Multiplex Configuration Register 1 - IMCR1 (06)H

bit15							bit8	bit7							bit 0
LP7	DEL7	ST(7)1	ST(7)0	LP6	DEL6	ST(6)1	ST(6)0	LP5	DEL5	ST(5)1	ST(5)0	LP4	DEL4	ST(4)1	ST(4)0
After reset $(0000)_H$															

ST(i)0 : STEP0 for each Input Multiplex i($0 \le i \le 7$), delayed or not.

ST(i)1 : STEP1 for each Input Multiplex i($0 \le i \le 7$), delayed or not.

DEL(i); : DELAYED Multiplex i($0 \le i \le 7$).

DEL (i)	ST (i) 1	ST (i) 0	STEP for each Input Multiplex 0/7 delayed or not
X	0	0	Each received bit is sampled at 3/4 bit-time without delay. First bit of the frame is defined by Frame synchronization Signal.
1	0	1	Each received bit is sampled with 1/2 bit-time delay.
1	1	0	Each received bit is sampled with 1 bit-time delay.
1	1	1	Each received bit is sampled with 2 bit-time delay.
0	0	1	Each received bit is sampled with 1/2 bit-time advance.
0	1	0	Each received bit is sampled with 1 bit-time advance
0	1	1	Each received bit is sampled with 2 bit-time advance.

When IMTD = 0 (bit of SMCR), DEL = 1 is not taken into account by the circuit.
1/2 bit time 244ns if TDM at 2048 kHz,
1/2 bit time 122ns if TDM at 4096 kHz.

VIII - INTERNAL REGISTERS (continued)

LP (i) : LOOPBACK 0/7
LPi = 1, Output Multiplex i is put instead of Input Multiplex i ($0 \le i \le 7$). LOOPBACK is transparent or not in accordance with OMVi (bit of Output Multiplex Configuration Register).
LPi = 0, Normal case, Input Multiplex i($0 \le i \le 7$) is taken into account.

N.B. If DIN4 and DIN5 are GCI Multiplexes : then ST(4)1 = ST(4)0 = 0 and ST(5)1 = ST(5)0 = 0 normally.

VIII.5 - Output Multiplex Configuration Register 0 - OMCR0 (08)H

bit15							bit8	bit7							bit 0
OMV3	DEL3	ST(3)1	ST(3)0	OMV2	DEL2	ST(2)1	ST(2)0	OMV1	DEL1	ST(1)1	ST(1)0	OMV0	DEL0	ST(0)1	ST(0)0
After reset $(0000)_H$															

See definition in next Paragraph.

VIII.6 - Output Multiplex Configuration Register 1 - OMCR1 (0A)H

bit15							bit8	bit7							bit 0
OMV7	DEL7	ST(7)1	ST(7)0	OMV6	DEL6	ST(6)1	ST(6)0	OMV5	DEL5	ST(5)1	ST(5)0	OMV4	DEL4	ST(4)1	ST(4)0
After reset $(0000)_H$															

ST(i)0 : STEP0 for each Output Multiplex i($0 \le i \le 7$), delayed or not.
ST(i)1 : STEP1 for each Output Multiplex i($0 \le i \le 7$), delayed or not.
DEL(i); : DELAYED Multiplex i($0 \le i \le 7$).

DEL (i)	ST (i) 1	ST (i) 0	STEP for each Output Multiplex 0/7 delayed or not
X	0	0	Each bit is transmitted on the rising edge of the double clock without delay. Bit 0 is defined by Frame synchronization Signal.
1	0	1	Each bit is transmitted with 1/2 bit-time delay.
1	1	0	Each bit is transmitted with 1 bit-time delay.
1	1	1	Each bit is transmitted with 2 bit-time delay.
0	0	1	Each bit is transmitted with 1/2 bit-time advance.
0	1	0	Each bit is transmitted with 1 bit-time advance
0	1	1	Each bit is transmitted with 2 bit-time advance.

When IMTD = 0 (bit of SMCR), DEL = 0 is not taken into account by the circuit.
1/2 bit time 244ns if TDM at 2048 kHz,
1/2 bit time 122ns if TDM at 4096 kHz.

OMV (i) : Output Multiplex Validated 0/7
OMVi =1, condition to have DOUTi pin active ($0 \le i \le 7$).
OMVi =0, DOUTi pin is High Impedance continuously ($0 \le i \le 7$).

N.B. If DIN4 and DIN5 are GCI Multiplexes : then ST(4)1 = ST(4)0 = 0 and ST(5)1 = ST(5)0 = 0 normally.

VIII.7 - Switching Matrix Configuration Register - SMCR (0C)H

bit15							bit8	bit7							bit 0
SW1	SW0	M1	M0	DR64	DR44	DR24	DR04	AISD	ME	SGC	SAV	SGV	TS1	TS0	IMTD
After reset $(0000)_H$															

IMTD : Increased Minimum Throughput Delay
When SI = 0 (bit of CMDR, variable delay mode) :
IMTD = 1, the minimum delay through the matrix memory is three time slots whatever the selected TDM output.
IMTD = 0, the minimum delay through the matrix memory is two time slots whatever the selected TDM output.
When IMTD = 0, the input TDMs cannot be delayed versus the frame synchronization (Use of IMCR is limited) and the output TDMs cannot be advanced versus the frame synchronization.(Use of OMCR is limited).

VIII - INTERNAL REGISTERS (continued)

TS0 : Tristate 0
TS0 = 1, the DOUT0/3 and DOUT6/7 pins are tristate : ”0” is at low impedance, ”1” is at low impedance and the third state is high impedance.
TS0 = 0, the DOUT0/3 and DOUT6/7 pins are open drain : ”0” is at low impedance, ”1” is at high impedance.

TS1 : Tristate 1
TS1 = 1, the DOUT4/5 pins are tristate : ”0” is at low impedance, ”1” is at low impedance and the third state is high impedance.
TS1 = 0, the DOUT4/5 pins are open drain : ”0” is at low impedance, ”1” is at high impedance.

SGV : Pseudo Random Sequence Generator Validated
SGV = 1,PRS Generator is validated.The Pseudo Random Sequence is transmitted during the related time slot(s).
SGV = 0, PRS Generator is reset.”0” are transmitted during the related time slot.

SAV : Pseudo Random Sequence analyzer Validated
SAV = 1, PRS analyzer is validated.
SAV = 0, PRS analyzer is reset.

SGC : Pseudo Random Sequence Generator Corrupted
When SGC bit goes from 0 to 1, one bit of sequence transmitted is corrupted.
When the corrupted bit has been transmitted, SGC bit goes from 1 to 0 automatically.

ME : MESSAGE ENABLE
ME = 1 The contents of Connection Memory is output on DOUT0/7 continuously.
ME = 0 The contents of Connection Memory acts as an address for the Data Memory.

AISD : Alarm Indication Signal Detection.
AISD = 1, the Alarm Indication Signal detection is validated.
Sixteen independent detections are performed for sixteen hyperchannels. The contents of any input hyperchannel (B1, B2, D) switched (in transparent mode or not) on GCI channels is analysed independently.
For each GCI channel, the 16bits of B1 and B2 are checked together; when all “one” has been detected during 30 milliseconds, a status is stored in the Command/ Indicate interrupt queue and an interrupt is generated if not masked (like the reception of primitive from GCI multiplexes).
See “RECEIVE Command/Indicate INTERRUPT” on page 97.
AISD=0, the Alarm Indication Signal detection for 16 hyperchannels is not validated.

DR04 : Data Rate of TDM0 is at 4Mb/s. Case:M1=M0=0
DR04 = 1, the signal received from DIN0 pin and the signal delivered by Dout0 pin are at 4Mb/s. DIN1 pin and DOUT1 pin are ignored.
The Time Division Multiplex 0 is constituted by 64 timeslots numbered from 0 to 63.
DR04 = 0, the signals received from DIN0/1 pins and the signals delivered by Dout0/1 pins are at 2Mb/s.

DR24 : Data Rate of TDM2 is at 4Mb/s.Case:M1=M0=0
R24 = 1, the signal received from DIN2 pin and the signal delivered by Dout2 pin are at 4Mb/s. DIN3 pin and DOUT3 pin are ignored.
The Time Division Multiplex 2 is constituted by 64 timeslots numbered from 0 to 63.
DR24 = 0, the signals received from DIN2/3 pins and the signals delivered by Dout2/3 pins are at 2Mb/s.

DR44 : Data Rate of TDM4 is at 4Mb/s.Case: M1=M0=0
DR44 = 1, the signal received from DIN4 pin and the signal delivered by Dout4 pin are at 4Mb/s. DIN5 pin and DOUT5 pin are ignored.
TDM4/5 cannot be GCI multiplexes.
The Time Division Multiplex 4 is constituted by 64 timeslots numbered from 0 to 63.
DR44 = 0, the signals received from DIN4/5 pins and the signals delivered by Dout4/5 pins are at 2Mb/s.

VIII - INTERNAL REGISTERS (continued)

DR64 : Data Rate of TDM6 is at 4Mb/s.Case:M1=M0=0
DR64 = 1, the signal received from DIN6 pin and the signal delivered by Dout6 pin are at 4Mb/s. DIN7 pin and DOUT7 pin are ignored.
The Switching Matrix cannot be used to switch the channels to/from the HDLC controllers but the RX HDLC controller can be connected to DIN8 and the TX HDLC controller can be connected to CB pin.
The Time Division Multiplex 6 is constituted by 64 timeslots numbered from 0 to 63.
DR64 = 0, the signals received from DIN6/7 pins and the signals delivered by Dout6/7 pins are at 2M b/s.

M1/0 : Data Rate of TDM0/8;
these two bits indicate the data rate of height Time Division Multiplexes TDM0/7 relative to DIN0/7 and DOUT0/7. The table below shows the different data rates with the clock frequency defined by HCL bit (General Configuration Register).

M1	M0	Data Rate of TDM0/7 in Kbit/s	CLOCKA/B signal frequency	
			HCL = 0	HCL = 1
0	0	2048 (or 4096 in accordance with DR0x4)	4096KHz	8192KHz
0	1	1536 (or 3072 in accordance with DR0x4)	3072KHz	6144KHz
1	0	Reserved		
1	1	Reserved		

SW : Switching at 32 Kbit/s for the TDM0 (DIN0/DOUT0)
SW0=1
DIN0 can receive 64 channels at 32 Kbit/s if Data Rate of TDM0 is at 2048 Kbit/s.
DOUT0 can deliver 64 channels at 32 Kbit/s.
DIN2/DOUT2 are not available.
DIN2 is used to receive internally TDM0 (DIN0) 4 bit-times shifted
DOUT2 is used to multiplex internally TDM2 and TDM4. Downstream switching at 32 kb/s on page 22.

SW1 : SW1: Switching at 32 Kbit/s for the TDM1 (DIN1/DOUT1)
SW1=1
DIN1 can receive 64 channels at 32 Kbit/s if Data Rate of TDM1is at 2048 Kbit/s.DOUT0 can deliver 64 channels at 32 Kbit/s.
DIN3/DOUT3 are not available.
DIN3 is used to receive internally TDM1(DIN1) and to shift it (4 bit-times)DOUT3 is used to multiplex internally TDM3 and TDM5. Downstream switching at 32 kb/s on page 22.
SW1=0
DIN0 receive 32 (or 24) channels at 64 Kbit/s or 64 (or 48) channels at 64 Kbit/s depending on DR04 bit.

VIII - INTERNAL REGISTERS (continued)

VIII.8 - Connection Memory Data Register - CMDR (0E)H

CONTROL REGISTER (CTLR)								SOURCE REGISTER (SRCR)							
bit15							bit8	bit7							bit 0
SCR	PS	PRSA	S1	S0	OTSV	LOOP	SI	IM2	IM1	IM0	ITS 4	ITS 3	ITS 2	ITS 1	ITS 0
After reset $(0000)_H$															

This 16 bit register is constituted by two registers :
SOURCE REGISTER (SRCR) and CONTROL REGISTER (CTLR)

SOURCE REGISTER (SRCR) has two use modes depending on CM (bit of CMAR).

CM = 1, access to connection memory (read or write)

- PRSG = 0, ITS 0/4 and IM0/2 bits are defined hereafter :
  ITS 0/4 : Input time slot 0/4 define ITSx with : $0 \leq x \leq 31$;
  IM0/2 : Input Time Division Multiplex 0/2 define ITDMp with : $0 \leq p \leq 7$.
- PRSG = 1, the Pseudo Random Sequence Generator is validated, SRCR is not significant.

CM = 0, access to data memory (read only). SRC is the data register of the data memory.

CONTROL REGISTER (CTLR) defines each Output Time Slot OTSy of each Output Time Division Multiplex OTDMq :

SI : SEQUENCE INTEGRITY
SI = 1, the delay is always : (31 - ITSx) + 32 + OTSy.
SI = 0, the delay is minimum to pass through the data memory.

LOOP : LOOPBACK per channel relevant if a bidirectional connection has been established.
LOOP = 1, OTSy, OTDMq is taken into account instead of ITSy, ITDMq.
OTSV = 1, transparent Mode LOOPBACK.
OTSV = 0, not Transparent Mode LOOPBACK.

OTSV : OUTPUT TIME SLOT VALIDATED
OTSV = 1, OTSy OTDMq is enabled.
OTSV = 0, OTSy OTDMq is High Impedance.
(OTSy : Output Time slot with $0 \leq y \leq 31$; OTDMq : Output Time Division Multiplex with $0 \leq q \leq 7$).

S1/S0 : SOURCE 1/0

S1	S0	Source for each timeslot of DOUT0/7
0	0	Data Memory (Normal case)
0	1	Connection Memory
1	0	D channels from/to GCI multiplexes (See note and table hereafter)
1	1	Pseudo Random Sequence Generator delivers Hyperchannel at n x 64Kb/s is possible.

Note:
Connection

When the source of D channels is selected (GCI channels defined by ITS 1/0) and when the destination is selected (Output timeslot defined by OTS 0/4; output TDM defined by OM 0/2) the upstream connection is set up; the downstream connection (reverse direction TDM to GCI) is set up automatically if ITS 2 bit is at 1. So BID, bit of CMAR must be written at"0".

Release

Remember: write S1=1, S0=0 and ITS 2 bit = 0 to release the downstream connection; the upstream connection is released when the source changes.

VIII - INTERNAL REGISTERS (continued)

TABLE: SWITCHING AT 16Kb/s WHEN ITS3 = 0

S1	S0	ITS 3	ITS 2	ITS 1	ITS 0	Upstream Source: D channels of one of 16 GCI channels Destination: two bits of one TDM	Downstream Source: two bits of one TDM Destination: D channels of one of 16 GCI channels
1	0	0	1	0	0	The contents of D channels of GCI 0 /3 of multiplex DIN4 are transferred into the output timeslot of one TDM defined by the destination register (CMAR). D channel of GCI 0 in bit 1/2 D channel of GCI 1 in bit 3/4 D channel of GCI 2 in bit 5/6 D channel of GCI 3 in bit 7/8	The contents of the input timeslot (same number as the number of the output timeslot) is transferred in D channel of GCI 0/3 of multiplex DOUT4 bit 1/2 in D channel of GCI 0 bit 3/4 in D channel of GCI 1 bit 5/6 in D channel of GCI 2 bit 7/8 in D channel of GCI 3
				0	1	The contents of D channels of GCI 4/7 of multiplex DIN4 are transferred into the output timeslot of one TDM defined by the destination register (CMAR). D channel of GCI 4 in bit 1/2 D channel of GCI 5 in bit 3/4 D channel of GCI 6 in bit 5/6 D channel of GCI 7 in bit 7/8	The contents of the input timeslot (same number as the number of the output timeslot) is transferred in D channel of GCI 4/7 of multiplex DOUT4. bit 1/2 in D channel of GCI 4 bit 3/4 in D channel of GCI 5 bit 5/6 in D channel of GCI 6 bit 7/8 in D channel of GCI 7
				1	0	The contents of D channels of GCI 0 /3 of multiplex DIN5 are transferred into the output timeslot of one TDM defined by the destination register (CMAR). D channel of GCI 0 in bit 1/2 D channel of GCI 1 in bit 3/4 D channel of GCI 2 in bit 5/6 D channel of GCI 3 in bit 7/8	The contents of the input timeslot (same number as the number of the output timeslot) is transferred in D channel of GCI 0/3 of multiplex DOUT5. bit 1/2 in D channel of GCI 0 bit 3/4 in D channel of GCI 1 bit 5/6 in D channel of GCI 2 bit 7/8 in D channel of GCI 3
				1	1	The contents of D channels of GCI 4/7 of multiplex DIN5 are transferred into the output timeslot of one TDM defined by the destination register (CMAR). D channel of GCI 4 in bit 1/2 D channel of GCI 5 in bit 3/4 D channel of GCI 6 in bit 5/6 D channel of GCI 7 in bit 7/8	The contents of the input timeslot (same number as the number of the output timeslot) is transferred in D channel of GCI 4/7 of multiplex DOUT5. bit 1/2 in D channel of GCI 4 bit 3/4 in D channel of GCI 5 bit 5/6 in D channel of GCI6 bit 7/8 in D channel of GCI 7

VIII - INTERNAL REGISTERS (continued)

TABLE: SWITCHING AT 16KB/S when ITS3 =1

S1	S0	ITS 3	ITS 2	ITS 1	ITS 0	Upstream Source: D channels of one of 16 GCI channels Destination: two bits of one TDM	Downstream Source: two bits of one TDM Destination: D channels of one of 16 GCI channels
1	0	1	1	0	0	The contents of D channels of GCI 0 /3 of multiplex DIN4 are transferred into the output timeslot of one TDM defined by the destination register (CMAR). D channel of GCI 0 in bit 7/8 D channel of GCI 1 in bit 5/6 D channel of GCI 2 in bit 3/4 D channel of GCI 3 in bit 1/2	The contents of the input timeslot (same number as the number of the output timeslot) is transferred in D channel of GCI 0/3 of multiplex DOUT4 bit 7/8 in D channel of GCI 0 bit 5/6 in D channel of GCI 1 bit 3/4 in D channel of GCI 2 bit 1/2 in D channel of GCI 3
				0	1	The contents of D channels of GCI 4/7 of multiplex DIN4 are transferred into the output timeslot of one TDM defined by the destination register (CMAR). D channel of GCI 4 in bit 7/8 D channel of GCI 5 in bit 5/6 D channel of GCI 6 in bit 3/4 D channel of GCI 7 in bit 1/2	The contents of the input timeslot (same number as the number of the output timeslot) is transferred in D channel of GCI 4/7 of multiplex DOUT4. bit 7/8 in D channel of GCI 4 bit 5/6 in D channel of GCI 5 bit 3/4 in D channel of GCI 6 bit 1/2 in D channel of GCI 7
				1	0	The contents of D channels of GCI 0 /3 of multiplex DIN5 are transferred into the output timeslot of one TDM defined by the destination register (CMAR). D channel of GCI 0 in bit 7/8 D channel of GCI 1 in bit 5/6 D channel of GCI 2 in bit 3/4 D channel of GCI 3 in bit 1/2	The contents of the input timeslot (same number as the number of the output timeslot) is transferred in D channel of GCI 0/3 of multiplex DOUT5. bit 7/8 in D channel of GCI 0 bit 5/6 in D channel of GCI 1 bit 3/4 in D channel of GCI 2 bit 1/2 in D channel of GCI 3
				1	1	The contents of D channels of GCI 4/7 of multiplex DIN5 are transferred into the output timeslot of one TDM defined by the destination register (CMAR). D channel of GCI 4 in bit 7/8 D channel of GCI 5 in bit 5/6 D channel of GCI 6 in bit 3/4 D channel of GCI 7 in bit 1/2	The contents of the input timeslot (same number as the number of the output timeslot) is transferred in D channel of GCI 4/7 of multiplex DOUT5. bit 7/8 in D channel of GCI 4 bit 5/6 in D channel of GCI 5 bit 3/4 in D channel of GCI 6 bit 1/2 in D channel of GCI 7

PRSA : Pseudo Random Sequence analyzer
If PRSA = 1, PRS analyzer is enabled during OTSy OTDMq and receives data :
INS = 0, data comes from Data Memory.
INS = 1 AND PRSG=1, Data comes from PRS Generator (Test Mode).
If PRSA = 0, PRS analyzer is disabled during OTSy OTDMq.

PS : Programmable Synchronization
If PS = 1, Programmable Synchronization Signal Pin is at "1" during the bit time defined by OTSy and OTDMq.
For OTSy and OTDMq with y = q = 0, PSS pin is at "1" during the first bit of the frame defined by the Frame synchronization Signal (FS).
If PS = 0, PSS Pin is at "0" during the bit time defined by OTSy and OTDMq.

SCR : Scrambler/ Descrambler
SCR=1, the scrambler or the descrambler are enabled. Both of them are located after the switching matrix.

VIII - INTERNAL REGISTERS (continued)

SCR (cont'd) : The scrambler is enabled when the output timeslot defined by the destination register (DSTR) is an output timeslot belonging to any TDM except the two GCI multiplexes; the contents of this output timeslot will be scrambled in accordance with the IUT-T V.29 Rec.
The descrambler is enabled when the output timeslot defined by the destination register (DSTR) is an output timeslot belonging to the two GCI multiplexes except any TDM; the contents of this output timeslot is descrambled in accordance with the IUT-T V.29 Rec.
Only 32 timeslots of 256 can be scrambled or/and descrambled:
GCI side, only B1 and B2 can be selected in each GCI channel (16 GCI channels are available: 8 per GCI multiplex).
*TDM side, it is forbidden to select a given timeslot more than once when several TDMs are selected.
SCR=0, the scrambler or the descrambler are disabled; the contents of output timeslots are not modified.

VIII.9 - Connection Memory Address Register - CMAR (10)H

ACCESS MODE REGISTER (AMR)								DESTINATION REGISTER (DSTR)							
bit15							bit8	bit7							bit 0
Nu	Nu	TC	CACL	CAC	BID	CM	READ	OM2	OM1	OM0	OTS4	OTS3	OTS2	OTS1	OTS0
After reset $(0800)_H$															

This 16 bit register is constituted by two registers : DESTINATION REGISTER (DSTR) and ACCESS MODE REGISTER (AMR) respectively 8 bits and 6 bits.

DESTINATION REGISTER (DSTR)

When DSTR Register is written by the microprocessor, a memory access is launched. DSTR has two use modes depending on CM (bit of CMAR).

CM = 1, access to connection memory (read or write) ;

OTS 0/4 : Output time slot 0/4 define OTSy with : $0 \leq y \leq 31$,

OM0/2 : Output Time Division Multiplex 0/2 define OTDMq with : $0 \leq q \leq 7$.

See table hereafter when DR04, DR24, DR44 and/or DR64 are at "1"; the bits of SMCR define the TDMs at 4 Mbit/s.

The IM2/1 bits of Source Register (SRCR of CMDR) indicate the DIN pin number and the OM2/1 bits of Destination Register (DSTR of CMAR) indicate the Dout pin number.

IM2 (bit7)	IM1 (bit6)	DIN pin	OM2 (bit7)	OM1(bit6)	DOUT pin
0	0	DIN0	0	0	DOUT0
0	1	DIN2	0	1	DOUT2
1	0	DIN4	1	0	DOUT4
1	1	DIN6	1	1	DOUT6

The ITS4/0 and IM0 bits of Source Register (SRCR of CMDR) indicate the input timeslot number. (IM0 bit is the Least Significant Bit; it indicates either even timeslot or odd timeslot.

ITS4 (bit4)	ITS3 (bit3)	ITS2 (bit2)	ITS1 (bit1)	ITS0 (bit0)	IMO (bit5)	Input timeslot number
0	0	0	0	0	0	0
0	0	0	0	0	1	1
0	0	0	0	1	0	2
0	0	0	0	1	1	3
=						=
1	1	1	1	1	1	63

VIII - INTERNAL REGISTERS (continued)

The OTS4/0 and OM0 bits of Destination Register (DSTR of CMAR) indicate the output timeslot number. (OM0 bit is the Least Significant Bit; it indicates either even timeslot or odd timeslot

OTS4 (bit4)	OTS3 (bit3)	OTS2 (bit2)	OTS1 (bit1)	OTS0 (bit0)	OMO (bit5)	Output timeslot number
0	0	0	0	0	0	0
0	0	0	0	0	1	1
0	0	0	0	1	0	2
0	0	0	0	1	1	3
=						=
1	1	1	1	1	1	63

Nota Bene:
- CLOCK A/B is at 4 or at 8 MHz in accordance with HCL bit of General Configuration Register GCR (02).
  HCL=1, bit clock frequency is at 8 192 KHz.
  For a TDM at 4 Mbit/s or 2Mbit/s, each received bit is sampled at 3/4 bit-time.
  HCL=0, bit clock frequency is at 4 096 KHz
  For a TDM at 4 Mbit/s, each received bit is sampled at half bit-time.
  For a TDM at 2 Mbit/s, each received bit is sampled at 3/4 bit-time.

The definition of IMCRO/1, OMCRO/1 are kept with bit time = 244 ns

Remarks:
- OM0, bit5 of DSTR indicates either even TDM or odd TDM if TDM at 2 Mb/s.
- OM0, bit5 of DSTR indicates either even Output timeslot or odd Output timeslot if TDM at 4 Mb/s.
- IM0, bit5 of SRCR indicates either even TDM or odd TDM if TDM at 2 Mb/s.
- IM0, bit5 of SRCR indicates either even Output timeslot or odd Output timeslot if TDM at 4 Mb/s.
- CAC = CACL = 0, DSTR is the Address Register of the Connection Memory;
- CAC or CACL = 1, DSTR is used to indicate the current address for the Connection Memory ; its contents is assigned to the outputs.

CM = 0, access to data memory (read only) ;
- DSTR is the Address Register of the Data Memory; its contents is assigned to the inputs.

ACCESS MODE REGISTER (AMR)

READ : READ MEMORY
READ = 1, Read Connection Memory (or Data Memory in accordance with CM).
READ = 0, Write Connection Memory.

CM : CONNECTION MEMORY
CM = 1, Write or Read Connection Memory in accordance with READ.
CM = 0, Read only Data Memory (READ = 0 has no effect).

BID : BIDIRECTIONAL CONNECTION
BID = 1; Two connections are set up:
ITSx ITDMp -----> OTSy OTDMq (LOOP of CMDR Register is taken into account) and
ITSy ITDMq -----> OTSx OTDMp (LOOP of CMDR Register is not taken into account).
BID = 0; One connection is set up:
ITSx ITDMp -----> OTSy OTDMq only.

CAC : CYCLICAL ACCESS
CAC = 1 (BID is ignored)
if Write Connection Memory, an automatic data write from Connection Memory Data Register (CMDR) up to 256 locations of Connection Memory occurs. The first address is indicated by the register DSTR, the last is (FF)H.
if Read Connection Memory, an automatic transfer of data from the location indicated by the register (DSTR) into Connection Memory Data Register (CMDR) after reading by the microprocessor occurs. The last location is (FF)H.
CAC = 0, Write and Read Connection Memory in the normal way.

VIII - INTERNAL REGISTERS (continued)

CACL : CYCLICAL ACCESS LIMITED
CACL = 1 (BID is ignored)
If Write Connection Memory, an automatic data write from Connection Memory Data Register (CMDR) up to 32 locations of Connection Memory occurs. The first location is indicated by OTS 0/4bits of the register (DSTR) related to OTDMq as defined by OM0/2 occurs. The last location is q +1 F(H).
If Read Connection Memory, an automatic transfer of data from Connection Memory into Connection Memory Data Register (CMDR) after reading this last by the microprocessor occurs.The first location is indicated by OTS 0/4 bits of the register (DSTR) related to OTDMq as defined by OM0/2. The last location is q +1 F(H).
CACL = 0, Write and Read Connection Memory in the normal way.

TC : Transparent Connection
TC = 1, (BID is ignored), if READ = 0 :
CAC = 0 and CACL = 0. The DSTR bits are taken into account instead of SRCR bits. SRCR bits are ignored (Destination and Source are identical). The contents of Input time slot i - Input multiplex j is switched into Output time slot i - Output multiplex j.
CAC = 0 and CACL = 1. Up to 32 "Transparent Connections" are set up.
CAC = 1 and CACL = 0. Up to 256 "Transparent Connections" are set up.
TC = 0, Write and Read Connection Memory are in accordance with BID.

VIII.10 - Sequence Fault Counter Register - SFCR (12)H

bit15							bit8	bit7							bit 0
F15	F14	F13	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	F0
After reset $(0000)_H$															

When this register is read by the microprocessor, this register is reset $(0000)_H$.

F0/15 : FAULT0/15
Number of faults detected by the Pseudo Random Sequence analyzer if the analyzer has been validated and has recovered the receive sequence.
When the Fault Counter Register reaches $(00FF)_H$ it stays at its maximum value.

NB. As the SFCR is reset after reading, a 8-bit microprocessor must read the LSB that will represent the number of faults between 0 and 255. To avoid overflow escape notice, it is necessary to start counting at FF00h, by writing this value in SFCR before launching PRSA. If there are more than FFh errors, the SFCO interrupt bit (see interrupt register IR -38H address) will signal that the fault count register has reached the value FFFFh (because of the number of faults exceeded 255).

VIII.11 - Time Slot Assigner Address Register - TAAR (14)H

bit15							bit8	bit7							bit 0
TS4	TS3	TS2	TS1	TS0	READ	Nu	HDI	r	e	s	e	r	v	e	d
After reset $(0100)_H$															

READ : READ MEMORY
READ = 1, Read Time slot Assigner Memory.
READ = 0, Write Time slot Assigner Memory.

TS0/4 : TIME SLOTS0/4
These five bits define one of 32 time slots in which a channel is set-up or not.

VIII - INTERNAL REGISTERS (continued)

HDI : HDLC INIT
HDI = 1, TSA Memory, Tx HDLC, Tx DMA, Rx HDLC, Rx DMA and GCI controllers are reset within 250ms. An automate writes data from Time slot Assigner Data Register (TADR) (except CH0/4 bits) into each TSA Memory location. If the microprocessor reads Time slot Assigner Memory after HDLC INIT, CH0/4 bits of Time slot Assigner Data Register are identical to TS0/4 bits of Time slot Assigner Address Register.
HDI = 0, Normal state.

N.B. After software reset (bit 2 of IDCR Register) or pin reset the automate above-mentioned is working. The automate is stopped when the microprocessor writes TAAR Register with HDI = 0.

VIII.12 - Time Slot Assigner Data Register - TADR (16)H

bit15							bit8	bit7							bit 0
V11	V10	V9	V8	V7	V6	V5	V4	V3	V2	V1	CH4	CH3	CH2	CH1	CH0
After reset $(0000)_H$															

CH0/4 : CHANNEL0/4
These five bits define one of 32 channels associated to TIME SLOT defined by the previous Register (TAAR).

V1/8 : VALIDATION
The logical channel CHx is constituted by each subchannel 1 to 8 and validated by V1/8 bit at 1 respectively.
V1 to V8 at 0: the subchannels are ignored
V1 at 1: the first bit of the current time slot is taken into account in reception the first bit received and in transmission the first bit transmitted.
V8 at 1: the last bit of the current time slot is taken into account in reception the last bit received and in transmission the last bit transmitted in transmission.

V9 : VALIDATION SUBCHANNEL
V 9 = 1, each V1/8 bit is taken into account once every 250ms.
In transmit direction, data is transmitted consecutively during the time slot of the current frame and during the same time slot of the next frame.Id est.: the same data is transmitted in two consecutive frames.
In receive direction, HDLC controller fetches data during the time slot of the current frame and ignores data during the same time slot of the next frame.
V 9 = 0, each V1/8 bit is taken into account once every 125ms.

V10 : DIRECT MHDLC ACCESS
If V10 = 1, the Rx HDLC Controller receives data issued from DIN8 input during the current time slot (bits validated by V1/8) and DOUT6 output transmits data issued from the Tx HDLC Controller.
If V10 = 0, the Rx HDLC Controller receives data issued from the matrix output 7 during the current time slot ; DOUT6 output delivers data issued from the matrix output 6 during the same current time slot.
N.B : If D7 = 1, (see "General Configuration Register GCR (02)H") the Tx HDLC controller is connected to matrix input 7 continuously so the HDLC frames can be sent to any DOUT (i.e. DOUT0 to DOUT7).

V11 : VALIDATION of CB pin
This bit is not taken into account if CSMA = 1 (HDLC Transmit Command Register).
if CSMA = 0 :
V11 = 1, Contention Bus pin is validated and Echo pin (which is an input) is not taken into account.
V11 = 0, Contention Bus pin is high impedance during the current time slot (This pin is an open drain output).

VIII - INTERNAL REGISTERS (continued)

VIII.13 - HDLC Transmit Command Register - HTCR (18)H

bit15							bit8	bit7							bit 0
CH4	CH3	CH2	CH1	CH0	READ	Nu	CF	PEN	CSMA	NCRC	F	P1	P0	C1	C0
After reset $(0000)_H$															

READ : READ COMMAND MEMORY
READ = 1, READ COMMAND MEMORY.
READ = 0, WRITE COMMAND MEMORY.

CH0/4 : These five bits define one of 32 channels.

C1/C0 : COMMAND BITS

C1	C0	Commands Bits
0	0	ABORT ; if this command occurs during the current frame, HDLC Controller transmits seven "1" immediately, afterwards HDLC Controller transmits "1" or flag in accordance with F bit, generates an interrupt and waits new command such as START orn CONTINUE. If this command occurs after transmitting a frame, HDLC Controller generates an interrupt and waits a new command such as START or CONTINUE.
0	1	START ; Tx DMA Controller is now going to transfer first frame from buffer related to initial descriptor. The initial descriptor address is provided by the Initiate Block located in external memory.
1	0	CONTINUE ; Tx DMA Controller is now going to transfer next frame from buffer related to next descriptor. The next descriptor address is provided by the previous descriptor from which the related frame had been already transmitted.
1	1	HALT ; after transmitting frame, HDLC Controller transmits "1" or flag in accordance with F bit, generates an interrupt and is waiting new command such as START or CONTINUE.

P0/1 : PROTOCOL BITS

P1	P0	Transmission Mode
0	0	HDLC
0	1	Transparent Mode 1 (per byte) ; the fill character defined in FCR Register is taken into account.
1	0	Transparent Mode 2 (per byte) ; the fill character defined in FCR Register is not taken into account.
1	1	Reserved

F : Flag
F = 1 ; flags are transmitted between closing flag of current frame and opening flag of next frame.
F = 0 ; "1" are transmitted between closing flag of current frame and opening flag of next frame.

NCRC : CRC NOT TRANSMITTED
NCRC = 1, the CRC is not transmitted at the end of the frame.
NCR C =0, the CRC is transmitted at the end of the frame.

CSMA : Carrier Sense Multiple Access with Contention Resolution
CSMA = 1, CB output and the Echo Bit are taken into account during this channel transmission by the Tx HDLC.
CSMA = 0, CB output and the Echo Bit are defined by V11 (see " Time slot Assigner Data Register TADR (16)H").

VIII - INTERNAL REGISTERS (continued)

PEN : CSMA PENALTY significant if CSMA = 1
PEN = 1, the penalty value is 1 ; a transmitter which has transmitted a frame correctly will count (PRI +1) logic one received from Echo pin before transmitting next frame. (PRI, priority class 8 or 10 given by the buffer descriptor related to the frame.
PEN = 0, the penalty value is 2 ; a transmitter which has transmitted a frame correctly will count (PRI +2) logic one received from Echo pin before transmitting next frame. (PRI, priority class 8 or 10 given by the transmit descriptor related to the frame).

CF : Common flag
CF = 1, the closing flag of previous frame and opening flag of next frame are identical if the next frame is ready to be transmitted.
CF = 0, the closing flag of previous frame and opening flag of next frame are distinct.

VIII.14 - HDLC Receive Command Register - HRCR (1A)H

bit15							bit8	bit7							bit 0
CH4	CH3	CH2	CH1	CH0	READ	AR21	AR20	AR11	AR10	CRC	FM	P1	P0	C1	C0
After reset $(0000)_H$															

READ : READ COMMAND MEMORY
READ = 1, READ COMMAND MEMORY.
READ = 0, WRITE COMMAND MEMORY.

CH0/4 : These five bits define one of 32 channels.

C1/C0 : COMMAND

C1	C0	Commands Bits
0	0	ABORT ; if this command occurs during receiving a current frame, HDLC Controller stops the reception, generates an interrupt and waits new command such as START orn CONTINUE. If this command occurs after receiving a frame, HDLC Controller generates an interrupt and waits a new command such as START or CONTINUE.
0	1	START ; Rx DMA Controller is now going to transfer first frame into buffer related to the initial descriptor. The initial descriptor address is provided by the Initiate Block located in external memory.
1	0	CONTINUE ; Rx DMA Controller is now going to transfer next frame into buffer related to next descriptor. The next descriptor address is provided by the previous descriptor from which the related frame had been already received.
1	1	HALT ; after receiving frame, HDLC Controller stops the reception, generates an interrupt and waits a new command such as START or CONTINUE.

P0/1 : PROTOCOL BITS

P1	P0	Transmission Mode
0	0	HDLC
0	1	Transparent Mode 1 (per byte) ; the fill character defined in FCR Register is taken into account.
1	0	Transparent Mode 2 (per byte) ; the fill character defined in FCR Register is not taken into account.
1	1	Reserved

FM : Flag Monitoring.
This bit is a status bit read by the microprocessor.
FM=1: HDLC Controller is receiving a frame or HDLC Controller has just received one flag.
FM is put to 0 by the microprocessor.

CRC : CRC stored in external memory
CRC = 1, the CRC is stored at the end of the frame in external memory.
CRC = 0, the CRC is not stored into external memory.

VIII - INTERNAL REGISTERS (continued)

AR10 : Address Recognition10
AR10 = 1, First byte after opening flag of received frame is compared to AF0/7 bits of AFRDR. If the first byte received and AF0/7 bits are not identical the frame is ignored.
AR10 = 0, First byte after opening flag of received frame is not compared to AF0/7 bits of AFRDR Register.

AR11 : Address Recognition 11
AR11 = 1, First byte after opening flag of received frame is compared to all "1"s.If the first byte received is not all "1"s the frame is ignored.
AR11 = 0, First byte after opening flag of received frame is not compared to all "1"s.

AR20 : Address Recognition 20
AR20 = 1, Second byte after opening flag of received frame is compared to AF8/15 bits of AFRDR Register. If the second byte received and AF8/15 bits are not identical the frame is ignored.
AR20 = 0, Second byte after opening flag of received frame is not compared to AF8/15 bits of AFRDR Register.

AR21 : Address Recognition 21
AR21 = 1, Second byte after opening flag of received frame is compared to all "1"s. If the Second byte received is not all "1"s the frame is ignored.
AR21 = 0, Second byte after opening flag of received frame is not compared to all "1"s.

Second Byte		First Byte		Conditions to Receive a Frame
AR21	AR20	AR11	AR10	
0	0	0	0	Each frame is received without condition.
0	0	0	1	Only value of the first received byte must be equal to that of AF0/7 bits.
0	0	1	0	Only value of the first received byte must be equal to all "1"s.
0	0	1	1	The value of the first received byte must be equal either to that of AF0/7 or to all "1"s.
0	1	0	0	Only value of the second received byte must be equal to that of AF8/15 bits.
0	1	0	1	The value of the first received byte must be equal to that of AF0/7 bits and the value of the second received byte must be equal to that of AF8/15 bits.
0	1	1	0	The value of first received byte is must be equal to all "1"s and the value of second received byte must be equal to that of AF8/15 bits.
0	1	1	1	The value of the first received byte must be equal either to that of AF0/7 or to all "1"s and the value of the second received byte must be equal to that of AF8/15 bits.
1	0	0	0	Only the value of the second received byte must be equal to all "1"s.
1	0	0	1	The value of the first received byte must be equal to that of AF0/7 bits and the value of the second received byte must be equal to all "1"s.
1	0	1	0	The value of the first received byte must be equal to all "1"s and the value of the second received byte must be equal to "1" also.
1	0	1	1	The value of the first received byte must be equal either to that of AF0/7 or to "1" and the value of the second received byte must be equal to all "1"s.
1	1	0	0	The value of the second received byte must be equal either to that of AF8/15 or to all "1"s.
1	1	0	1	The value of the first received byte must be equal to that of AF0/7 bits and the value of the second received byte must be equal either to that of AF8/15 or to all "1"s.
1	1	1	0	The value of the first received byte must be equal to "1" and the value of the second received byte must be equal either to that of AF8/15 or to all "1"s.
1	1	1	1	The value of the first received byte must be equal either to that of AF0/7 or to "1" and the value of the second received byte must be equal either to that of AF8/15 or to all "1"s.

VIII - INTERNAL REGISTERS (continued)

VIII.15 - Address Field Recognition Address Register - AFRAR (1C)H

bit15							bit8	bit7							bit 0
CH4	CH3	CH2	CH1	CHO	READ	AMM	Nu	r	e	s	e	r	v	e	d
After reset $(0000)_H$															

The write operation is lauched when AFRAR is written by the microprocessor.

AMM : Access to Mask Memory.
AMM=1, Access to Address Field Recognition Mask Memory.
AMM=0, Access to Address Field Recognition Memory.

READ : READ ADDRESS FIELD RECOGNITION MEMORY
READ=1, READ AFR MEMORY.
READ=0, WRITE AFR MEMORY.

CH0/4 : These five bits define one of 32 channels in reception

VIII.16 - Address Field Recognition Data Register - AFRDR (1E)H

bit15							bit8	bit7							bit 0
AF15/ AFM15	AF14/ AFM14	AF13/ AFM13	AF12/ AFM12	AF11/ AFM11	AF10/ AFM10	AF9/ AFM9	AF8/ AFM8	AF7/ AFM7	AF6/ AFM6	AF5/ AFM5	AF4/ AFM4	AF3/ AFM3	AF2/ AFM2	AF1/ AFM1	AF0/ AFMO
After reset $(0001)_H$															

AF0/15 : ADDRESS FIELD BITS
AF0/7 ; First byte received; AF8/15: Second byte received.
These two bytes are stored into Address Field Recognition Memory when AFRAR is written by the microprocessor.

AFM0/15: ADDRESS FIELD BIT MASK0/15 if AMM=1 (AMM bit of AFRAR)
AMF0/7. When AR10=1 (See HRCR) each bit of the first received byte is compared respectively to AFx bit if AFMx=0. In case of mismatching, the received frame is ignored. If AFMx=1, no comparison between AFx and the corresponding received bit.
AMF8/15. When AR20=1 (See HRCR) each bit of the second received byte is compared respectively to AFy bit if AFMy=0. In case of mismatching, the received frame is ignored. If AFMy=1, no comparison between AFy and the corresponding received bit.
These two bytes are stored into Address Field Recognition Mask Memory when AFRAR is written by the microprocessor (AMM=1).

VIII.17 - Fill Character Register - FCR (20)H

bit15							bit8	bit7							bit 0
r	e	s	e	r	v	e	d	FC7	FC6	FC5	FC4	FC3	FC2	FC1	FC0
After reset $(0000)_H$															

FC0/7 : FILL CHARACTER (eight bits)
In Transparent Mode M1, two messages are separated by FILL CHARACTERS and the detection of one FILL CHARACTER marks the end of a message.

VIII.18 - GCI Channels Definition Register 0 - GCIR0 (22)H

The definitions of x and y indices are the same for GCIR0, GCIR1, GCIR2, GCIR3 :
- $0 \leq x \leq 7$, 1 of 8 GCI CHANNELS belonging to the same multiplex TDM4 or TDM5
- y = 0, TDM4 is selected
- y = 1, TDM5 is selected.

VIII - INTERNAL REGISTERS (continued)

bit15							bit8	bit7							bit 0
ANA11	VCI11	V*11	VM11	ANA10	VCI10	V*10	VM10	ANA01	VCI01	V*01	VM01	ANA00	VCI00	V*00	VM00
TDM5				TDM4				TDM5				TDM4			
GCI CHANNEL 1								GCI CHANNEL 0							
After reset $(0000)_H$															

VMxy : VALIDATION of MONITOR CHANNELx, MULTIPLEX y :
When this bit is at 1, monitor channel xy is validated.
When this bit is at 0, monitor channel xy is not validated.
On line to reset (if necessary) one MON channel which had been selected previously VMxy must be put at 0 during 125ms before reselecting this channel. Deselecting one MON channel during 125ms resets this MON channel.

V*xy : VALIDATION of V Starx, MULTIPLEX y
When this bit is at 1, V Star protocol is validated if VMxy=1.
When this bit is at 0, GCI Monitor protocol is validated if VMxy=1.

VCxy : VALIDATION of Command/Indicate CHANNEL x, MULTIPLEXy
When this bit is at 1, Command/Indicate channelxy is validated.
When this bit is at 0, Command/Indicate channelxy is not validated.
It is necessary to let VCxy at ”0” during 125ms to initiate the Command/Indicate channel.

ANAxy : ANALOG APPLICATION
When this bit is at 1, Primitive has 6 bits if C/Ixy is validated.
When this bit is at 0, Primitive has 4 bits if C/Ixy is validated.

VIII.19 - GCI Channels Definition Register 1 - GCIR1 (24)H

bit15							bit8	bit7							bit 0
ANA31	VCI31	V*31	VM31	ANA30	VCI30	V*30	VM30	ANA21	VCI21	V*21	VM21	ANA20	VCI20	V*20	VM20
TDM5				TDM4				TDM5				TDM4			
GCI CHANNEL 3								GCI CHANNEL 2							
After reset $(0000)_H$															

For definition see GCI Channels Definition Register above.

VIII.20 - GCI Channels Definition Register 2 - GCIR2 (26)H

bit15							bit8	bit7							bit 0
ANA51	VCI51	V*51	VM51	ANA50	VCI50	V*50	VM30	ANA41	VCI41	V*41	VM41	ANA40	VCI40	V*40	VM40
TDM5				TDM4				TDM5				TDM4			
GCI CHANNEL 5								GCI CHANNEL 4							
After reset $(0000)_H$															

For definition see GCI Channels Definition Register above.

VIII.21 - GCI Channels Definition Register 3 - GCIR3 (28)H

bit15							bit8	bit7							bit 0
ANA71	VCI71	V*71	VM71	ANA70	VCI70	V*70	VM70	ANA61	VCI61	V*61	VM61	ANA60	VCI60	V*60	VM60
TDM5				TDM4				TDM5				TDM4			
GCI CHANNEL 7								GCI CHANNEL 6							
After reset $(0000)_H$															

For definition see GCI Channels Definition Register above.

VIII - INTERNAL REGISTERS (continued)

VIII.22 - Transmit Command / Indicate Register - TCIR (2A)H

bit15							bit8	bit7							bit 0
D	G0	CA2	CA1	CA0	READ	0	0	Nu	Nu	C6A	C5/E	C4/S1	C3/S2	C2/S3	C1/S4
After reset $(00FF)_H$															

When this register is written by the microprocessor, these different bits mean :

READ : READ C/I MEMORY
READ = 1, READ C/I MEMORY.
READ = 0, WRITE C/I MEMORY.

CA 0/2 : TRANSMIT COMMAND/INDICATE MEMORY ADDRESS
CA 0/2 : These bits define one of eight Command/Indicate Channels.

G0 : This bit defines one of two GCI MULTIPLEXy.
G0 = 0, GCI0 (DIN4/DOUT4) is selected.
G0 = 1, GCI1 (DIN5/DOUT5) is selected.

D : Destination; this bit defines the destination of bits 0 to 5.
D=0: the primitive C6 to C1 is transmitted directly into one of 16 GCI channels defined by G0 and CA 0/2.
D=1: the 6 bit word A, E, S1, S2, S3, S4 is put instead of the six bits received latest during the timeslot 4n+3 (GCI channel defined by G0 and CA 0/2) and these 6 bit word is transmitted into any selected output timeslot after switching.

bit15							bit8	bit7							bit 0
D=0	G0	CA2	CA1	CA0	READ	Nu	Nu	Nu	Nu	C6	C5	C4	C3	C2	C1
D=0	G0	CA2	CA1	CA0	READ	Nu	Nu	Nu	Nu	A	E	S1	S2	S3	S4

C6/1 : New Primitive to be transmitted to the selected GCI channel (DOUT4 or DOUT5). Case of D=0.
C6 is transmitted first if ANA=1.
C4 is transmitted first if ANA=0.

A, E, S1 to S4: New 6 bit word to be transmitted into any output timeslot. Case of D=1.
The New Primitive (or the 6 bit word) is taken into account by the transmitter after writing bits 8 to 15 (if 8bit microprocessor).

Transmit Command/Indicate Register (after reading)

bit15							bit8	bit7							bit 0
D=0	G0	CA2	CA1	CA0	READ	Nu	Nu	PT1	PT0	C6	C5	C4	C3	C2	C1
D=1	G0	CA2	CA1	CA0	READ	Nu	Nu	PT1	PT0	A	E	S1	S2	S3	S4

When this register is read by the microprocessor, these different bits mean :

READ : READ C/I MEMORY
READ = 1, READ C/I MEMORY.
READ = 0, WRITE C/I MEMORY.

CA 0/2 : TRANSMIT C/I ADDRESS
CA 0/2 : These bits define one of eight Command/Indicate Channels.

G0 : This bit defines one of two GCI multiplexes.
G0 = 0, DIN4/DOUT4 are selected.
G0 = 1, DIN5/DOUT5 are selected.

D : Destination. This bit defines the destination of bits 0 to 5
D=0: the destination is one of 16 GCI channels defined by G0 and CA 0/2.
D=1:the destination is any TDM (after switching).

C6/1 : Last Primitive transmitted. Case of D=1

VIII - INTERNAL REGISTERS (continued)

A, E, S1 to S4: 6 bit word transmitted. Case of D=1.

PT0/1 : Status bits

P1	P0	Primitive Status
0	0	Primitive (or 6 bit word) has not been transmitted yet.
0	1	Primitive (or 6 bit word) has been transmitted once.
1	0	Primitive (or 6 bit word) has been transmitted twice.
1	1	Primitive (or 6 bit word) has been transmitted three times or more.

VIII.23 - Transmit Monitor Address Register - TMAR (2C)H

bit15							bit8	bit7							bit 0
0	G0	MA2	MA1	MA0	READ	Nu	Nu	Nu	Nu	TIV	FABT	L	NOB	0	Nu
After reset $(000F)_H$															

When this register is written by the microprocessor, these different bits mean :

READ : READ MON MEMORY
READ=1, READ MON MEMORY.
READ=0, WRITE MON MEMORY.

MA 0/2 : TRANSMIT MONITOR ADDRESS
MA 0/2 :These bits define one of eight Monitor Channel if validated.

G0 : This bit defines one of two GCI multiplexes.
G0 = 0, TDM4 is selected.
G0 = 1, TDM5 is selected.

NOB : NUMBER OF BYTE to be transmitted
NOB = 1, One byte to transmit.
NOB = 0, Two bytes to transmit.

L : Last byte
L = 1, the word (or the byte) located in the Transmit Monitor Data Register (TMDR) is the last.
L = 0, the word (or the byte) located in the Transmit Monitor Data Register (TMDR) is not the last.

FABT : FABT = 1, the current message is aborted by the transmitter.

TIV : Timer interrupt is Validated
TIV = 1, Time Out alarm generates an interrupt when the timer has expired.
TIV = 0, Time Out alarm is masked.

If 8 bit microprocessor the Data (TMDR Register) is taken into account by the transmitter after writing bits 8 to 15 of this register.

Transmit Monitor Address Register (after reading)

bit15							bit8	bit7							bit 0
0	G0	MA2	MA1	MA0	READ	Nu	Nu	Nu	Nu	TO	ABT	L	NOBT	EXE	IDLE

When this register is read by the microprocessor, these different bits mean :

READ, MA0/2, G0 have same definition as already described for the write register cycle.

IDLE : When this bit is at ”1”, IDLE (all 1’s) is transmitted during the channel validation.

EXE : EXECUTED
When this status bit is at ”1”, the command written previously by the microprocessor has been executed and a new word can be stored in the Transmit Monitor Data Register (TMDR) by the microprocessor.
When this bit is at ”0”, the command written previously by the microprocessor has not yet been executed.

VIII - INTERNAL REGISTERS (continued)

NOBT : NUMBER OF BYTE which has been transmitted.
NOBT = 1, the first byte is transmitting.
NOB T = 0, the second byte is transmitting, the first byte has been transmitted.
L : Last byte ; this L bit is the L bit which has been written by the microprocessor.
ABT : ABORT
ABT=1, the remote receiver has aborted the current message.
TO : Time Out one millisecond
TO = 1, the remote receiver has not acknowledged the byte which has been transmitted one millisecond ago.

VIII.24 - Transmit Monitor Data Register - TMDR (2E)H

bit15							bit8	bit7							bit 0
M18	M17	M16	M15	M14	M13	M12	M11	M08	M07	M06	M05	M04	M03	M02	M01
After reset $(FFFF)_H$															

M08/01 : First Monitor Byte to transmit. M08 bit is transmitted first.
M18/11 : Second Monitor Byte to transmit if NOB = 0 (bit of TMAR). M18 bit is transmitted first.

VIII.25 - Transmit Monitor Interrupt Register - TMIR (30)H

bit15	TDM5						bit8	bit7	TDM4						bit 0
MI71	MI61	MI51	MI41	MI31	MI21	MI11	MI01	MI70	MI60	MI50	MI40	MI30	MI20	MI10	MI00
After reset $(0000)_H$															

When the microprocessor read this register, this register is reset (0000)H.

MIxy : Transmit Monitor Channel x Interrupt, Multiplex y with :
$0 \leq x \leq 7$, 1 of 8 GCI CHANNELS belonging to the same multiplex TDM4 or TDM5
y = 0, GCI CHANNEL belongs to the multiplex TDM4 and y = 1 to TDM5.
MIxy = 1 when :
- a word has been transmitted and pre-acknowledged by the Transmit Monitor Channel xy (In this case the Transmit Monitor Data Register (TMDR) is available to transmit a new word) or
- the message has been aborted by the remote receive Monitor Channel or
- the Timer has reached one millisecond (in accordance with TIV bit of TMAR) by IM3 bit of IMR.

When MIxy goes to "1", the Interrupt MTX bit of IR is generated. Interrupt MTX can be masked.

VIII.26 - Memory Interface Configuration Register - MICR (32)H

bit15							bit8	bit7							bit 0
P41	P40	P31	P30	P21	P20	P11	P10	Z	W	V	U	T	S	R	REF
After reset $(E4F0)_H$															

REF : MEMORY REFRESH
REF = 1, DRAM REFRESH is validated,
REF = 0, DRAM REFRESH is not validated.

R,S,T : These three bits define the external RAM circuit organization (1word=2bytes)
The cycle duration is always 15.625ms (512 periods of the clock applied on XTAL1 pin).

T	S	R		If refresh
0	0	0	128K x 8 SRAM circuit (up to 512K words)	
0	0	1	512K x 8 SRAM circuit (up to 512K words)	
0	1	0	256K x 16 DRAM circuit (up to 1M word)	512 cycles / 8ms
0	1	1	1M x 4 (or 16) bits DRAM circuit (up to 4M words)	1024 cycles / 16ms
1	0	0	4M x 4 (or 16) bits DRAM circuit (up to 8M words)	2048 cycles / 32ms
1	0	1	101 to 111 not used (this writting is forbidden)	

The cycle duration is always 15.625ms (512 periods of the clock applied on XTAL1 Pin).

VIII - INTERNAL REGISTERS (continued)

U,V,W,Z : These four bits define the different signals delivered by the MHDLC.

First Case : the external RAM circuit is DRAM (T = 1 or S = 1)

- U defines the time Tu comprised between beginning of cycle and falling edge of NRAS : U = 1, Tu = 60ns - U = 0, Tu = 30ns
- V defines the time Tv comprised between falling edge of NRAS and falling edge of NCAS : V = 1, Tv = 60ns - V = 0, Tv = 30ns
- W defines the time Tw comprised between falling edge of NCAS and rising edge of NCAS : W = 1, Tw = 60ns - W = 0, Tw = 30ns
- Z defines the time Tz comprised between rising edge of NCAS and end of cycle : Z = 1, Tz = 60ns - Z = 0, Tz = 30ns

The total cycle is Tu + Tv + Tw + Tz.

The different output signals are high impedance during 15ns before the end of each cycle.

Second Case : the external RAM circuit is SRAM (T = 0 or S = 0)

- U and V define a part of write cycle for SRAM : the time Tuv comprised between falling edge and rising edge of NCE. The total of write cycle is : 15ns+Tuv + 15ns.

V	U	Tuv
0	0	30ns
0	1	60ns
1	0	90ns
1	1	120ns

- W and Z define a part of read cycle for SRAM : the time Twz comprised between falling edge of NOE and rising edge of NOE. The total of read cycle is : Twz +30ns

Z	W	Twz
0	0	30ns
0	1	60ns
1	0	90ns
1	1	120ns

N.B. The different output signals are high impedance during 15ns before the end of each cycle. On the outside of each (DRAM or SRAM) cycle all the outputs are high impedance or not in accordance with MBL bit (see "MBL : Memory Bus Low impedance").

Memory

bit15							bit8	bit7							bit 0
P4E1	P4E0	P3E1	P3E0	P2E1	P2E0	P1E1	P1E0	Z	W	V	U	T	S	R	REF
After reset $(E4F0)_H$															

P1 E0/1 : PRIORITY 1 for entity defined by E0/1
P2 E0/1 : PRIORITY 2 for entity defined by E0/1
P3 E0/1 : PRIORITY 3 for entity defined by E0/1
P4 E0/1 : PRIORITY 4 for entity defined by E0/1

Entity definition :

E1	E0	Entity
0	0	Rx DMA Controller
0	1	Microprocessor
1	0	Tx DMA Controller
1	1	Interrupt Controller

VIII - INTERNAL REGISTERS (continued)

PRIORITY 5 is the last priority for DRAM Refresh if validated. DRAM Refresh obtains PRIORITY 0 (the first priority) automatically when the first half cycle is spent without access to memory.

After reset $(E400)_H$, the Rx DMA Controller has the PRIORITY 1
the Microprocessor has the PRIORITY 2
the Tx DMA Controller has the PRIORITY 3
the Interrupt Controller has the PRIORITY 4
the DRAM Refresh has the PRIORITY 5

VIII.27 - Initiate Block Address Register - IBAR (34)H

bit15							bit8	bit7							bit 0
A23	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8
After reset (0000)H															

A8/23 : Address bits. These 16 bits are the segment address bits of the Initiate Block (A8 to A23 for the external memory in the MHDLC address space).The offset is zero (A0 to A7 ="0").

The Initiate Block Address (IBA) is :

23															8	7							0
A23	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	0	0	0	0	0	0	0	0

The 23 more significant bits define one of 8 Megawords. (One word comprises two bytes.)
The least significant bit defines one of two bytes when the microprocessor selects one byte.

Example: MHDLC device address inside µP mapping = 100000H
Initiate Block address inside µP mapping = 110000H
IBAR value = (110000 - 100000)/256 = 100H

VIII.28 - Interrupt Queue Size Register - IQSR (36)H

bit15							bit8	bit7							bit 0
TBFS	0	0	0	0	0v	0	0d	HS2	HS1	HS0	MS2	MS1	MS0	CS1	CS0
After reset $(0000)_H$															

CS0/1 : Command/Indicate Interrupt Queue Size
These two bits define the size of Command/Indicate Interrupt Queue in external memory.
The location is IBA + 256 + HDLC Queue size + Monitor Channel Queue Size (see The Initiate Block Address (IBA)).

MS0/2 : Monitor Channel Interrupt Queue Size
These three bits define the size of Monitor Channel Interrupt Queue in external memory.
The location is IBA + 256 + HDLC Queue size.

HS0/2 : HDLC Interrupt Queue Size
These three bits define the size of HDLC status Interrupt Queue in external memory for each channel.
The location is IBA+256 (see The Initiate Block Address (IBA))

HS2	HS1	HS0	HDLC Queue Size	MS2	MS1	MS0	MON Queue Size	CS1	CS0	C/I Queue Size
0	0	0	128 words	0	0	0	128 words	0	0	64 words
0	0	1	256 words	0	0	1	256 words	0	1	128 words
0	1	0	384 words	0	1	0	384 words	1	0	192 words
0	1	1	512 words	0	1	1	512 words	1	1	256 words
1	0	0	640 words	1	0	0	640 words			
1	0	1	768 words	1	0	1	768 words			
1	1	0	896 words	1	1	0	896 words			
1	1	1	1024 words	1	1	1	1024 words			

VIII - INTERNAL REGISTERS (continued)

TBFS : Time Base running with Frame Synchronisation signal
TBFS=1, the Time Base defined by the Timer Register (see page 92) is running on the rising edge of Frame Synchronisation signal.
TBFS=0, the Time Base defined by the Timer Register is running on the rising edge of MCLK signal.

VIII.29 - Interrupt Register - IR (38)H

bit15							bit8	bit7							bit 0
Nu	Nu	SFCO	PRSR	TIM	INT FOV	INT FWAR	Tx FOV	Tx FWAR	Rx FOV	Rx FWAR	ICOV	MTX	MRX	C/IRX	HDLC
After reset $(0000)_H$															

This register is read only.

When this register is read by the microprocessor, this register is reset $(0000)_H$.
If not masked, each bit at "1" generates "1" on INT0 pin.

HDLC : HDLC INTERRUPT
HDLC = 1, Tx HDLC or Rx HDLC has generated an interrupt The status is in the HDLC queue.

C/IRX : Command/Indicate Rx Interrupt
C/IRX = 1, Rx Commande/Indicate has generated an interrupt. The status is in the HDLC queue.

MRX : Rx MONITOR CHANNEL INTERRUPT
MRX = 1, one Rx MONITOR CHANNEL has generated an interrupt.The status is in the Rx Monitor Channel queue.

MTX : Tx MONITOR CHANNEL INTERRUPT
MTX = 1, one or several Tx MONITOR CHANNELS have generated an interrupt. Transmit Monitor Interrupt Register (TMIR) indicates the Tx Monitor Channels which have generated this interrupt.

ICOV : INTERRUPT CIRCULAR OVERLOAD
ICOV = 1, One of three circular interrupt memories is completed.

RxFWAR : Rx DMA CONTROLLER FIFO WARNING
RxFWAR = 1, Rx DMA CONTROLLER has generated an interrupt, its fifo is 3/4 completed.

RxFOV : Rx DMA CONTROLLER FIFO OVERLOAD
RxFOV = 1, Rx DMA CONTROLLER has generated an interrupt, it cannot transfer data from Rx HDLC to external memory, its fifo is completed.

TxFWAR : Tx DMA CONTROLLER FIFO WARNING
TxFWAR = 1, Tx DMA CONTROLLER has generated an interrupt, its fifo is 3/4 completed.

TxFOV : Tx DMA CONTROLLER FIFO OVERLOAD
TxFOV = 1, Tx DMA CONTROLLER has generated an interrupt, it cannot transfer data from Tx HDLC to external memory, its fifo is completed.

INTFWAR : INTERRUPT CONTROLLER FIFO WARNING
INTFWAR = 1, INTERRUPT CONTROLLER has generated an interrupt, its fifo is 3/4 completed.

INTFOV : INTERRUPT CONTROLLER FIFO OVERLOAD
INTFOV = 1, INTERRUPT CONTROLLER has generated an interrupt, it cannot transfer status from DMA and GCI controllers to external memory, its internal fifo is completed.

TIM : TIMER
TIM = 1, the programmable timer has generated an interrupt.

VIII - INTERNAL REGISTERS (continued)

PRSR : Pseudo Random Sequence Recovered
PRSR = 1,the Pseudo Random Sequence transmitted by the generator has been recovered by the analyzer.

SFCO : Sequence Fault Counter Overload
SFCO = 1, the Fault Counter has reached the value $(00FF)_H$.

VIII.30 - Interrupt Mask Register - IMR (3A)H

bit15							bit8	bit7							bit 0
Nu	Nu	IM13	IM12	IM11	IM10	IM9	IM8	IM7	IM6	IM5	IM4	IM3	IM2	IM1	IM0
After reset $(FFFF)_H$															

IM13/0 : INTERRUPT MASK 0/7
When IM0 = 1, HDLC bit is masked.
When IM1 =1, C/IRX bit is masked.
When IM2 = 1, MRX bit is masked.
When IM3 = 1, MTX bit is masked.
When IM4 = 1, ICOV bit is masked
When IM5 = 1, RxFWAR bit is masked.
When IM6 = 1, RxFOV bit is masked.
When IM7 = 1, TxFWAR bit is masked.
When IM8 = 1, TxFOV bit is masked.
When IM9 = 1, INTFWAR bit is masked.
When IM10 = 1, INTFOV bit is masked.
When IM11 = 1, TIM bit is masked.
When IM12 = 1, PRSR bit is masked.
When IM13 = 1, SFCO bit is masked.

VIII.31 - Timer Register - TIMR (3C)H

bit15				bit12									bit0	bit1	bit 0
S3	S2	S1	S0	MS9	MS8	MS7	MS6	MS5	MS4	MS3	MS2	MS1	MS0	MM1	MM0
0 to 15s				0 to 999ms										0 to 3x0.25ms	
After reset $(0800)_H$ id 512ms															

This programmable register indicates the time at the end of which the Watch Dog delivers logic ”1” on the pin WDO (which is an output) but only if the microprocessor does not reset the counter assigned (with the help of WDR bit of IDCR Identification and Dynamic Command Register) during the time defined by the Timer Register.

The Timer Register and its counter can be used as a time base by the microprocessor. An interrupt (TIM) is generated at each period defined by the Timer Register if the microprocessor does not reset the counter with the help of WDR (bit of IDCR).

The Watch Dog or the Timer is incremented by the Frame Synchronisation clock (TBFS=1) or by a submultiple of MCLK signal (TBFS=0; TBFS, bit of Interrupt Queue Size Register).

When TSV=1{Time Stamping Validated (GCR)} this programmable register is not used.

VIII.32 - Test Register - TR (3E)H

bit15							bit8	bit7							bit 0

IX - EXTERNAL REGISTERS

These registers are located in shared memory. Initiate Block Address Register (IBAR) gives the Initiate Block Address (IBA) in shared memory (see Register IBAR(34)H on Page 90).

'Not used' bits (Nu) are accessible by the microprocessor but the use of these bits by software is not recommended.

IX.1 - Initialization Block in External Memory

			Descriptor Address			
Channel		**Address**	**bit15**	**bit8**	**bit7**	**bit0**
CH 0	T	IBA+00	Not used		TDA High	
		IBA+02	Transmit Descriptor Address (TDA Low)			
	R	IBA+04	Not used		RDA High	
		IBA+06	Receive Descriptor Address (RDA Low)			
CH1	T	IBA+08	Not used		TDA High	
		IBA+10	Transmit Descriptor Address (TDA Low)			
	R	IBA+12	Not used		RDA High	
		IBA+14	Receive Descriptor Address (RDA Low)			
CH 2 to CH30		IBA+16 to IBA+246				
CH 31	T	IBA+248	Not used		TDA High	
		IBA+250	Transmit Descriptor Address (TDA Low)			
	R	IBA+252	Not used		RDA High	
		IBA+254	Receive Descriptor Address (RDA Low)			

When Direct Memory Access Controller receives Start from one of 64 channels, it reads initialization block immediately to know the first address of the first descriptor for this channel.
Bit 0 of Transmit Descriptor Address (TDA Low) and bit 0 of Receive Descriptor Address (RDA Low), are at ZERO mandatory. This Least Significant Bit is not used by DMA Controller, The shared memory is always a 16 bit memory for the DMA Controller.

N.B. If several descriptors are used to transmit one frame then before transmitting frame, DMA Controller stores the address of the first Transmit Descriptor Address into this Initialization Block.

IX - EXTERNAL REGISTERS (continued)

IX.2 - Receive Descriptor

This receive descriptor is located in shared memory. The quantity of descriptors is limited by the memory size only.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RDA+00			IBC	EOQ	Size Of the Buffer (SOB)											0
RDA+02	Not used								RBA High (8 bits)							
RDA+04	Receive Buffer Address Low (16 bits)															
RDA+06	Not used								NRDA High (8 bits)							
RDA+08	Next Receive Descriptor Address Low (16 bits)															
RDA+10	FR	ABT	OVF	FCRC	Number of Bytes Received (NBR)											

The 5 first words located in shared memory to RDA+00 from RDA+08 are written by the microprocessor and read by the DMAC only. The 6th word located in shared memory in RDA+10 is written by the DMAC only during the frame reception and read by the microprocessor.

SOB : Size Of the Buffer associated to descriptor up to 2048 words (1 word = 2 bytes).
If SOB = 0, DMAC goes to next descriptor.

RBA : Receive Buffer Address. LSB of RBA Low is at Zero mandatory.

RDA : Receive Descriptor Address.

NRDA : Next Receive Descriptor Address. LSB of NRDA Low is at Zero mandatory.

NBR : Number of Bytes Received (up to 4096).

IX.2.1 - Bits written by the Microprocessor only

IBC : Interrupt if the buffer has been completed.
IBC=1, the DMAC generates an interrupt if the buffer has been completed.

EOQ : End Of Queue.
EOQ=1, the DMAC stops immediately its reception generates an interrupt (HDLC = 1 in IR) and waits a command from the HRCR (HDLC Receive Command Register).
EOQ=0, the DMAC continues.

IX.2.2 - Bits written by the Rx DMAC only

FR	ABT	OVF	FCRC	Definition
1	0	0	0	The frame has been received without error. The end of frame is in this buffer.
1	0	0	1	The frame has been received with false CRC.
0	0	0	0	If NBR is different to 0, the buffer related to this descriptor is completed.The end of frame is not in this buffer.
0	0	0	0	If NBR is equal to 0, the Rx DMAC is receiving a frame.
0	1	0	0	ABORT. The received frame has been aborted by the remote transmitter or the local microprocessor.
0	1	1	0	OVERFLOW of FIFO. The received frame has been aborted.
0	1	0	1	The received frame had not an integer of bytes.

IX.2.3 - Receive Buffer

Each receive buffer is defined by its receive descriptor.
The maximum size of the buffer is 2048 words (1 word=2 bytes)

	15 8	7 0
RBA	SECOND BYTE LOCATION	FIRST BYTE LOCATION
		THIRD BYTE LOCATION
RBA+SOB-2	LAST BYTE LOCATION AVAILABLE in the Receive Buffer	LAST - 1 BYTE LOCATION AVAILABLE in the Receive Buffer

Note: for Motorola processors, a swap may be necessary to read/write the Receive Buffer.

IX - EXTERNAL REGISTERS (continued)

IX.3 - Transmit Descriptor

This transmit descriptor is located in shared memory. The quantity of descriptors is limited by the memory size only.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDA+00	BINT	BOF	EOF	EOQ	Number of Bytes to be Transmitted (NBT)											
TDA+02	Not used						CRCC	PRI	TBA High (8 bits)							
TDA+04	Transmit Buffer Address Low (16 bits)															
TDA+06	Not used								NTDA High (8 bits)							
TDA+08	Next Transmit Descriptor Address Low (16 bits)															
TDA+10	CFT	ABT	UND													

The 5 first words located in shared memory to TDA+00 from TDA+08 are written by the microprocessor and read by the DMAC only. The 6th word located in shared memory in TDA+10 is written by the DMAC only during the frame reception and read by the microprocessor.

NBT : Number of Bytes to be transmitted (up to 4096).

TBA : Transmit Buffer Address. LSB of TBA Low is at Zero mandatory.

TDA : Transmit Descriptor Address.

NTDA : Next Transmit Descriptor Address. LSB of NTDA Low is at Zero mandatory.

IX.3.1 - Bits written by the Microprocessor only

BINT : Interrupt at the end of the frame or when the buffer is become empty.
BINT = 1,
if EOF = 1 the DMAC generates an interrupt when the frame has been transmitted ;
if EOF = 0 the DMAC generates an interrupt when the buffer is become empty.
BINT = 0, the DMAC does not generate an interrupt during the transmission of the frame.

BOF : Beginning Of Frame
BOF = 1,the transmit buffer associated to this transmit descriptor contains the beginning of frame. The DMA Controller will store automatically the current descriptor address in the Initialization Block.
BOF = 0, the DMA Controller will not store the current descriptor address in the Initialization Block.

EOF : End Of Frame
EOF = 1,the transmit buffer associated to this transmit descriptor contains the end of frame.
EOF = 0,the transmit buffer associated to this transmit descriptor does not contain the end of frame.

EOQ : End Of Queue
EOQ = 1, the DMAC stops immediately its transmission, generates an interrupt (HDLC = 1 in IR) and waits a command from the HTCR (HDLC Transmit Command Register).
EOQ = 0, the DMAC continues.

CRCC : CRC Corrupted
CRCC = 1,at the end of this frame the CRC will be corrupted by the Tx HDLC Controller.

PRI : Priority Class 8 or 10
PRI = 1, if CSMA/CR is validated for this channel, the priority class is 8.
PRI = 0, if CSMA/CR is validated for this channel the priority class is 10.
(see Register CSMA)

IX - EXTERNAL REGISTERS (continued)

IX.3.2 - Bits written by the DMAC only

CFT : Frame correctly transmitted
CFT = 1, the Frame has been correctly transmitted.
CFT = 0, the Frame has not been correctly transmitted.

ABT : Frame Transmitting Aborted
ABT = 1, the frame has been aborted by the microprocessor during the transmission.
ABT = 0, the microprocessor has not aborted the frame during the transmission.

UND : Underrun
UND = 1, the transmit FIFO has not been fed correctly during the transmission.
UND = 0, the transmit FIFO has been fed correctly during the transmission.

IX.3.3 - Transmit Buffer

Each transmit buffer is defined by its transmit descriptor.
The maximum size of the buffer is 2048 words (1 word=2 bytes)

	15 8	7 0
TBA	SECOND BYTE TO TRANSMIT	FIRST BYTE TO TRANSMIT
		THIRD BYTE TO TRANSMIT
TBA + x ; NBT is odd : x = NBT - 1 NBT is even : x = NBT - 2	LAST BYTE TO TRANSMIT if NBT is even	LAST BYTE TO TRANSMIT if NBT is odd

Note: for Motorola processors, a swap may be necessary to read/write the Receive Buffer.

IX.4 - Receive & Transmit HDLC Frame Interrupt

bit15							bit8	bit7							bit 0
NS	0	Tx	A4	A3	A2	A1	A0	0	0	0	CFT/CFR	BE/BF	HALT	EOQ	RRLF/ERF

This word is located in the HDLC interrupt queue ; IQSR Register indicates the size of this HDLC interrupt queue located in the external memory.

NS : New Status.
Before writing the features of event in the external memory the Interrupt Controller reads the NS bit :
if NS = 0, the Interrupt Controller puts this bit at '1' when it writes the status word of the frame which has been transmitted or received.
if NS = 1, the Interrupt Controller puts ICOV bit at '1' to generate an interrupt (IR Register).
When the microprocessor has read the status word, it puts this bit at '0' to acknowledge the new status. This location becomes free for the Interrupt Controller.

Transmitter

Tx : Tx = 1, Transmitter

A4/0 : Tx HDLC Channel 0 to 31

RRLF : Ready to Repeat Last Frame
In consequence of event such as Abort Command HDLC, Controller is waiting Start or Continue.

EOQ : End of Queue
The Transmit DMA Controller (or the Receive DMA Controller) has encountered the current Descriptor with EOQ at "1". DMA Controller is waiting "Continue" from microprocessor.

HALT : The Transmit DMA Controller has received HALT from the microprocessor; it is waiting "Continue" from microprocessor.

BE : Buffer Empty
If BINT bit of Transmit Descriptor is at '1', the Transmit DMA Controller puts BE at "1" when the buffer has been emptied.

CFT : Correctly Frame Transmitted
A frame has been transmitted. This status is provided only if BINT bit of Transmit Descriptor is at '1'. CFT is located in the last descriptor if several descriptors are used to define a frame.

IX - EXTERNAL REGISTERS (continued)

Receiver

Tx : Tx = 0, Receiver

A4/0 : Rx HDLC Channel 0 to 31

ERF : Error detected on Received Frame
An error such as CRC not correct, Abort, Overflow has been detected.

EOQ : End of Queue
The receive DMA Controller has encountered the current receive Descriptor with EOQ at "1". DMA Controller is waiting "Continue" from microprocessor.

HALT : The Receive DMA Controller has received HALT or ABORT (on the outside of frame) from the microprocessor; it is waiting "Continue" from the microprocessor.

BE : Buffer Filled
If IBC bit of Receiver Descriptor is at '1', the Receive DMA Controller puts BF at"1" when it has filled the current buffer with data from the received frame.

CFR : Correctly Frame Received
A receive frame is ended with a correct CRC. The end of the frame is located in the last descriptor if several Descriptors.

IX.5 - Receive Command / Indicate Interrupt

IX.5.1 - Receive Command / Indicate Interrupt when TSV = 0

Time Stamping not validated (bit of GCR Register)

bit15							bit8	bit7							bit 0
NS	Nu	S1	S0	G0	A2	A1	A0	Nu	Nu	C6/A	C5/E	C4/S1	C3/S2	C2/S3	C1/S4

This word is located in the Command/Indicate interrupt queue ; IQSR Register indicates the size of this interrupt queue located in the external memory.

NS : New Status.
Before writing the features of event in the external memory the Interrupt Controller reads the NS bit :
if NS = 0, the Interrupt Controller puts this bit at '1' when it writes the new primitive which has been received.
if NS = 1, the Interrupt Controller puts INTFOV bit at '1' to generate an interrupt (IR Interrupt Register).
When the microprocessor has read the status word, it puts this bit at '0' to acknowledge the new status. This location becomes free for the Interrupt Controller.

S0/S1 Source of the event:

S1	S0	G0	Word stored in shared memory
0	0	0	Primitive C1/6 received from GCI Multiplex 0 corresponding to DIN4
0	0	1	Primitive C1/6 received from GCI Multiplex 1 corresponding to DIN5
0	1	0	A, E, S1/S4 bits from any input timeslot switched to one timeslot 4n+3 of GCI 0 without outgoing to DOUT4
0	1	1	A, E, S1/S4 bits from any input timeslot switched to one timeslot 4n+3 of GCI 1 without outgoing to DOUT5
1	0	0	AIS detected during more 30 ms from any input timeslot and switched to B1, B2 channels (16 bits) of the GCI 0 (DOUT4) in transparent mode or not
1	0	1	AIS detected during more 30 ms from any input timeslot and switched to B1, B2 channels (16 bits) of the GCI 1 (DOUT5) in transparent mode or not.
1	1	X	Reserved

IX - EXTERNAL REGISTERS (continued)

G0 : This bit defines one of two GCI y (DIN4/DOUT4 or DIN5/DOUT5).
G0 = 0, GCI0 (DIN4/DOUT4) is the source.
G0 = 1, GCI1 (DIN5/DOUT5) is the source.

A2/0 : GCI Channel 0 to 7 belonging to GCI 0 or GCI 1.

C6/1 : New Primitive received twice consecutively. Case of S0=S1=0.
A, E, S1/S4 bits received twice consecutively. Case of S0 = 1 S1 = 0.
Bit0/5 are not Significant when S0 = 0, S1 = 1.

IX.5.2 - Receive Command / Indicate Interrupt when TSV = 1

Time Stamping validated (bit of GCR Register)

bit15							bit8	bit7							bit 0
NS	Nu	Nu	Nu	G0	A2	A1	A0	Nu	Nu	C6/A	C5/E	C4/S1	C3/S2	C2/S3	C1/S4
T15	T14	T13	T12	T11	T10	T9	T8	T7	T6	T5	T4	T3	T2	T1	T0

These two words are located in the Command/Indicate interrupt queue.

First word see definition above.

T0/15: binary counter value when a new primitive is occured.

IX.6 - Receive Monitor Interrupt

IX.6.1 - Receive Monitor Interrupt when TSV = 0

TSV : Time Stamping not Validated (bit of GCR Register)

bit15							bit8	bit7							bit 0
NS				G0	A2	A1	A0					ODD	A	F	L
M18	M17	M16	M15	M14	M13	M12	M11	M8	M7	M6	M5	M4	M3	M2	M1

These two words are transferred into the Monitor interrupt queue ; IQSR Register indicates the size of this interrupt queue located in the external memory.

NS : New Status.
Before writing the features of event in the external memory the Interrupt Controller reads the NS bit :
if NS = 0, the Interrupt Controller stores two new bytes M1/8 and M11/18 then puts NS bit at '1' when it writes the status of these two bytes which has been received.
if NS = 1, the Interrupt Controller puts ICOV bit at '1' to generate an interrupt (IR Register).

G0 : G0 = 0, GCI 0 corresponding to DIN4 input and DOUT4 output.
G0 = 1, GCI 1 corresponding to DIN5 input and DOUT5 output.

L : Last byte
L=1, two cases:
if ODD = 1, the following word of the Interrupt Queue contains the Last byte of message
if ODD =0, the previous word of the Interrupt Queue (concerning this channel) contains the Last byte of message.
L = 0, the following word and the previous word does not contains the Last byte of message.

F : First byte
F=1, the following word contains the First byte of message.
F=0, the following word does not contain the First byte of message.

A : Abort
A=1, Received message has been aborted.

IX - EXTERNAL REGISTERS (continued)

ODD : Odd byte number
ODD = 1, one byte has been written in the following word.
ODD = 0, two bytes have been written in the following word.

In case of V* protocol ODD,A,F,L bits are respectively 1,0,1,1.

M1/8 : New Byte received twice consecutively if GCI Protocol has been validated.
Byte received once if V* Protocol has been validated.

M11/18 : Next new Byte received twice consecutively if GCI Protocol has been validated.
This byte is at "1" in case of V* protocol.

IX.6.2 - Receive Monitor Interrupt when TSV = 1

TSV : Time Stamping Validated (bit of GCR Register)

bit15							bit8	bit7							bit 0
NS				G0	A2	A1	A0					ODD	A	F	L
M18	M17	M16	M15	M14	M13	M12	M11	M8	M7	M6	M5	M4	M3	M2	M1
T15	T14	T13	T12	T11	T10	T9	T8	T7	T6	T5	T4	T3	T2	T1	T0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

These four words are located in the Monitor interrupt queue ; IQSR Register indicates the size of this interrupt queue located in the external memory.

NS : New Status.
Before writing the features of event in the external memory the Interrupt Controller reads the NS bit :
if NS = 0, the Interrupt Controller stores two new bytes M1/8 and M11/18 then puts NS bit at '1' when it writes the status of these two bytes which has been received.
if NS = 1, the Interrupt Controller puts ICOV bit at '1' to generate an interrupt (IR Register).

G0 : G0 = 0, GCI 0 corresponding to DIN4 input and DOUT4 output.
G0 = 1, GCI 1 corresponding to DIN5 input and DOUT5 output.

L : Last byte
L=1, two cases:
if ODD = 1, the following word of the Interrupt Queue contains the Last byte of message
if ODD =0, the Last byte of message has been stored at the previous access of the Interrupt Queue (concerning this channel).
L=0, the following word and the previous word does not contain the Last byte of message.

F : First byte
F=1, the following word contains the First byte of message.
F=0, the First byte of message is not the following word.

A : Abort
A=1, Received message has been aborted.

ODD : Odd byte number
ODD = 1, one byte has been written in the following word.
ODD = 0, two bytes have been written in the following word.

M1/8 : New Byte received twice consecutively if GCI Protocol has been validated.
Byte received once if V* Protocol has been validated.

M11/18 : Next new Byte received twice consecutively if GCI Protocol has been validated.
This byte is at "1" in case of V* protocol.

T15/0 : Binary counter value when a new primitive is occurred.

X - PQFP160 PACKAGE MECHANICAL DATA

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			4.07			0.160
A1	0.25			0.010		
A2	3.17	3.42	3.67	0.125	0.135	0.144
B	0.22		0.38	0.009		0.015
C	0.13		0.23	0.005		0.009
D	30.95	31.20	31.45	1.219	1.228	1.238
D1	27.90	28.00	28.10	1.098	1.102	1.106
D3		25.35			0.998	
e		0.65			0.026	
E	30.95	31.20	31.45	1.219	1.228	1.238
E1	27.90	28.00	28.10	1.098	1.102	1.106
E3		25.35			0.998	
L	0.65	0.80	0.95	0.026	0.0315	0.0374
L1		1.60			0.063	
K	0^o (Min.), 7^o (Max.)