Preliminary

32K X 36 & 64K X 18 SRAM

Features

- 32K x 36 or 64K x 18 Organizations
- 0.5 Micron CMOS Technology
- Synchronous Pipeline Mode Of Operation with Self-Timed Late Write
- Single Differential PECL Clock compatible with LVTTL Levels
- Single +3.3V Power Supply and Ground
- Common I/O & LVTTL I/O Compatible
- Registered Addresses, Write Enables, Synchronous Select and Data Ins
- Registered Outputs
- Asynchronous Output Enable and Power Down Inputs
- Boundary Scan using limited set of JTAG 1149.1 functions
- Byte Write Capability & Global Write Enable
- 7 X 17 Bump Ball Grid Array Package with SRAM JEDEC Standard Pinout and Boundary SCAN Order.

Description

The IBM043611RLA and IBM041811RLA 1Mb SRAMs are Synchronous Pipeline Mode, high performance CMOS Static Random Access Memories that are versatile, wide I/O, and achieves 5 ns cycle times. Dual differential K clocks are used to initiate the read/write operation and all internal operations are self-timed. At the rising edge of the K Clock, all Addresses, Write-Enables, Sync Select and Data Ins are registered internally. Data Outs are updated from output registers off the next rising edge of the K Clock. An internal Write buffer allows write data to follow one cycle after addresses and controls. The chip is operated with a single +3.3V power supply and is compatible with LVTTL I/O interfaces.

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X36 BGA Bump Layout (Top View)

	1	2	3	4	5	6	7
A	VDDQ	SA8	SA7	NC	SA4	SA3	VDDQ
B	NC	NC	NC	NC	NC	NC	NC
C	NC	SA9	SA6	VDD	SA5	SA2	NC
D	DQ23	DQ18	VSS	NC	VSS	DQ17	DQ12
E	DQ19	DQ24	VSS	$\overline{SS}$	VSS	DQ11	DQ16
F	VDDQ	DQ20	VSS	$\overline{G}$	VSS	DQ15	VDDQ
G	DQ21	DQ25	$\overline{SBWc}$	NC	$\overline{SBWb}$	DQ10	DQ14
H	DQ26	DQ22	VSS	NC	VSS	DQ13	DQ9
J	VDDQ	VDD	NC	VDD	NC	VDD	VDDQ
K	DQ27	DQ31	VSS	K	VSS	DQ4	DQ8
L	DQ32	DQ28	$\overline{SBWd}$	$\overline{K}$	$\overline{SBWa}$	DQ7	DQ3
M	VDDQ	DQ33	VSS	$\overline{SW}$	VSS	DQ2	VDDQ
N	DQ34	DQ29	VSS	SA1	VSS	DQ6	DQ1
P	DQ30	DQ35	VSS	SA0	VSS	DQ0	DQ5
R	NC	SA14	M1*	VDD	M2*	SA10	NC
T	NC	NC	SA13	SA12	SA11	NC	ZZ
U	VDDQ	TMS	TDI	TCK	TDO	NC	VDDQ

Note: * M1 and M2 are clock mode pins. For this application, M1 and M2 need to connect to VSS and VDD, respectively.

X18 BGA Bump Layout (Top View)

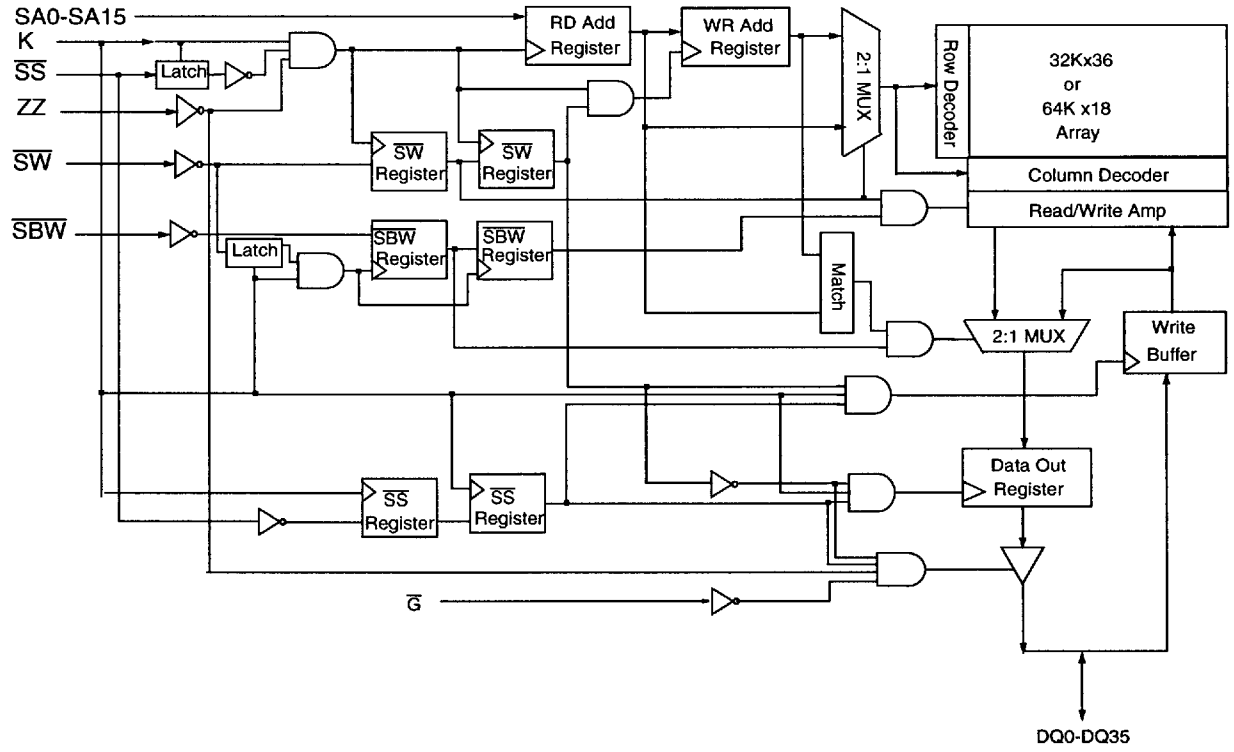
	1	2	3	4	5	6	7
A	VDDQ	SA8	SA7	NC	SA4	SA3	VDDQ
B	NC	NC	NC	NC	NC	NC	NC
C	NC	SA9	SA6	VDD	SA5	SA2	NC
D	DQ9	NC	VSS	NC	VSS	DQ8	NC
E	NC	DQ10	VSS	$\overline{SS}$	VSS	NC	DQ7
F	VDDQ	NC	VSS	$\overline{G}$	VSS	DQ6	VDDQ
G	NC	DQ11	$\overline{SBWb}$	NC	VSS	NC	DQ5
H	DQ12	NC	VSS	NC	VSS	DQ4	NC
J	VDDQ	VDD	NC	VDD	NC	VDD	VDDQ
K	NC	DQ13	VSS	K	VSS	NC	DQ3
L	DQ14	NC	VSS	$\overline{K}$	$\overline{SBWa}$	DQ2	NC
M	VDDQ	DQ15	VSS	$\overline{SW}$	VSS	NC	VDDQ
N	DQ16	NC	VSS	SA1	VSS	DQ1	NC
P	NC	DQ17	VSS	SA0	VSS	NC	DQ0
R	NC	SA15	M1	VDD	M2	SA11	NC
T	NC	SA13	SA14	NC	SA12	SA10	ZZ
U	VDDQ	TMS	TDI	TCK	TDO	NC	VDDQ

Note: * M1 and M2 are clock mode pins. For this application, M1 and M2 need to connect to VSS and VDD respectively.

Pin Description

SA0-SA15	Address Input	TDO	IEEE 1149 Test Output
DQa,DQb,DQc,DQd	Data I/O (DQ0-8,DQ9-17,DQ18-26,DQ27-35)	$\overline{SS}$	Synchronous Select
K, $\overline{K}$	Differential PECL CLocks (LVTTL Compatible)	M1, M2	Clock Mode Inputs
$\overline{SW}$	Write Enable, global	V_{DD}	Power Supply (+3.3V)
$\overline{SBWa}$	Write Enable, Byte a (DQ0 to DQ8)	V_{SS}	Ground
$\overline{SBWb}$	Write Enable, Byte b (DQ9 to DQ17)	V_{DDQ}	Output Power Supply
$\overline{SBWc}$	Write Enable, Byte c (DQ18 to DQ26)	$\overline{G}$	Asynchronous Output Enable
$\overline{SBWd}$	Write Enable, Byte d (DQ27 to DQ35)	ZZ	Asynchronous Sleep Mode
TMS,TDI,TCK	IEEE 1149 Test Inputs	NC	No Connect

Block Diagram



SRAM FEATURES

Late Write

Late Write function allows for write data to be registered one cycle after addresses and controls. This feature will alleviate SRAM data bus contention going from a Read to Write cycle by eliminating one dead cycle. Late Write is accomplished by buffering write addresses and data so that the write operation occurs during the next write cycle. In the case a read cycle occurs after a write cycle, the address and write data information are stored temporarily in holding registers. During the first write cycle preceded by a read cycle, the SRAM array will be updated with the address and data from the holding registers. Read cycle addresses are monitored to determine if read data is to be supplied from the SRAM array or the write buffer. The bypassing of the SRAM array data occurs on a byte by byte basis. When one byte is written during a write cycle, read data from the last written address will have new byte data from the write buffer and remaining bytes from the SRAM array.

Mode Control

Mode control pins: M1 and M2 are used to select four different JEDEC standard read protocols. This SRAM only supports the single clock pipeline (M1 = VSS, M2 = VDD) protocol. Mode control inputs must be set with power up and must not change during SRAM operation.

Power Down Mode

Power Down Mode, or "Sleep Mode" is accomplished by switching asynchronous signal ZZ high. When the SRAM is in Sleep Mode, the outputs will go to a HIZ state and the SRAM will draw standby current. SRAM data will be preserved and a recovery time (t_{ZZR}) is required before the SRAM resumes to normal operation.

Ordering Information

Part Number	Organization	Speed	Leads
IBM041811RLA - 5	64K x 18	2.5ns Access / 5 ns Cycle	7 X 17 BGA
IBM041811RLA - 6	64K x 18	3.0ns Access / 6ns Cycle	7 X 17 BGA
IBM041811RLA - 7	64K x 18	3.5ns Access / 7ns Cycle	7 X 17 BGA
IBM043611RLA - 5	32K x 36	2.5ns Access / 5 ns Cycle	7 X 17 BGA
IBM043611RLA - 6	32K x 36	3.0ns Access / 6ns Cycle	7 X 17 BGA
IBM043611RLA - 7	32K x 36	3.5ns Access / 7ns Cycle	7 X 17 BGA

Clock Truth Table

K	ZZ	$\overline{SS}$	$\overline{SW}$	$\overline{SBWa}$	$\overline{SBWb}$	$\overline{SBWc}$	$\overline{SBWd}$	DQ (n)	DQ (n+1)	MODE
L→H	L	L	H	X	X	X	X	X	Dout 0-35	Read Cycle All Bytes
L→H	L	L	L	L	H	H	H	X	Din 0-8	Write Cycle 1st Byte
L→H	L	L	L	H	L	H	H	X	Din 9-17	Write Cycle 2nd Byte
L→H	L	L	L	H	H	L	H	X	Din 18-26	Write Cycle 3rd Byte
L→H	L	L	L	H	H	H	L	X	Din 27-35	Write Cycle 4th Byte
L→H	L	L	L	L	L	L	L	X	Din 0-35	Write Cycle All Bytes
L→H	L	L	L	H	H	H	H	X	HIZ	Abort Write Cycle
L→H	L	H	X	X	X	X	X	X	HIZ	Deselect Cycle
X	H	X	X	X	X	X	X	HIZ	HIZ	Sleep Mode

Output Enable Truth Table

Operation	$\overline{G}$	DQ
Read	L	Dout 0-35
Read	H	HIZ
Sleep (ZZ=H)	X	HIZ
Write ($\overline{SW}$=L)	X	HIZ
Deselect ($\overline{SS}$=H)	X	HIZ

Absolute Maximum Ratings

Item	Symbol	Rating	Units	Notes
Power Supply Voltage	V_{DD}	-0.5 to 4.6	V	1
Output Power Supply Voltage	V_{DDQ}	-0.5 to 4.6	V	1
Input Voltage	V_{IN}	-0.5 to V_{DD}+0.5	V	1
Output Voltage	V_{OUT}	-0.5 to V_{DD}+0.5	V	1
Operating Temperature	T_A	0 to +70	°C	1
Storage Temperature	T_{STG}	-55 to +125	°C	1
Short Circuit Output Current	I_{OUT}	25	mA	1
Latchup Current	I_{LI}	>200	mA	

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions (T_A=0 to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Supply Voltage	V_{DD}	3.15	3.3	3.60	V	1
Input High Voltage	V_{IH}	2.2	—	V_{DD}+0.3	V	1,2
Input Low Voltage	V_{IL}	-0.3	—	0.8	V	1,3
PECL Clock Input High Voltage	$V_{IH\text{-}PECL}$	2.135	—	2.420	V	1,2
PECL Clock Input Low Voltage	$V_{IL\text{-}PECL}$	1.490	—	1.825	V	1,3
Output Current	I_{OUT}	—	5	8	mA	

1. All voltages referenced to V_{SS}. All V_{DD}, V_{DDQ} and V_{SS} pins must be connected.
2. V_{IH}(Max)DC = V_{DD} + 0.3 V, V_{IH}(Max)AC = V_{DD} + 1.5 V (pulse width ≤ 4.0ns)
3. V_{IL}(Min)DC = - 0.3 V, V_{IL}(Min)AC= -1.5 V (pulse width ≤ 4.0ns)

Capacitance (T_A=0 to +70 C, V_{DD}=3.3 -5% + 10% V, f=1MHz)

Parameter	Symbol	Test Condition	Max	Units
Input Capacitance	C_{IN}	V_{IN} = 0V	5	pF
Data I/O Capacitance (DQ0-DQ35)	C_{OUT}	V_{OUT} = 0V	5	pF

DC Electrical Characteristics (T_A= 0 to +70 C, V_{DD}=3.3 -5% + 10% V)

Parameter	Symbol	Min.	Max.	Units	Notes
Average Power Supply Operating Current - X36 (I_{OUT} = 0, V_{IN} = V_{IH} or V_{IL} , ZZ & $\overline{SS}$ = V_{IL})	I_{DD5} I_{DD6} I_{DD7}	— —	630 540 470	mA	1
Average Power Supply Operating Current - X18 (I_{OUT} = 0, V_{IN} = V_{IH} or V_{IL}, ZZ & $\overline{SS}$ = V_{IL})	I_{DD5} I_{DD6} I_{DD7}	— —	590 500 440	mA	1
Power Supply Standby Current ($\overline{SS}$= V_{IH}, or ZZ =V_{IH} All other inputs = V_{IH} or V_{IL}, I_{OUT} = 0)	I_{SB}	—	10	mA	1
Input Leakage Current, any input (V_{IN} = Vss or V_{DD})	I_{LI}	—	+1	µA	
Output Leakage Current (V_{OUT} = Vss or V_{DD}, DQ in HIZ	I_{LO}	—	+1	µA	
Output High "H" Level Voltage (I_{OH}=-8mA @ 2.4V)	V_{OH}	2.4	—	V	
Output Low "L" Level Voltage (I_{OL}=+8mA @ 0.4V)	V_{OL}	—	0.4	V	

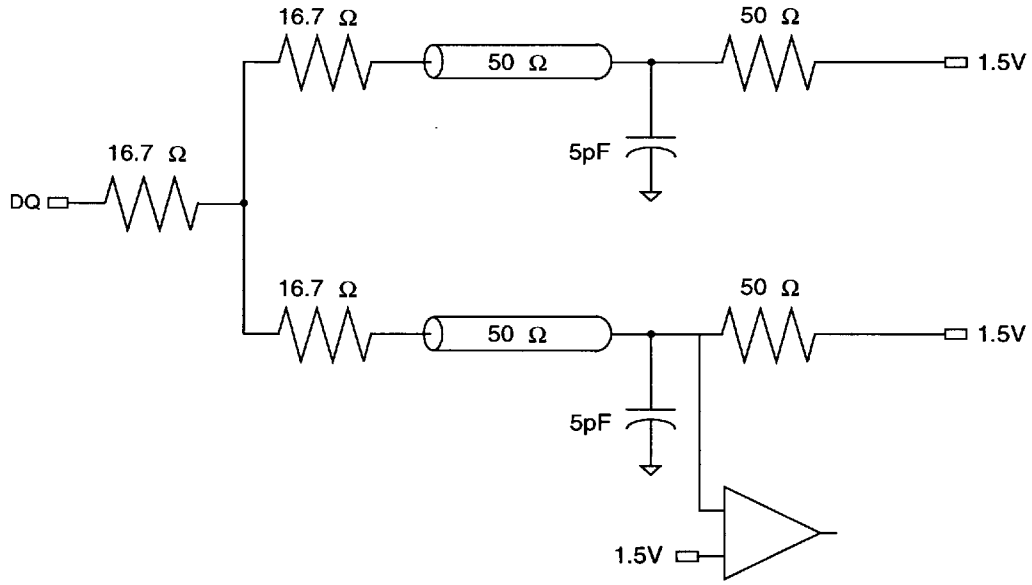
1. I_{OUT} = Chip Output Current

AC Test Conditions (T_A=0 to +70C, V_{DD}=3.3 -5% + 10% V)

Parameter	Symbol	Conditions	Units	Notes
Input High Level	V_{IH}	3.0	V	
Input Low Level	V_{IL}	0.0	V	
PECL Clock Input High Voltage	$V_{IH-PECL}$	2.4	V	
PECL Clock Input Low Voltage	$V_{IL-PECL}$	1.5	V	
Input Rise Time	T_R	1.0	ns	
Input Fall Time	T_F	1.0	ns	
PECL Clock Input Rise Time	T_{R-PECL}	0.5	ns	
PECL Clock Input Fall Time	T_{F-PECL}	0.5	ns	
Input and Output Timing Reference Level (except K,$\overline{K}$)		1.5	V	
PECL Clock Reference Level		K and $\overline{K}$ Cross Point	V	
Output Load Conditions				1

1. See AC Test Loading on page 7.

AC Test Loading

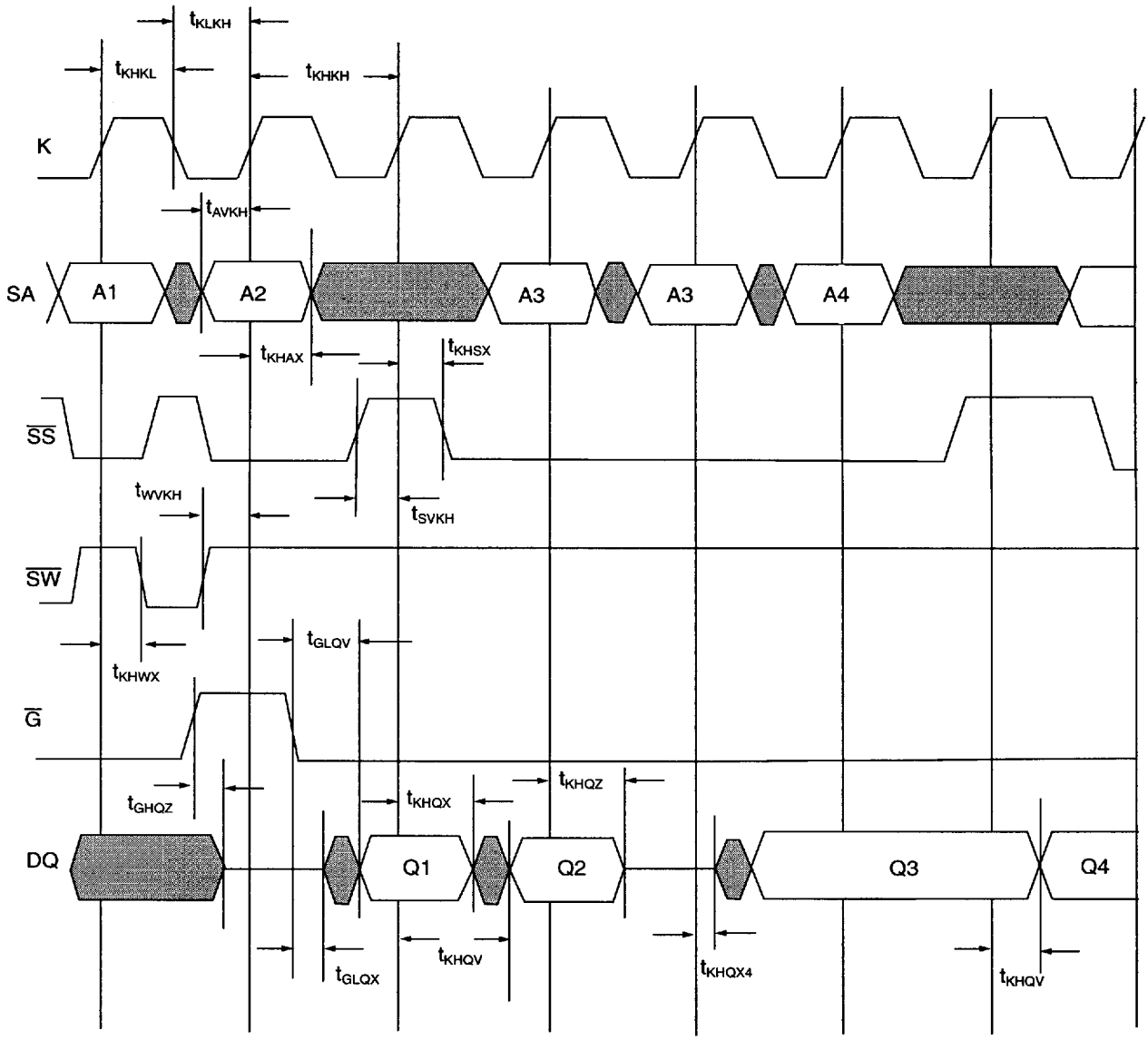


AC Characteristics (T_A=0 to +70C, V_{DD}=3.3 -5% + 10% V)

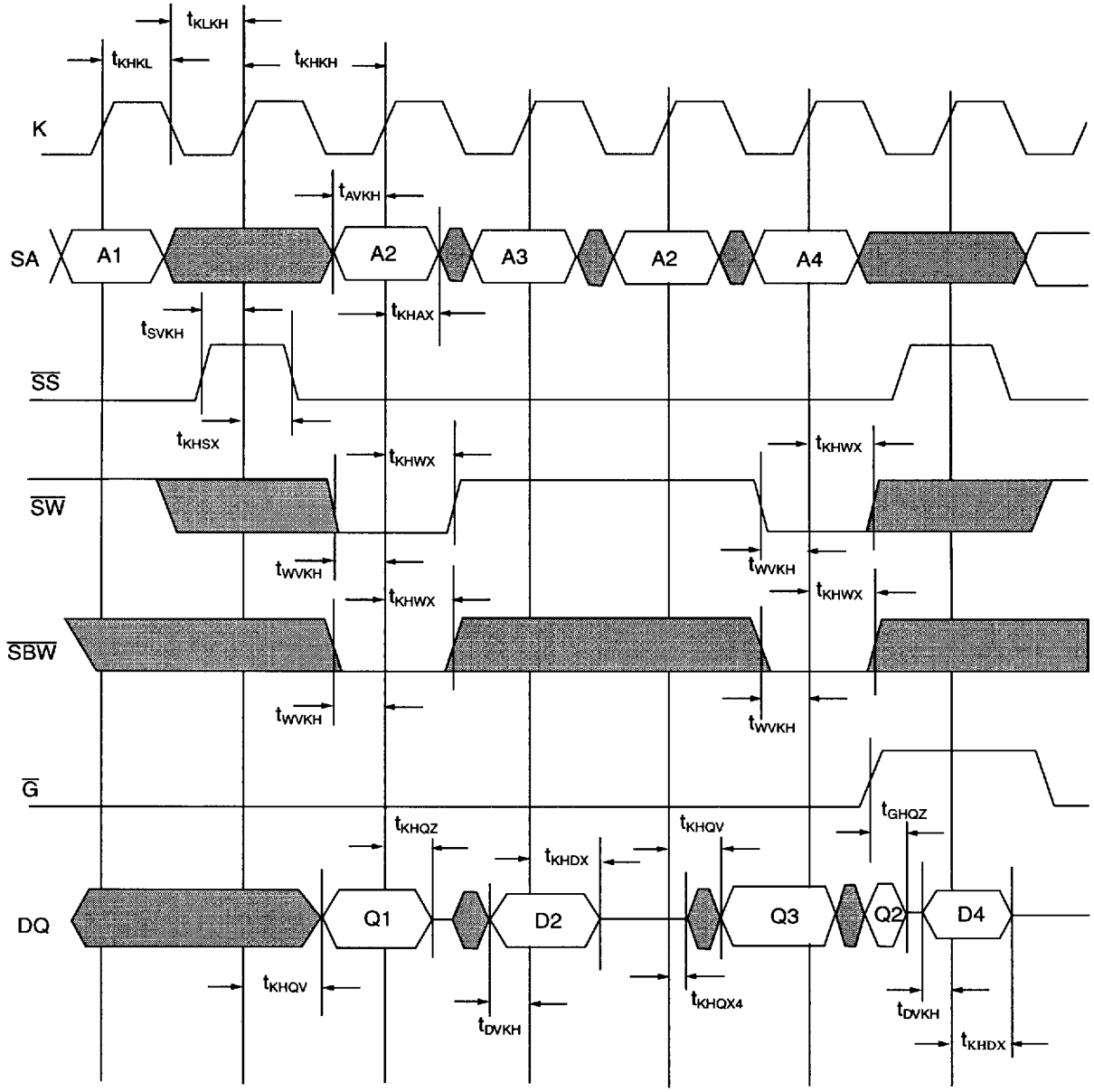
Parameter	Symbol	-5		-6		-7		Units	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
Cycle Time	t_{KHKH}	5.0	—	6.0	—	7.0	—	ns	
Clock High Pulse Width	t_{KHKL}	1.5	—	1.5	—	1.5	—	ns	
Clock Low Pulse Width	t_{KLKH}	1.5	—	1.5	—	1.5	—	ns	
Clock to Output Valid	t_{KHQV}	—	2.5	—	3.0	—	3.5	ns	1
Address Setup Time	t_{AVKH}	0.5	—	0.5	—	0.5	—	ns	
Address Hold Time	t_{KHAX}	1.0	—	1.0	—	1.0	—	ns	
Sync Select Setup Time	t_{SVKH}	0.5	—	0.5	—	0.5	—	ns	
Sync Select Hold Time	t_{KHSX}	1.0	—	1.0	—	1.0	—	ns	
Write Enables Setup Time	t_{WVKH}	0.5	—	0.5	—	0.5	—	ns	
Write Enables Hold Time	t_{KHWX}	1.0	—	1.0	—	1.0	—	ns	
Data In Setup Time	t_{DVKH}	0.5	—	0.5	—	0.5	—	ns	
Data In Hold Time	t_{KHDX}	1.0	—	1.0	—	1.0	—	ns	
Data Out Hold Time	t_{KHQX}	0.5	—	0.5	—	0.5	—	ns	1
Clock High to Output High Z	t_{KHQZ}	—	2.5	—	3.0	—	3.5	ns	1,2
Clock High to Output Active	t_{KHQX4}	1.0	—	1.0	—	1.0	—	ns	1,2
Output Enable to High Z	t_{GHQZ}	—	2.5		3.0	—	3.5	ns	1,2
Output Enable to Low Z	t_{GLQX}	0.5	—	0.5	—	0.5	—	ns	1,2
Output Enable to Output Valid	t_{GLQV}	—	2.5	—	3.0	—	3.5	ns	1
Sleep Mode Recovery TIme	t_{ZZR}	5	—	6	—	7	—	ns	
Sleep Mode Enable TIme	t_{ZZE}	—	5	—	6	—	7	ns	

1. See AC Test Loading on page 7
2. Transitions are measured ± 200 mV from steady state voltage.

Timing Diagram (Read and Deselect Cycles)



Timing Diagram (Read Write Cycles)



NOTES:

1. D2 is the input data written in memory location A2.
2. Q2 is output data read from the write buffer, as a result of address A2 being a match from the last write cycle address.

IEEE 1149.1 TAP AND BOUNDARY SCAN

The SRAM provides a limited set of JTAG functions intended to test the interconnection between SRAM I/Os and printed circuit board traces or other components. There is no multiplexer in the path from I/O pins to the RAM core.

In conformance with IEEE std. 1149.1, the SRAM contains a TAP controller, Instruction register, Boundary Scan register, Bypass register and ID register.

The TAP controller has a standard 16-state machine that resets internally upon power-up, therefore, TRST signal is not required.

Signal List

- TCK: Test Clock
- TMS: Test Mode Select
- TDI: Test Data In
- TDO: Test Data Out

Caution: TCK,TMS,TDI must be tied down, even when JTAG is not used.

JTAG Recommended DC Operating Conditions (T_A=0 to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
JTAG Input High Voltage	V_{IH1}	2.2	—	V_{DD}+0.3	V	1
JTAG Input Low Voltage	V_{IL1}	-0.3	—	0.8	V	1
JTAG Output High Level	V_{OH1}	2.4	—	—	V	1,2
JTAG Output Low Level	V_{OL1}	—	—	0.4	V	1,3

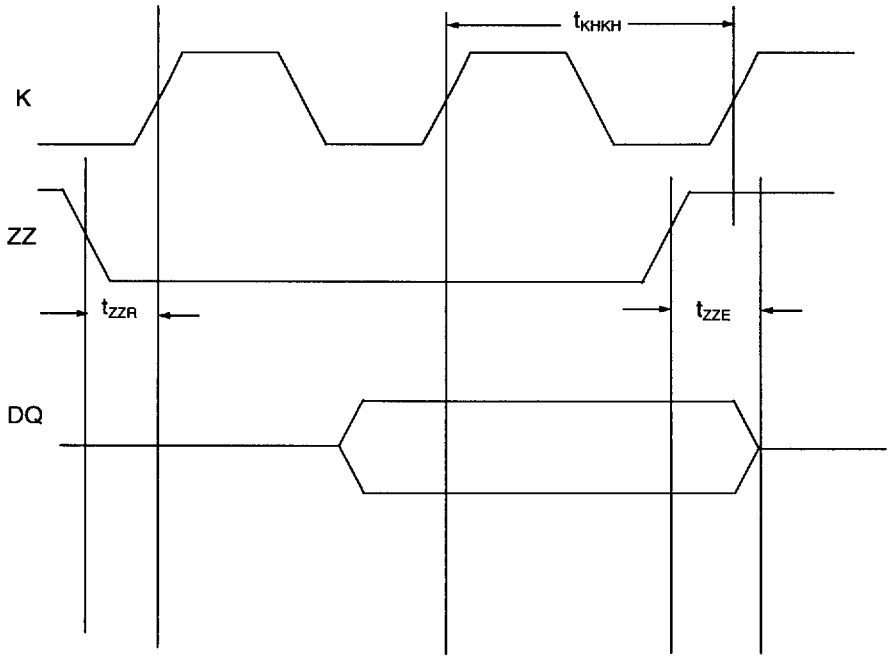
1. All JTAG Inputs/Outputs are LVTTL Compatible only.
2. I_{OH1} = -8mA at 2.4V.
3. IOL1 = +8mA at 0.4V.

JTAG AC Test Conditions (T_A=0 to +70C, V_{DD}=3.3 -5% + 10% V)

Parameter	Symbol	Conditions	Units	Notes
Input Pulse High Level	V_{IH1}	3.0	V	
Input Pulse Low Level	V_{IL1}	0.0	V	
Input Rise Time	T_{R1}	2.0	ns	
Input Fall Time	T_{F1}	2.0	ns	
Input and Output Timing Reference Level		1.5	V	1

1. See AC Test Loading on page 7

Timing Diagram (Sleep Mode)

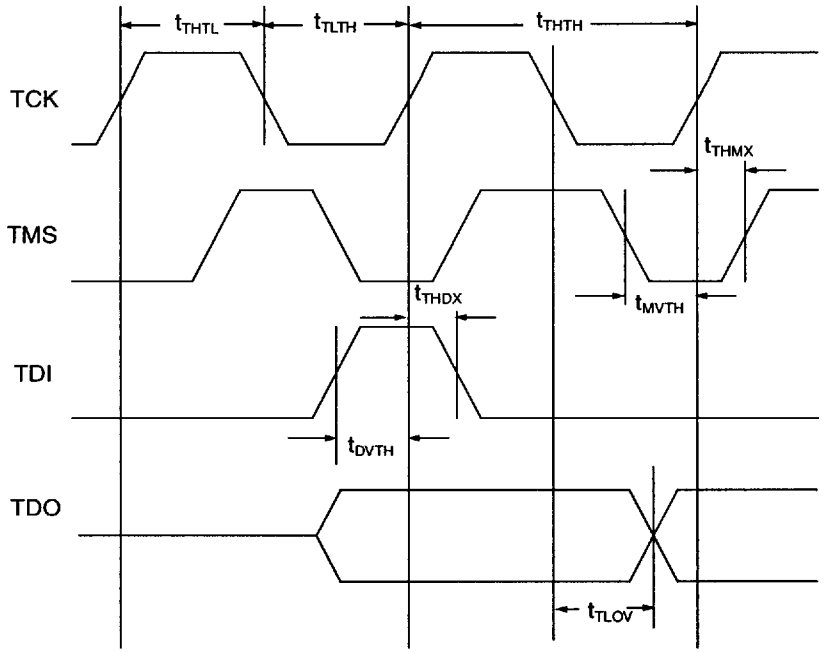


JTAG AC Characteristics (T_A=0 to +70C, V_{DD}=3.3 -5% + 10% V)

Parameter	Symbol	Min.	Max.	Units	Notes
TCK Cycle Time	t_{THTH}	20	—	ns	
TCK High Pulse Width	t_{THTL}	7	—	ns	
TCK Low Pulse Width	t_{TLTH}	7	—	ns	
TMS Setup	t_{MVTH}	4	—	ns	
TMS Hold	t_{THMX}	4	—	ns	
TDI Setup	t_{DVTH}	4	—	ns	
TDI Hold	t_{THDX}	4	—	ns	
TCK Low to Valid Data	t_{TLOV}	—	7	ns	1

1. See AC Test Loading on page 7

JTAG Timing Diagram



Scan Register Definition

Register Name	Bit Size X18	Bit Size X36
Instruction	3	3
Bypass	1	1
ID	32	32
Boundary Scan *	51	70

* The Boundary Scan chain consists of the following bits:
- 36 or 18 bits for Data Inputs Depending on X18 or X36 Configuration
- 15 bits for $\overline{SA0}$ - SA14 for X36, 16 bits for $\overline{SA0}$ - SA15 for X18
- 4 bits for $\overline{SBWa}$ - $\overline{SBWd}$ in X36, 2 bits for $\overline{SBWa}$ and $\overline{SBWb}$ in X18
- 8 bits for K, $\overline{K}$, $\overline{SS}$, $\overline{G}$, $\overline{SW}$, ZZ, M1 and M2
- 7 bits for Place Holders

* K and $\overline{K}$ clocks connect to a differential receiver that generates a single-ended clock signal. This signal and its inverted value are used for Boundary Scan sampling.

ID Register Definition

Part	Field Bit Number and Description				
	Revision Number (31:28)	Device Density and Configuration (27:18)	Vendor Definition (17:12)	Manufacture JEDEC Code (11:1)	Start Bit(0)
64K X18	0000	001 000 0011	000001	000 101 001 00	1
32K X36	0000	000 110 0100	000001	000 101 001 00	1

Instruction Set

Code	Instruction	Notes
000	SAMPLE-Z	1
001	IDCODE	2
010	SAMPLE-Z	1
011	BYPASS	3
100	SAMPLE	4
101	BYPASS	3
110	BYPASS	3
111	BYPASS	3

1. Places DQs in HIZ in order to sample all input data regardless of other SRAM inputs.
2. TDI is sampled as an input to the first ID register to allow for the serial shift of the external TDI data.
3. BYPASS register is initiated to VSS when BYPASS instruction is invoked. The BYPASS register also holds the last serially loaded TDI when exiting the Shift DR state.
4. SAMPLE instruction does not place DQs in HIZ.

List of IEEE 1149.1 standard violations:

- 7.2.1.b, e
- 7.7.1.a-f
- 10.1.1.b, e
- 10.7.1.a-d

Boundary Scan Order (X36)

(PH =Place Holder)

Exit Order	Signal	Bump #	Exit Order	Signal	Bump #	Exit Order	Signal	Bump #
1	M2	5R	25	DQb	6F	49	DQc	2H
2	SA	4P	26	DQb	7E	50	DQc	1H
3	SA	4T	27	DQb	6E	51	$\overline{SBWc}$	3G
4	SA	6R	28	DQb	7D	52	PH**	4D
5	SA	5T	29	DQb	6D	53	$\overline{SS}$	4E
6	ZZ	7T	30	SA	6A	54	PH*	4G
7	DQa	6P	31	SA	6C	55	PH**	4H
8	DQa	7P	32	SA	5C	56	$\overline{SW}$	4M
9	DQa	6N	33	SA	5A	57	$\overline{SBWd}$	3L
10	DQa	7N	34	PH*	6B	58	DQd	1K
11	DQa	6M	35	PH*	5B	59	DQd	2K
12	DQa	6L	36	PH*	3B	60	DQd	1L
13	DQa	7L	37	PH*	2B	61	DQd	2L
14	DQa	6K	38	SA	3A	62	DQd	2M
15	DQa	7K	39	SA	3C	63	DQd	1N
16	$\overline{SBWa}$	5L	40	SA	2C	64	DQd	2N
17	$\overline{K}$	4L	41	SA	2A	65	DQd	1P
18	K	4K	42	DQc	2D	66	DQd	2P
19	$\overline{G}$	4F	43	DQc	1D	67	SA	3T
20	$\overline{SBWb}$	5G	44	DQc	2E	68	SA	2R
21	DQb	7H	45	DQc	1E	69	SA	4N
22	DQb	6H	46	DQc	2F	70	M1	3R
23	DQb	7G	47	DQc	2G			
24	DQb	6G	48	DQc	1G			

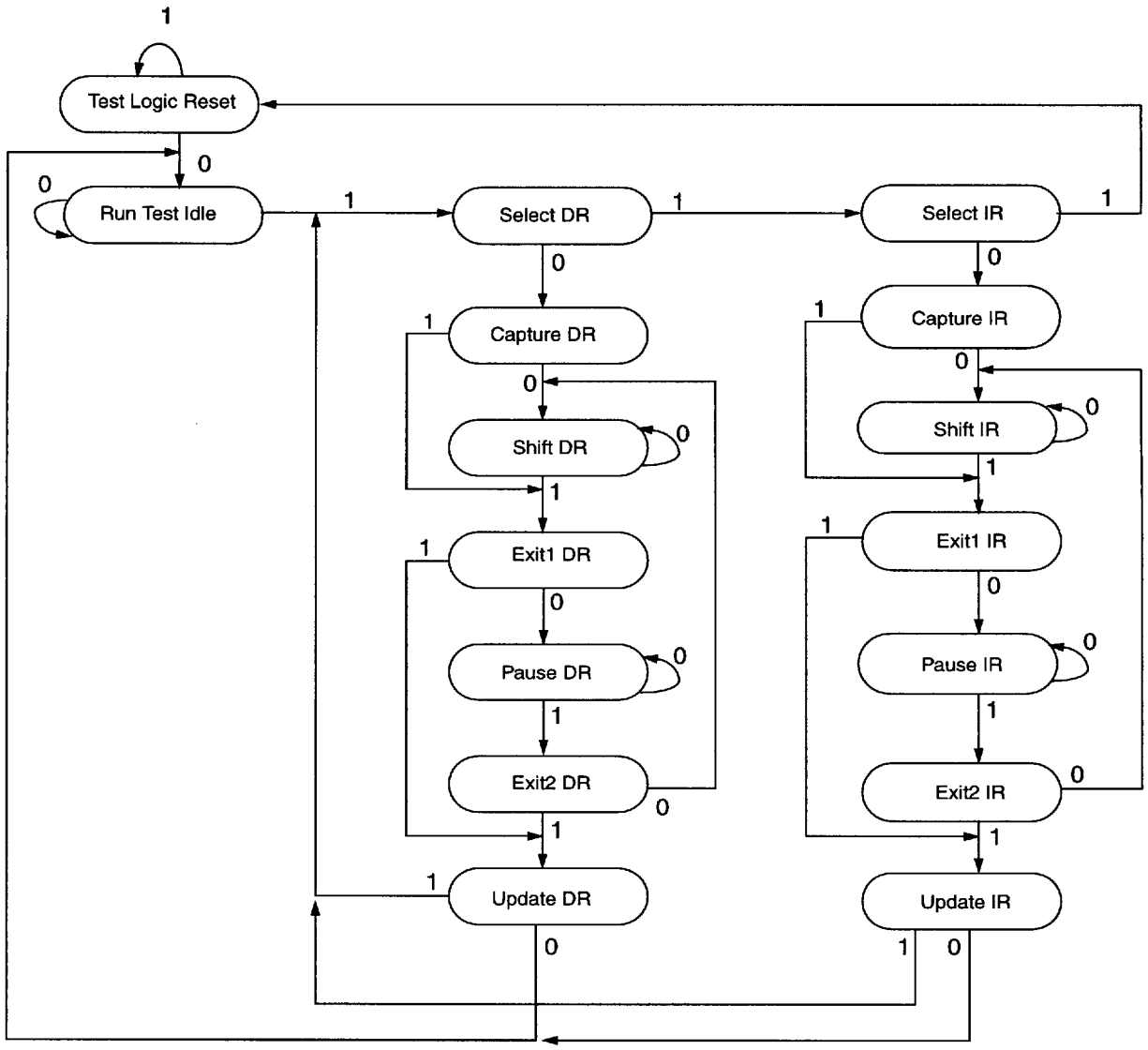
1. * Input of PH register connected to VSS
2. ** Input of PH register connected to VDD

Boundary Scan Order (X18)

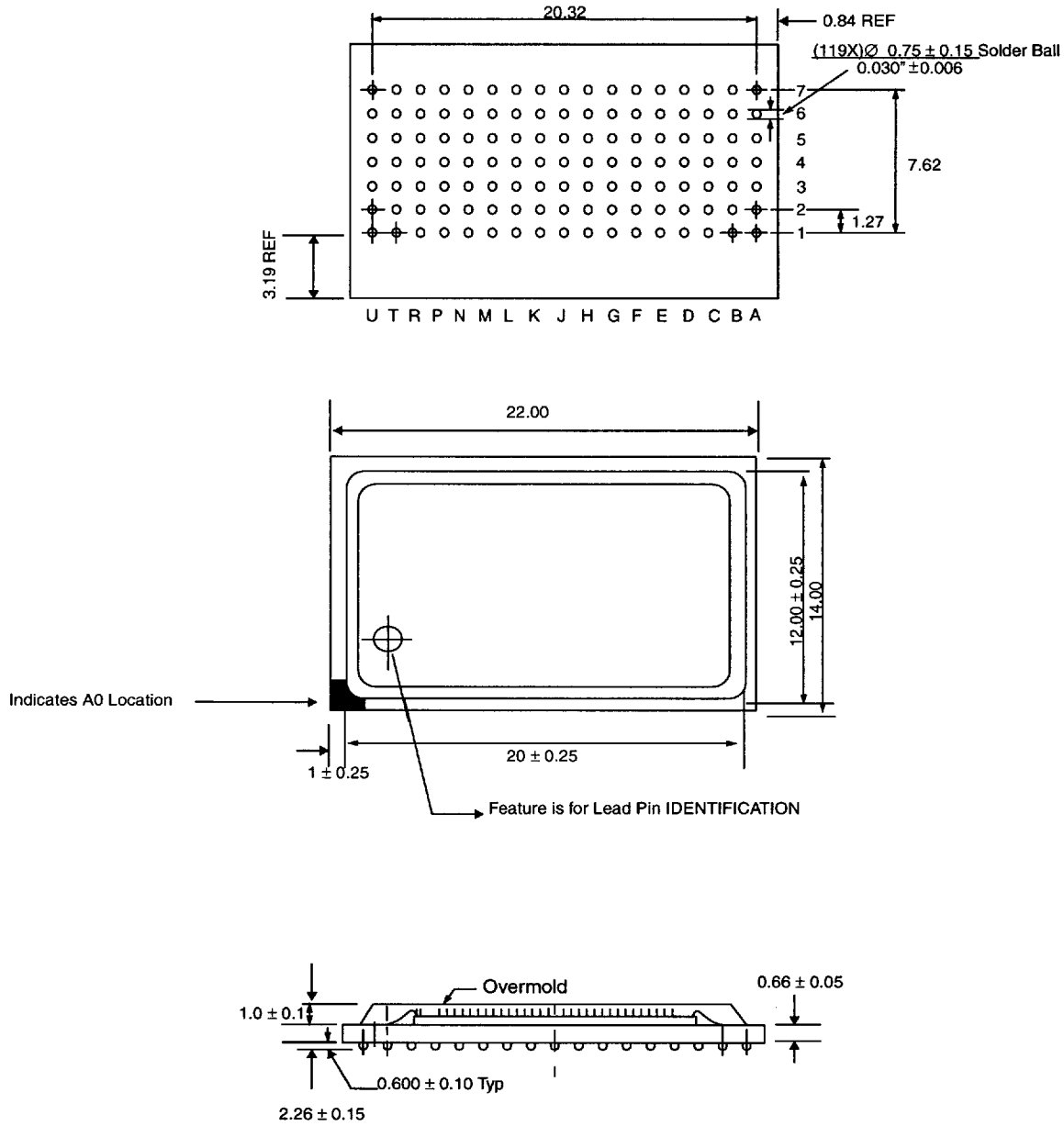
Exit Order	Signal	Bump #	Exit Order	Signal	Bump #
1	M2	5R	**27**	PH*	2B
2	SA	6T	**28**	SA	3A
3	SA	4P	**29**	SA	3C
4	SA	6R	**30**	SA	2C
5	SA	5T	**31**	SA	2A
6	ZZ	7T	**32**	DQb	1D
7	DQa	7P	**33**	DQb	2E
8	DQa	6N	**34**	DQb	2G
9	DQa	6L	**35**	DQb	1H
10	DQa	7K	**36**	$\overline{SBWb}$	3G
11	$\overline{SBWa}$	5L	**37**	PH**	4D
12	$\overline{K}$	4L	**38**	$\overline{SS}$	4E
13	K	4K	**39**	PH*	4G
14	$\overline{G}$	4F	**40**	PH**	4H
15	DQa	6H	**41**	$\overline{SW}$	4M
16	DQa	7G	**42**	DQb	2K
17	DQa	6F	**43**	DQb	1L
18	DQa	7E	**44**	DQb	2M
19	DQa	6D	**45**	DQb	1N
20	SA	6A	**46**	DQb	2P
21	SA	6C	**47**	SA	3T
22	SA	5C	**48**	SA	2R
23	SA	5A	**49**	SA	4N
24	PH*	6B	**50**	SA	2T
25	PH*	5B	**51**	M1	3R
26	PH*	3B			

1. * Input of PH register connected to VSS
2. ** Input of PH register connected to VDD

TAP Controller State Machine



7 x 17 BGA Dimensions



Note: All dimensions in Millimeters

Revision Log

Rev	Contents of Modification
6/94	Initial Release of the 32K x 36 & 64K x 18 (5/6/7) BGA FLOW THRU Application Spec.
1/95	Addition of SRAM Features section. Changed parameter/signal names for JEDEC compatibility.
2/95	Add package dimensions and identify SA and DQ pins.
4/95	Add Technology Product Names --page 1
5/95	Fax Server Release.
7/95	WWW release.
8/95	Update power numbers.