BUH51

SWITCHMODE™ NPN Silicon Planar Power Transistor

The BUH51 has an application specific state−of−art die designed for use in 50 W Halogen electronic transformers.

This power transistor is specifically designed to sustain the large inrush current during either the startup conditions or under a short circuit across the load.

- Improved Efficiency Due to the Low Base Drive Requirements:
  - High and Flat DC Current Gain h_{FE}
  - Fast Switching
- Epoxy Meets UL 94 V−0 @ 0.125 in
- ESD Ratings:
  - Machine Model, C
  - Human Body Model, 3B
- **This device is available in Pb−free package(s). Specifications herein apply to both standard and Pb−free devices. Please see our website at www.onsemi.com for specific Pb−free orderable part numbers, or contact your local ON Semiconductor sales office or representative.**

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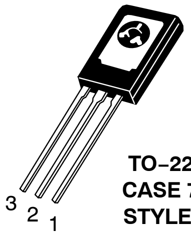
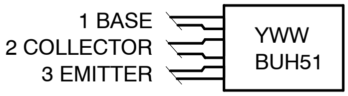
POWER TRANSISTOR
3.0 AMPERE
800 VOLTS
50 WATTS



TO−225
CASE 77
STYLE 3

MARKING DIAGRAM



Y = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
BUH51	TO−225	500 Units/Box

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Sustaining Voltage	V_{CEO}	500	Vdc
Collector−Base Breakdown Voltage	V_{CBO}	800	Vdc
Collector−Emitter Breakdown Voltage	V_{CES}	800	Vdc
Emitter−Base Voltage	V_{EBO}	10	Vdc
Collector Current − Continuous − Peak (Note 1)	I_C I_{CM}	3.0 8.0	Adc
Base Current − Continuous − Peak (Note 1)	I_B I_{BM}	2.0 4.0	Adc
*Total Device Dissipation @ T_C = 25°C *Derate above 25°C	P_D	50 0.4	Watt W/°C
Operating and Storage Temperature	T_J, T_{stg}	−65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	2.5	°C/W
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	100	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from case for 5 seconds	T_L	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

March, 2006 − Rev. 5

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic			Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Collector−Emitter Sustaining Voltage (I_C = 100 mA, L = 25 mH)			$V_{CEO(sus)}$	500	550	–	Vdc
Collector−Base Breakdown Voltage (I_{CBO} = 1.0 mA)			V_{CBO}	800	950	–	Vdc
Emitter−Base Breakdown Voltage (I_{EBO} = 1.0 mA)			V_{EBO}	10	12.5	–	Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, I_B = 0			I_{CEO}	–	–	100	μAdc
Collector Cutoff Current (V_{CE} = Rated V_{CES}, V_{EB} = 0)		@ T_C = 25°C @ T_C = 125°C	I_{CES}	– –	– –	100 1000	μAdc
Collector Base Current (V_{CB} = Rated V_{CBO}, V_{EB} = 0		@ T_C = 25°C @ T_C = 125°C	I_{CBO}	– –	– –	100 1000	μAdc
Emitter−Cutoff Current (V_{EB} = 9.0 Vdc, I_C = 0)			I_{EBO}	–	–	100	μAdc
ON CHARACTERISTICS							
Base−Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.2 Adc)		@ T_C = 25°C @ T_C = 125°C	$V_{BE(sat)}$	– –	0.92 0.8	1.1 –	Vdc
Collector−Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.2 Adc)		@ T_C = 25°C @ T_C = 125°C	$V_{CE(sat)}$	– –	0.3 0.32	0.5 0.6	Vdc
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)		@ T_C = 25°C @ T_C = 125°C	h_{FE}	8.0 6.0	10 8.0	– –	–
(I_C = 2.0 Adc, V_{CE} = 5.0 Vdc)		@ T_C = 25°C @ T_C = 125°C		5.0 4.0	7.5 6.2	– –	–
(I_C = 0.8 Adc, V_{CE} = 5.0 Vdc)		@ T_C = 25°C @ T_C = 125°C		10 8.0	14 13	– –	–
(I_C = 10 mAdc, V_{CE} = 5.0 Vdc)		@ T_C = 25°C @ T_C = 125°C		14 18	20 25	– –	–
DYNAMIC SATURATION VOLTAGE							
Dynamic Saturation Voltage: Determined 3.0 μs after rising I_{B1} reaches 90% of final I_{B1}	I_C = 1.0 Adc, I_{B1} = 0.2 Adc V_{CC} = 300 V	@ T_C = 25°C	$V_{CE(dsat)}$	–	1.7	–	V
		@ T_C = 125°C		–	6.0	–	V
	I_C = 2.0 Adc, I_{B1} = 0.4 Adc V_{CC} = 300 V	@ T_C = 25°C		–	5.1	–	V
		@ T_C = 125°C		–	15	–	V
DYNAMIC CHARACTERISTICS							
Current Gain Bandwidth (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)			f_T	–	23	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)			C_{ob}	–	34	100	pF
Input Capacitance (V_{EB} = 8.0 Vdc, f = 1.0 MHz)			C_{ib}	–	200	500	pF

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic			Symbol	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS: Resistive Load (D.C. ≤ 10%, Pulse Width = 40 μs)							
Turn−on Time	I_C = 1.0 Adc, I_{B1} = 0.2 Adc I_{B2} = 0.2 Adc V_{CC} = 300 Vdc	@ T_C = 25°C @ T_C = 125°C	t_{on}	– –	110 125	150 –	ns
Turn−off Time		@ T_C = 25°C @ T_C = 125°C	t_{off}	– –	3.5 4.1	4.0 –	μs
Turn−on Time	I_C = 2.0 Adc, I_{B1} = 0.4 Adc I_{B2} = 0.4 Adc V_{CC} = 300 Vdc	@ T_C = 25°C @ T_C = 125°C	t_{on}	– –	700 1250	1000 –	ns
Turn−off Time		@ T_C = 25°C @ T_C = 125°C	t_{off}	– –	1.75 2.1	2.0 –	μs
SWITCHING CHARACTERISTICS: Inductive Load (V_{clamp} = 300 V, V_{CC} = 15 V, L = 200 μH)							
Fall Time	I_C = 1.0 Adc I_{B1} = 0.2 Adc I_{B2} = 0.2 Adc	@ T_C = 25°C @ T_C = 125°C	t_{fi}	– –	200 320	300 –	ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_{si}	– –	3.4 4.0	3.75 –	μs
Crossover Time		@ T_C = 25°C @ T_C = 125°C	t_c	– –	350 640	500 –	ns
Fall Time	I_C = 2.0 Adc I_{B1} = 0.4 Adc I_{B2} = 0.4 Adc	@ T_C = 25°C @ T_C = 125°C	t_{fi}	– –	140 300	200 –	ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_{si}	– –	2.3 2.8	2.75 –	μs
Crossover Time		@ T_C = 25°C @ T_C = 125°C	t_c	– –	400 725	600 –	ns

TYPICAL STATIC CHARACTERISTICS

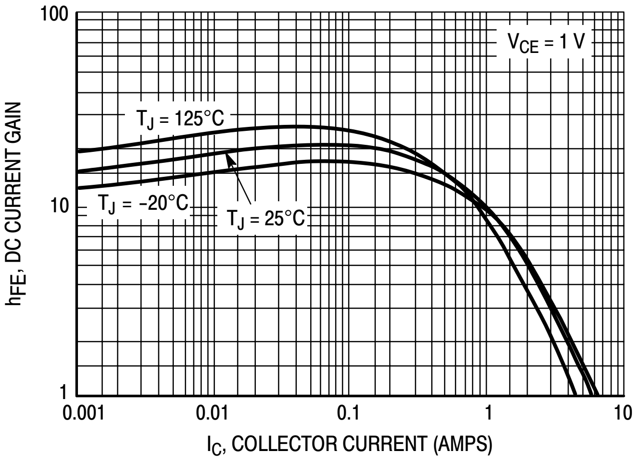


Figure 1. DC Current Gain @ 1.0 V

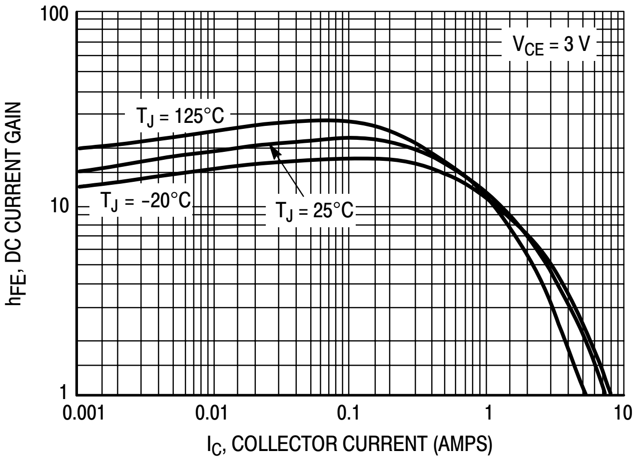


Figure 2. DC Current Gain @ 3.0 V

TYPICAL STATIC CHARACTERISTICS

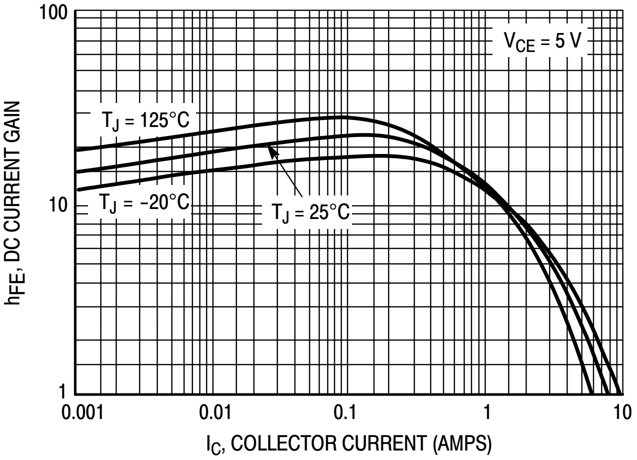


Figure 3. DC Current Gain @ 5.0 V

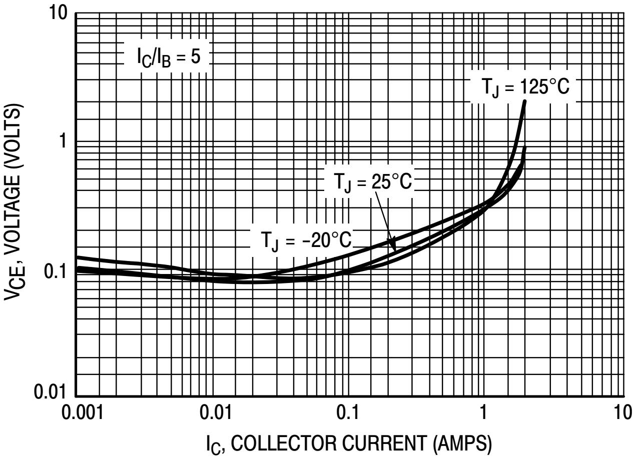


Figure 4. Collector−Emitter Saturation Voltage

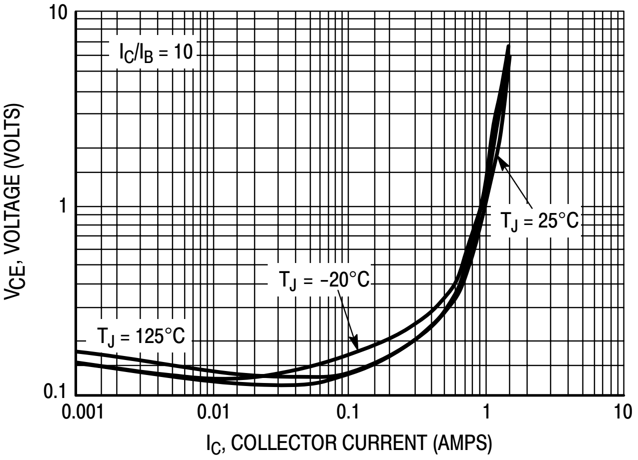


Figure 5. Collector−Emitter Saturation Voltage

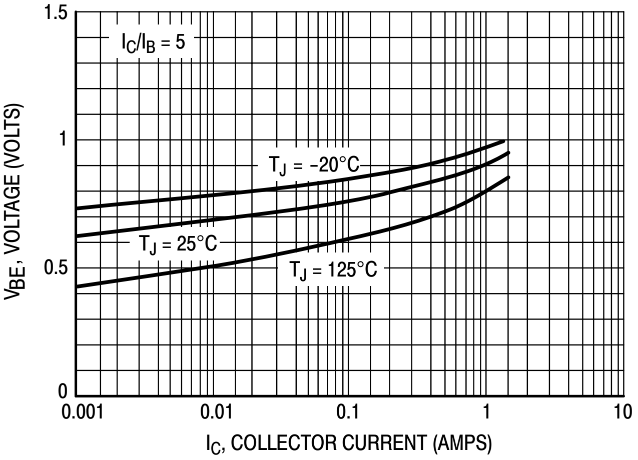


Figure 6. Base−Emitter Saturation Region

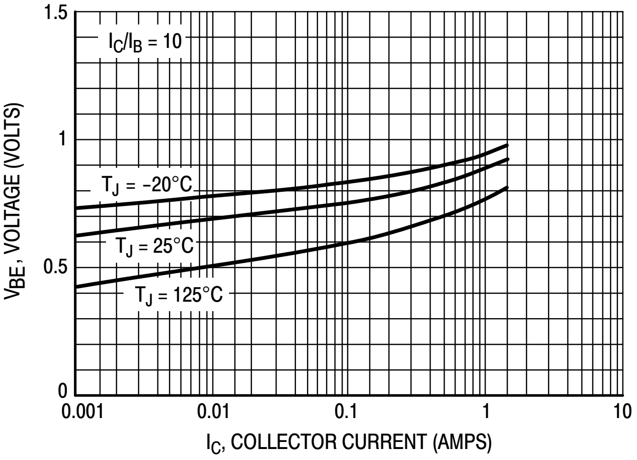


Figure 7. Base−Emitter Saturation Region

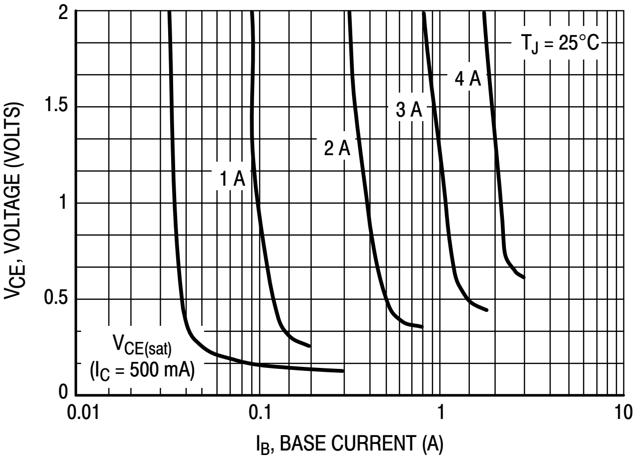


Figure 8. Collector Saturation Region

TYPICAL STATIC CHARACTERISTICS

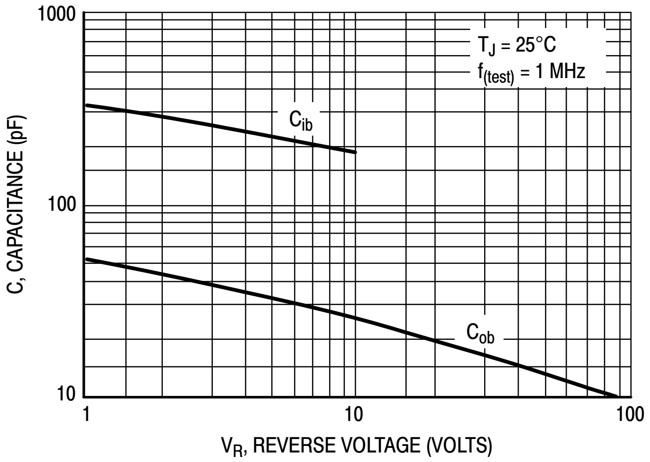


Figure 9. Capacitance

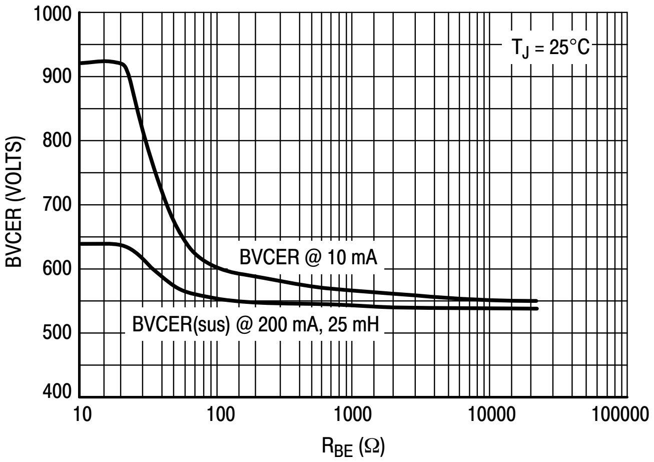


Figure 10. Resistive Breakdown

TYPICAL SWITCHING CHARACTERISTICS

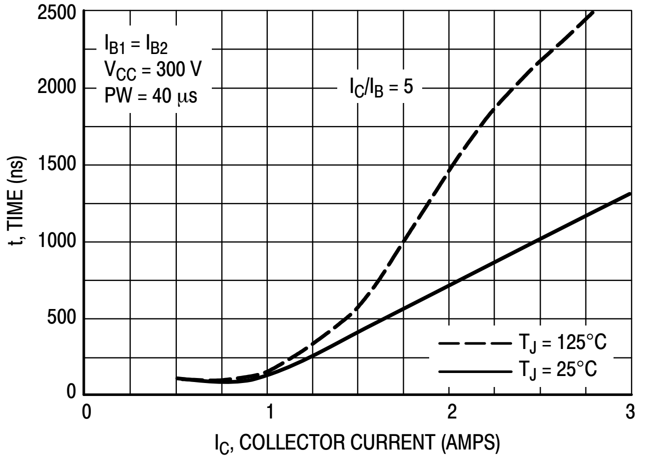


Figure 11. Resistive Switching, t$_{on}$

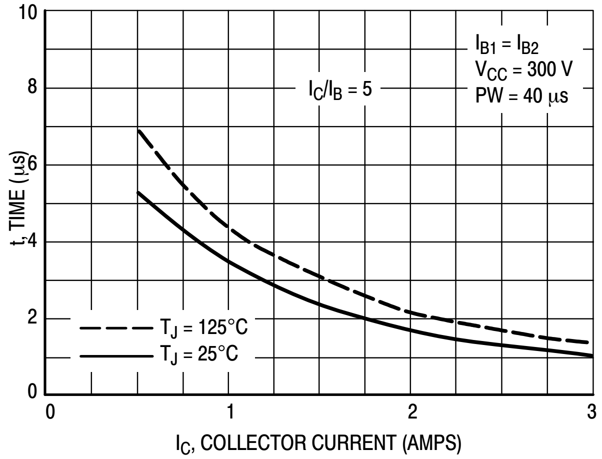


Figure 12. Resistive Switch Time, t$_{off}$

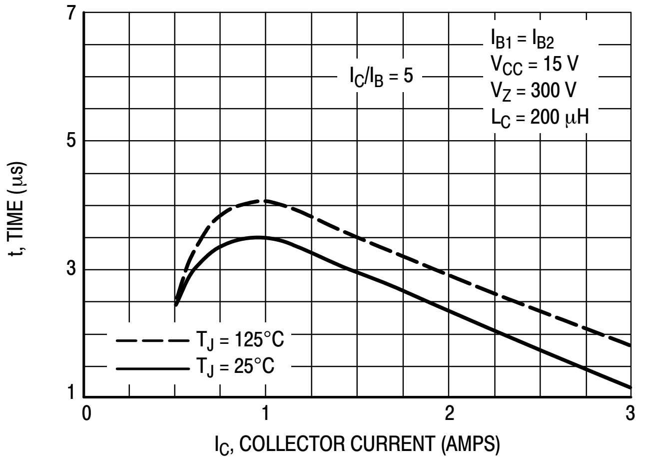


Figure 13. Inductive Storage Time, t$_{si}$

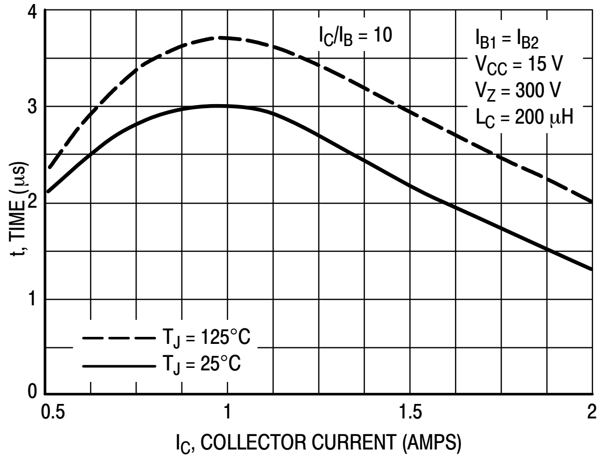


Figure 13 Bis. Inductive Storage Time, t$_{si}$

TYPICAL SWITCHING CHARACTERISTICS

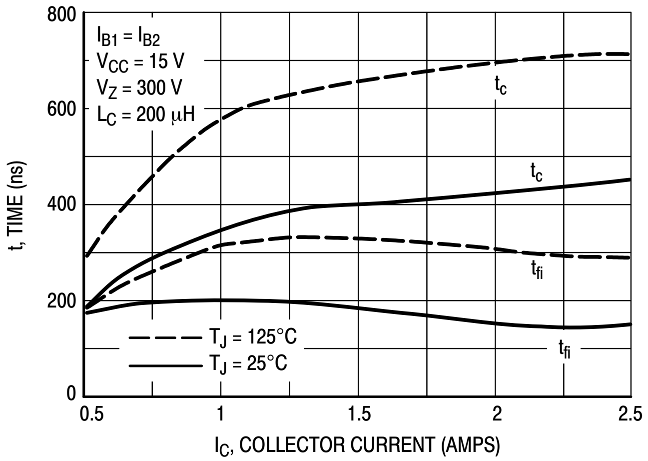


Figure 14. Inductive Storage Time, t_c & t_{fi} @ $I_C/I_B = 5$

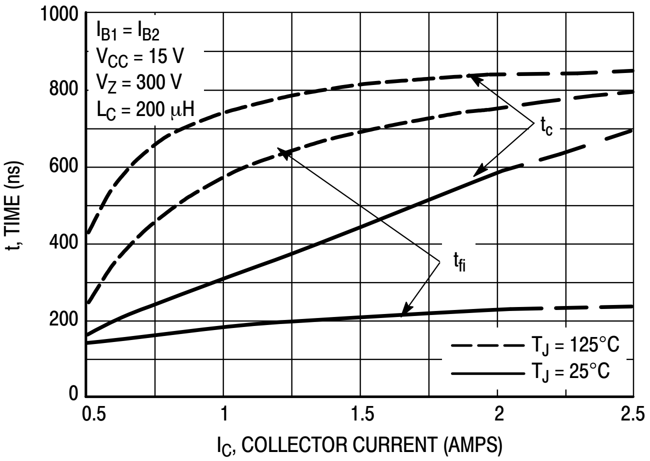


Figure 15. Inductive Storage Time, t_c & t_{fi} @ $I_C/I_B = 10$

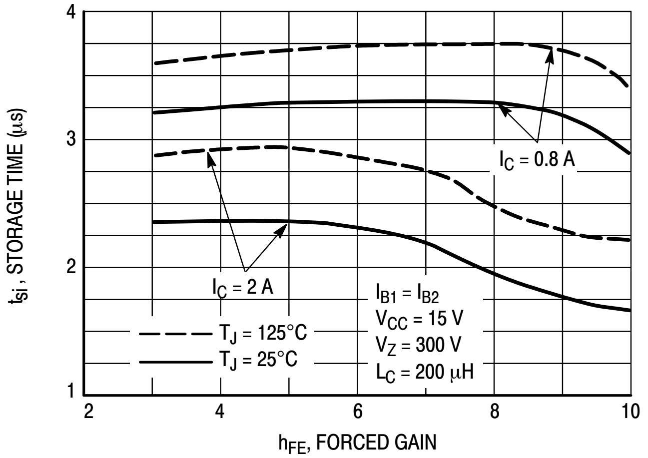


Figure 16. Inductive Storage Time

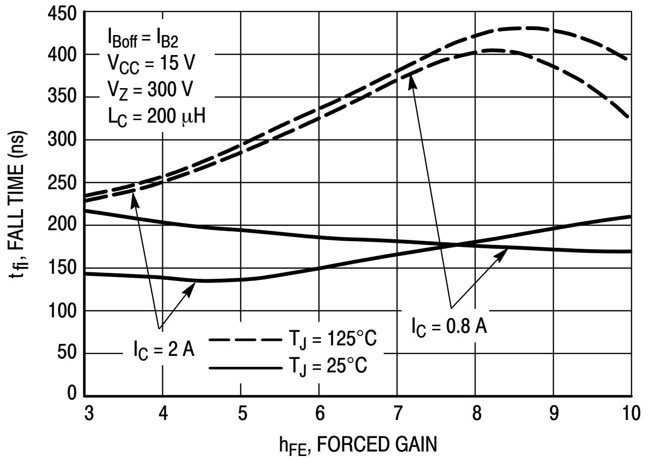


Figure 17. Inductive Fall Time

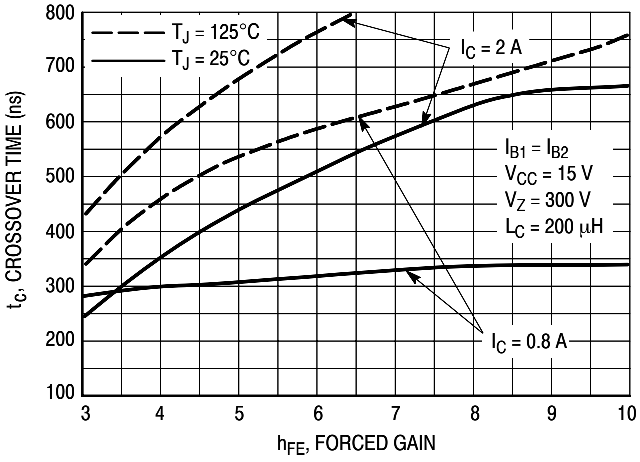


Figure 18. Inductive Crossover Time

TYPICAL SWITCHING CHARACTERISTICS

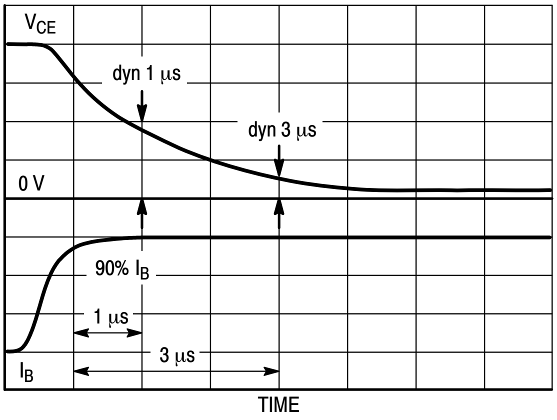


Figure 19. Dynamic Saturation Voltage Measurements

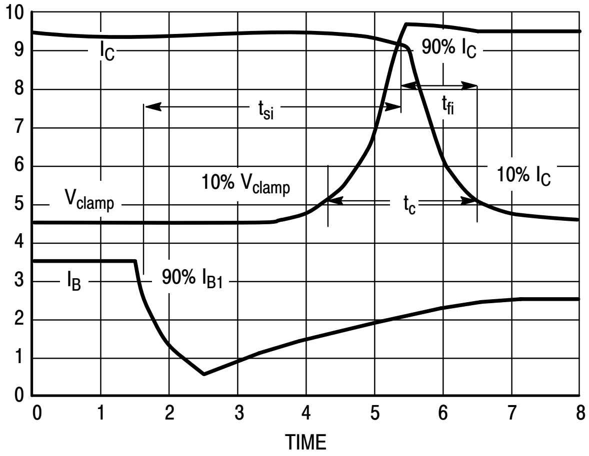
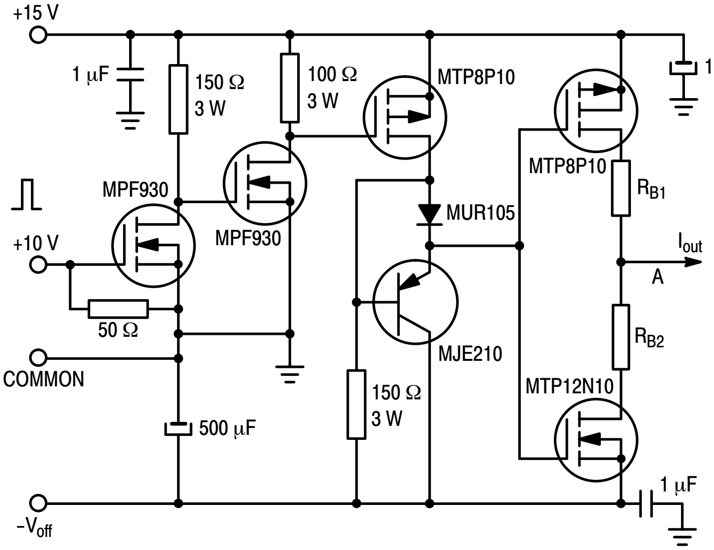
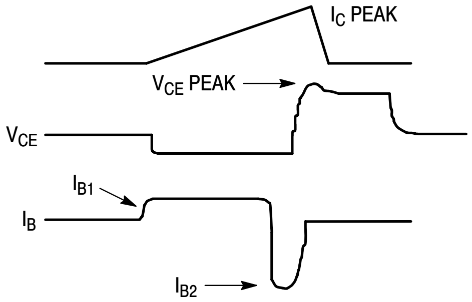


Figure 20. Inductive Switching Measurements

Table 1. Inductive Load Switching Drive Circuit





$V_{(BR)CEO(sus)}$	Inductive Switching	RBSOA
L = 10 mH	L = 200 μH	L = 500 μH
$R_{B2} = \infty$	$R_{B2} = 0$	$R_{B2} = 0$
V_{CC} = 20 Volts	V_{CC} = 15 Volts	V_{CC} = 15 Volts
$I_{C(pk)}$ = 100 mA	R_{B1} selected for desired I_{B1}	R_{B1} selected for desired I_{B1}

TYPICAL THERMAL RESPONSE

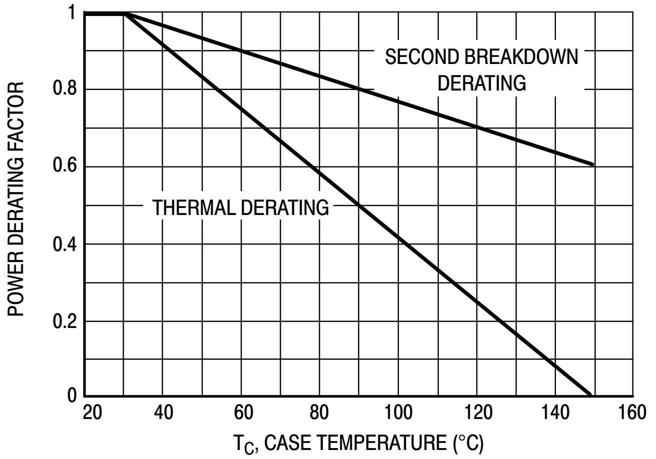


Figure 21. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 22 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C > 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 22 may be found at any case temperature by using the appropriate curve on Figure 21.

$T_{J(pk)}$ may be calculated from the data in Figure 24. At any case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn−off with the base to emitter junction reverse biased. The safe level is specified as a reverse biased safe operating area (Figure 23). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

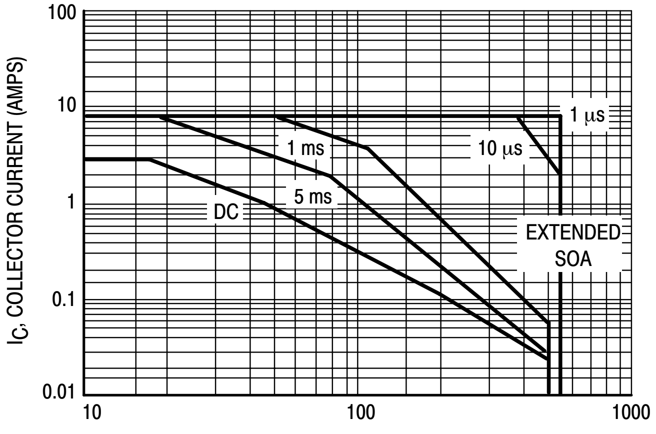


Figure 22. Forward Bias Safe Operating Area

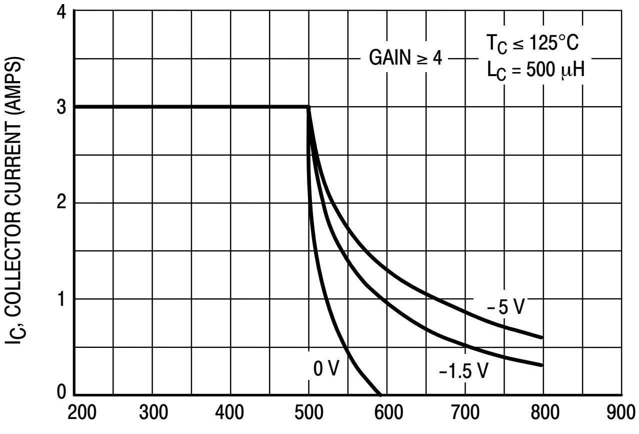


Figure 23. Reverse Bias Safe Operating Area

TYPICAL THERMAL RESPONSE

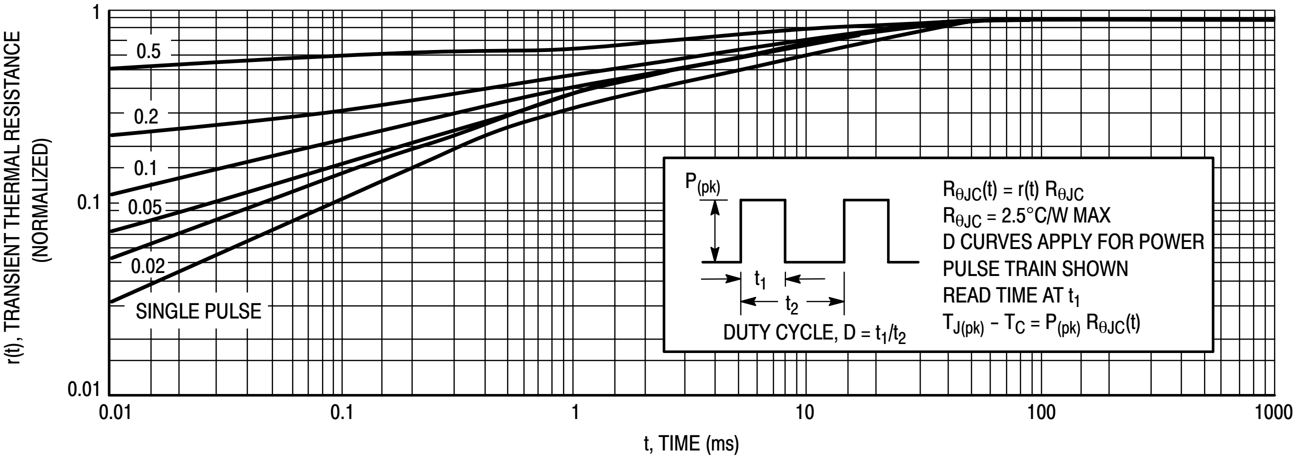
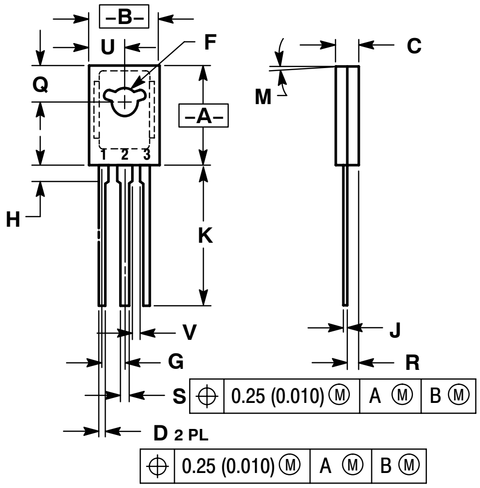


Figure 24. Typical Thermal Response ($Z_{\theta JC}(t)$) for BUH51

PACKAGE DIMENSIONS

TO−225
CASE 77−09
ISSUE Z



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 077−01 THRU −08 OBSOLETE, NEW STANDARD 077−09.

	INCHES		MILLIMETERS	
DIM	**MIN**	**MAX**	**MIN**	**MAX**
A	0.425	0.435	10.80	11.04
B	0.295	0.305	7.50	7.74
C	0.095	0.105	2.42	2.66
D	0.020	0.026	0.51	0.66
F	0.115	0.130	2.93	3.30
G	0.094 BSC		2.39 BSC	
H	0.050	0.095	1.27	2.41
J	0.015	0.025	0.39	0.63
K	0.575	0.655	14.61	16.63
M	5° TYP		5° TYP	
Q	0.148	0.158	3.76	4.01
R	0.045	0.065	1.15	1.65
S	0.025	0.035	0.64	0.88
U	0.145	0.155	3.69	3.93
V	0.040	---	1.02	---

STYLE 3:
PIN 1. BASE
2. COLLECTOR
3. EMITTER

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