NEC

BiCMOS INTEGRATED CIRCUIT

μPD3140GS

1.8 to 5.5 V BIAS, 80 MHz to 550 MHz DUAL PLL FREQUENCY SYNTHESIZER LSI FOR CORDLESS TELEPHONES AND PORTABLE CELLULAR RADIO

DESCRIPTION

μPD3140GS is a dual PLL frequency synthesizer LSI designed for cordless telephones and portable cellular radio. This LSI is manufactured using 13 GHz f_T BiCMOS process and integrated 2 pairs of prescaler + PLL operate from 80 MHz to 550 MHz. This LSI realizes low power consumption: on 1.8 V, 4.3 mA at dual operation and 2.7 mA at single operation. The additional functions are high-speed lockup and lock phase sensitivity setting. The package is a 20-pin SSOP (300 mil) suitable for high-density surface mounting. Thus, this product contributes to produce physically-small, low power-consumption, long-life battery systems.

FEATURES

- Supply voltage: V_{CC1} = V_{CC2} = 1.8 to 5.5 V
- Input operating frequency: f_{in} = 80 MHz to 550 MHz (PLL 1ch, 2ch in common)
- Reference oscillating frequency f_{ref} = 30 MHz MAX.. Built-in high-speed reference oscillator signal can be taken out from the buffer amplifier output pin.
- Built-in power-save function: control 2 prescaler's ON/OFF operation individually.
- Low power consumption: Dual operation (both ch ON): I_{CC} OP2 = 4.3 mA TYP. @ V_{CC} = 1.8 V
  Single operation (either ch ON): I_{CC} OP1 = 2.7 mA TYP. @ V_{CC} = 1.8 V
  Power save mode (both ch OFF): I_{CC} PS = 10 μA MAX. @ V_{CC} = 1.8 V
- Decreased lockup time available: charge pump switch control (lockup time: 9 ms @ f_{step} = 12.5 kHz, 1 MHz swing, decreased lockup time mode).
- Lock phase sensitivity programmable: Phase difference allowance for lock up can be controlled as 4 stages (150 ns to 5 μs).
- Pins and counter data are compatible to μPD2844BGS (except option data).
- High-density surface mounting: 20-pin plastic SSOP.

ORDERING INFORMATION

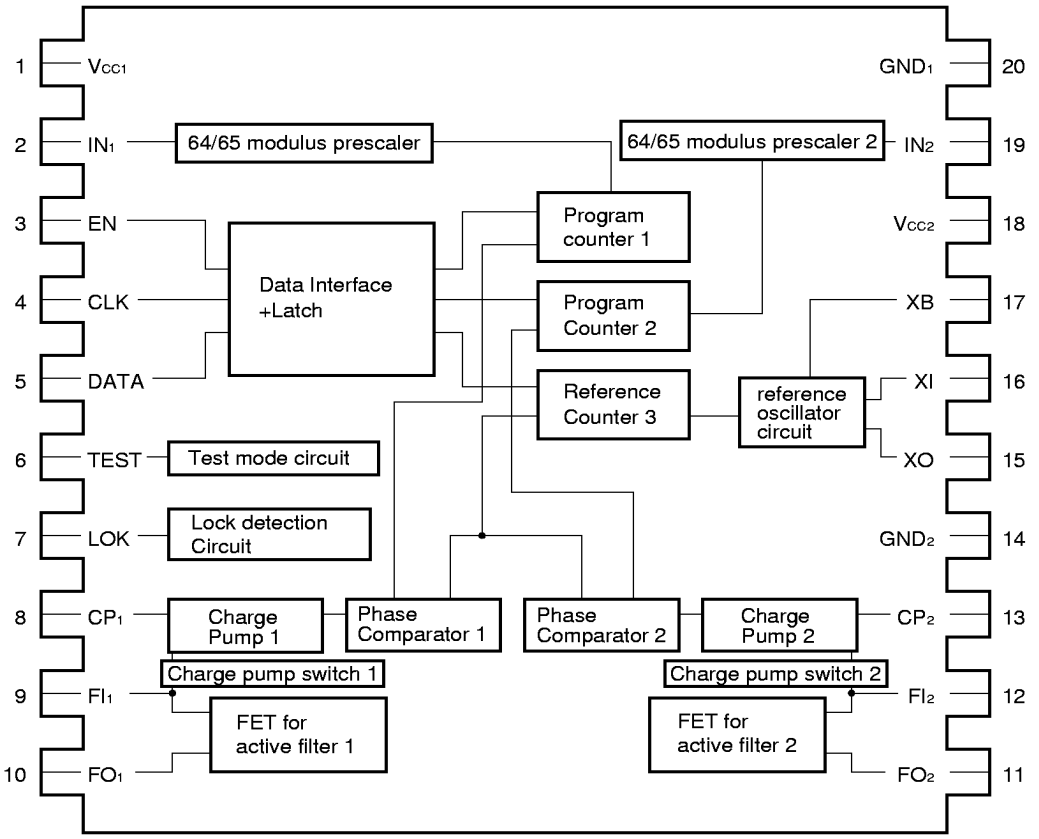
PARTS NUMBER	PACKAGE	SUPPLYING FORM
μPD3140GS-E1	20 pin plastic SSOP (300 mil)	Embossed tape 16 mm wide. QTY 2.5 k/reel Pin1 is in tape pull-out direction.
μPD3140GS-E2		Embossed tape 16 mm wide. QTY 2.5 k/reel Pin1 is in tape roll-in direction.
μPD3140GS-T1		Adhesive tape 32 mm wide. QTY 2 k/reel Pin1 is in tape pull-out direction.
μPD3140GS-T2		Adhesive tape 32 mm wide. QTY 2 k/reel Pin1 is in tape roll-in direction.

* To order evaluation sample, please contact your local NEC sales office (Order number : μPD3140GS).

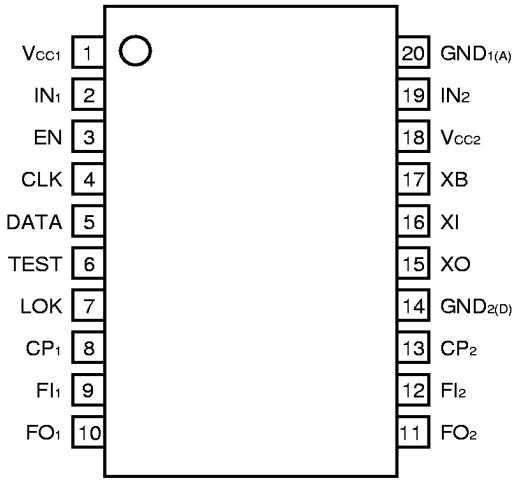
Caution: Electro-static sensitive device

Document No. P10957EJ2V0DS00 (2nd edition)
(Previous No. ID-3471)
Date Published April 1996 P
Printed in Japan

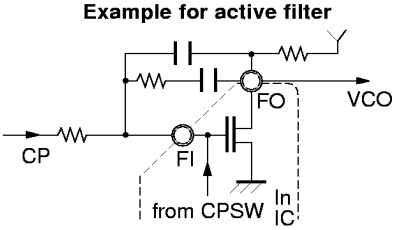
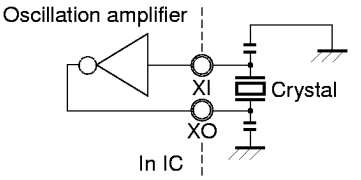
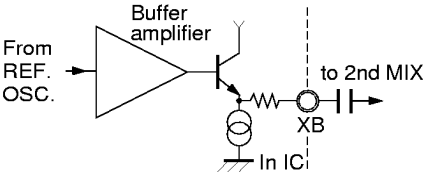
INTERNAL BLOCK DIAGRAM



PIN ASSIGNMENT (Top View)



PIN EXPLANATIONS

<table>
<tr><th>PIN No.</th><th>SYMBOL</th><th>EXPLANATIONS</th></tr>
<tr><td>1</td><td>V_{CC}</td><td>Supply voltage for analog block and 2 prescalers</td></tr>
<tr><td>2
19</td><td>IN_1
IN_2</td><td>Input for 64/65 modulus prescaler. This pin must be coupled with a capacitor (e.g. 1 000 pF).
IN_1: prescaler input for PLL1ch
IN_2: prescaler input for PLL2ch</td></tr>
<tr><td>3</td><td>EN</td><td>Load enable data input pin</td></tr>
<tr><td>4</td><td>CLK</td><td>Clock data input pin</td></tr>
<tr><td>5</td><td>DATA</td><td>Data input pin</td></tr>
<tr><td>6</td><td>TEST</td><td>Test pin (Refer to page 8). Used as PLL, this pin should be grounded.</td></tr>
<tr><td>7</td><td>LOK</td><td>Lock detecter output pin. This pin is designed as open drain.
Relation between operation mode and conditions to output is as follows.
<table>
<tr><th>OPERATE MODE</th><th>CONDITION TO OUTPUT LOCK</th><th>LOCK OUTPUT</th></tr>
<tr><td>SINGLE OPERATION</td><td>1 PLL LOCKED</td><td rowspan="2">LOW (SINK)</td></tr>
<tr><td>DUAL OPERATION</td><td>2 PLL LOCKED</td></tr>
</table>
(In other case, LOK pin output high as unlock.)</td></tr>
<tr><td>8
13</td><td>CP_1
CP_2</td><td>Charge pump output pin.
CP_1: Charge pump output from PLL1ch
CP_2: Charge pump output from PLL2ch</td></tr>
<tr><td>9
12</td><td>FI_1
FI_2</td><td>Gate input pin of active filter's FET
Also function as charge pump switch output pin.
FI_1: for PLL1ch
FI_2: for PLL2ch</td><td rowspan="2">Example for active filter
 
</td></tr>
<tr><td>10
11</td><td>FO_1
FO_2</td><td>Drain output of active filter's FET
FO_1: for PLL1ch
FO_2: for PLL2ch
In the case of passive filter, these pins should be opened.</td></tr>
<tr><td>14</td><td>GND_2</td><td>Ground pin of PLL digital block (PLL 1ch, 2ch in common)</td></tr>
<tr><td>15
16</td><td>XO
XI</td><td>Reference oscillator for both PLL
XO : output
XI : input
These pins should be externally equipped with crystal.
In the case of TCXO, input to XI pin through coupling capacitor (e.g. 1 000 pF).
V_{IN} = 0.2 V_{p-p} to 1.0 V_{p-p}, f_{max} = 30.0 MHz MAX.</td><td> 
</td></tr>
<tr><td>17</td><td>XB</td><td>Buffer output pin from reference oscillator</td><td> 
</td></tr>
<tr><td>18</td><td>V_{CC2}</td><td>Supply voltage for PLL digital block (PLL 1ch, PLL 2ch in common)</td></tr>
<tr><td>20</td><td>GND_1</td><td>Ground pin of analog block and 2 prescalers</td></tr>
</table>

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

Supply Voltage	V_{CC1}, V_{CC2}, V_{F0}	–0.3 to +6.0	V
Circuit Current	I_{CC}	40	mA
Operating Temperature	T_{opt}	–35 to +85	°C
Storage Temperature	T_{stg}	–40 to +125	°C

RECOMMENDED OPERATING RANGE

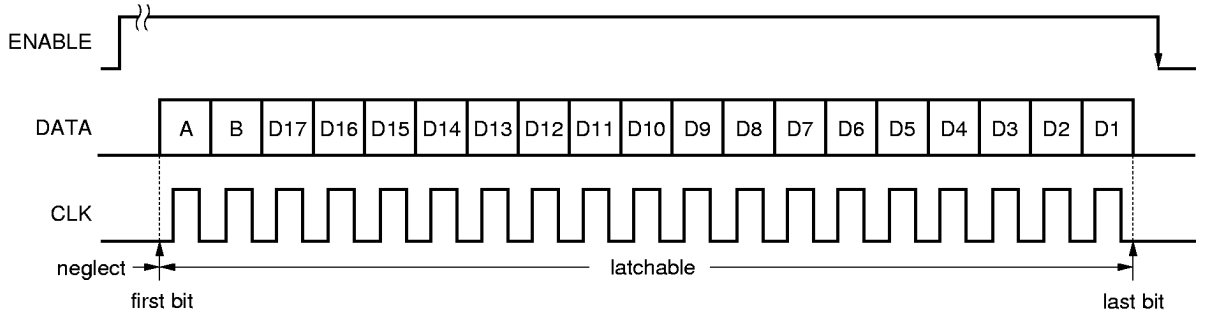
PARAMETER	SYMBOL	OPERATING RANGE	UNIT	Note
Supply Voltage	V_{CC1}, V_{CC2}, V_{F0}	1.8 to 2.0 to 5.5	V	V_{CC1} = V_{CC2}
Operating Temperature	T_{opt}	–35 to +25 to +85	°C	——

ELECTRICAL CHARACTERISTICS (Unless otherwise specified; V_{CC} = 1.8 to 5.5 V, T_A = –35 to +85 °C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Circuit Current 1 (OP1)	$I_{CC}OP1$		2.7	4.1	mA	V_{CC} = 1.8 V, +25 °C, total current of single operation
Circuit Current 2 (OP2)	$I_{CC}OP2$		4.3	6.6	mA	V_{CC} = 1.8 V, +25 °C, total current of dual operation
Circuit Current 3 (PS)	$I_{CC}PS$	–	0	10	μA	V_{CC} = 1.8 V, total current during power saving (both channels: off)
Circuit Current 1' (OP1')	$I_{CC}OP1'$		3.5	5.3	mA	V_{CC} = 5 V, +25 °C, total current of single operation
Circuit Current 2' (OP2')	$I_{CC}OP2'$		5.6	8.6	mA	V_{CC} = 5 V, +25 °C, total current of dual operation
High Level Input Voltage	V_H	V_{CC} × 0.7		V_{CC} + 0.5	V	EN, CLK, DATA pins
Low Level Input Voltage	V_L	–0.5		V_{CC} × 0.3	V	EN, CLK, DATA pins
Input Operating Frequency	f_{in}	200	–	550	MHz	V_{in} = –12 to 0 dBm, @ pins 2 and 19
		80	–	200		V_{in} = –8 to 0 dBm, @ pins 2 and 19 Note
Reference Frequency	f_{ref}	–	–	30	MHz	V_{in} = 0.2 to 1.0 V, @ pin 16
Crystal Oscillation Stability	X t stb	–4	–	+4	ppm	Application circuit: f_{ref} = 21.25 MHz , V_{CC1}, V_{CC2} constant
Crystal Oscillation Rise Time	X t frt	–	10	20	ms	Application circuit: f_{ref} = 21.25 MHz, ±4 ppm
Reference Oscillator Buffer Output Level	V xb		–3		dBm	Application circuit: f_{ref} = 21.25 MHz, R_L = 1 kΩ
Charge Pump and FI pin Leak Current	CP_{LEAK}	–20	0	20	nA	T_A = +25 °C, CP & FI pins, CP state: high impedance
Charge Pump Output Current 1	CPI_{000}		10		μA	V_{CC} = 2 V, CPH/L common, CP data: 000
Charge Pump Output Current 2	CPI_{001}		30		μA	V_{CC} = 2 V, CPH/L common, CP data: 001
Charge Pump Output Current 3	CPI_{010}		100		μA	V_{CC} = 2 V, CPH/L common, CP data: 010
Charge Pump Output Current 4	CPI_{100}		300		μA	V_{CC} = 2 V, CPH/L common, CP data: 100
Charge Pump Output Voltage	CPV_{111}	–	0.1		V	V_{CC} = 2 V, CP current = ±500 μA, CP data: 111
Phase difference allowance for lockup 1	$LOPW_{00}$		5.0		μs	V_{CC} = 2 V, LO data: 00
Phase difference allowance for lockup 2	$LOPW_{10}$		1.5		μs	V_{CC} = 2 V, LO data: 10
Phase difference allowance for lockup 3	$LOPW_{01}$		500		ns	V_{CC} = 2 V, LO data: 01
Phase difference allowance for lockup 4	$LOPW_{11}$		150		ns	V_{CC} = 2 V, LO data: 11
Clock Rate	Crate	1.0	–	–	μs	EN, CLK, DATA pins

Note: Refer to AC characteristic's Guaranteed operating range (page 12)

DATA FORMAT



Note: Data can be clocked in at falling edge of the CLK.
Latest 19 bits data before EN:H → L can be latched.

1. Relation between A, B data and setting data content

A	B	Setting data content
0	0	PLL 1ch (2 pin input) N counter data
0	1	PLL 2ch (19 pin input) N counter data
1	0	Option data
1	1	Reference counter data (PLL 1ch, 2ch common)

Remarks: Stable operation against same N counter data latched.

2. Counter data

- A, B = 0, 0 or 0, 1

PLL1ch, 2ch N counter Number : $N = D17 \times 2^{16} + D16 \times 2^{15} + D15 \times 2^{14} + D14 \times 2^{13} + D13 \times 2^{12} + D12 \times 2^{11} + D11 \times 2^{10} + D10 \times 2^{9} + D9 \times 2^{8} + D8 \times 2^{7} + D7 \times 2^{6} + D6 \times 2^{5} + D5 \times 2^{4} + D4 \times 2^{3} + D3 \times 2^{2} + D2 \times 2^{1} + D1 \times 2^{0}$

Note: Continuous setting range = 4 096 to 131 071 ('1' should be set to any of D13 to D17 data.)

- A, B = 1, 1

Reference Counter Number : $R = D11 \times 2^{11} + D10 \times 2^{10} + D9 \times 2^{9} + D8 \times 2^{8} + D7 \times 2^{7} + D6 \times 2^{6} + D5 \times 2^{5} + D4 \times 2^{4} + D3 \times 2^{3} + D2 \times 2^{2} + D1 \times 2^{1}$

Note: Setting range : 64 to 4 094 (Continuous even numbers can be set.)

3. Option settings (A, B = 1, 0)

<1> D1 to D6: Charge pump driving capability setting (CP data)

D3 (D6)	D2 (D5)	D1 (D4)	Charge pump driving capability		
			capability	Output Current	Output resistance Value
0	0	0	weak	10 μA	100 kΩ
0	0	1		30 μA	33 kΩ
0	1	0		100 μA	10 kΩ
0	1	1		130 μA	7.7 kΩ
1	0	0		300 μA	3.3 kΩ
1	0	1		330 μA	3 kΩ
1	1	0		400 μA	2.5 kΩ
1	1	1	strong	Voltage output	0.5 kΩ

1 Output resistance values are typical at V_{CC} = 2 V.
2 D1 to D3: PLL1ch data
D4 to D6: PLL2ch data

<2> D7: Charge pump polarity (PLL 1ch, 2ch common)

D7	Input phase status against reference signal phase			Filter Type
	phase advanced	phase delayed	Sychronized	
0	Low	High	High impedance	Passive filter
1	High	Low	High impedance	Active filter

<3> D8, D9: Prescaler ON/OFF control

D8	D9	PLL1ch	PLL2ch
0	0	OFF	OFF
0	1	OFF	ON
1	0	ON	OFF
1	1	ON	ON

<4> D11, 12: Lock phase sensitivity setting (PLL1 ch, 2 ch in common)

D11	D12	Lock Phase sensitivity
0	0	5.0 μs
1	0	1.5 μs
0	1	500 ns
1	1	150 ns

* Phase difference allowance for lock up, Input signal phase against reference signal phase.

<5> D10: Charge pump voltage/current output automatic control mode (PLL1ch, 2ch in common)

D10	CP data D1 to D3	Lock condition	PLL 1ch
0	except 111	UNLOCK	Current Output
		LOCK	
1	except 111	UNLOCK	Voltage Output
		LOCK	Current Output

* CP data D4 to D6 : PLL 2ch

Recommendable Application of CP V/I output control mode

1. External loop filter should be designed as minimum lock-up time at D1-D3, D4-D6 = (111).
2. Desired C/N and loop cut-off frequency should be optimized with chosen CP current data 000 to 110. This mode is called 'fixed frequency mode'.
3. On D10 = 1 setting, lock up mode and fixed frequency mode can be switched automatically.

<6> D13 to D17: Charge pump switch control (decreased lock up time) mode: PLL 1ch, PLL 2ch in common

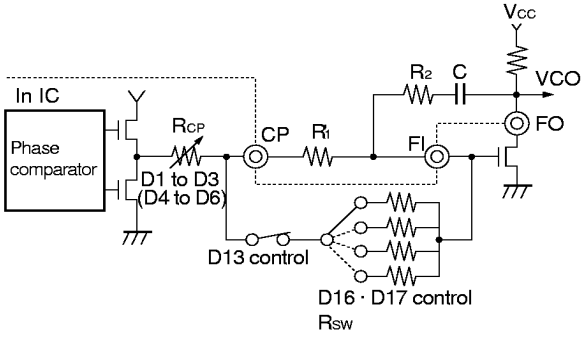
• D13: charge pump switch control

D10	D13	CPSW
1	1	ON *1
	0	OFF*2
0	1	OFF*2
	0	

*1 Output route can be controlled as 'CPSWout (FIpin) → CPout'.

*2 CPout only

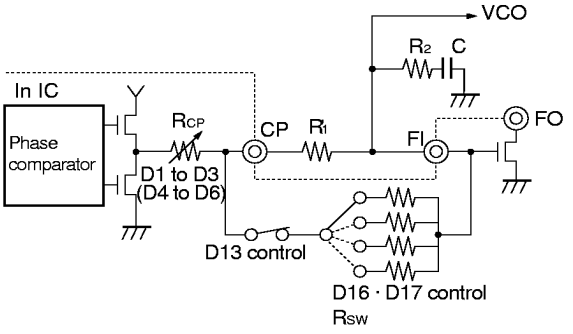
Active filter



D14	D15	CPSW out polarity reverse time
0	0	1 time
0	1	2 times
1	0	4 times
1	1	8 times

After CPSW out polarity reverse time, output route will be switched from FI pin to CP pin.

Passive filter (lag lead)



D16	D17	CPSW resistance: RSW (MOS: ON resistance)
0	0	150 Ω
0	1	500 Ω
1	0	1.5 kΩ
1	1	5.0 kΩ

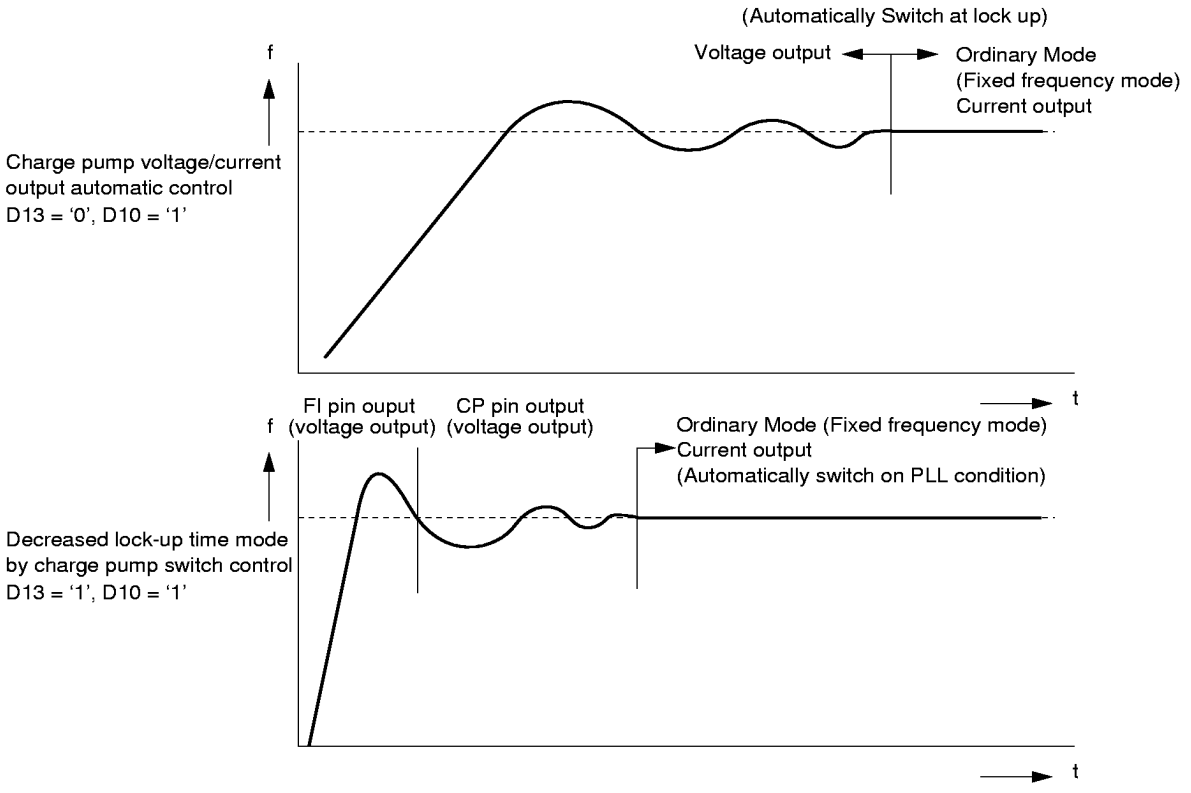
Recommendable Application of decreased lock up time by CPSW control mode

This mode can realize faster lock up than CP V/I output control mode.

- For sweep to adjacent frequency, CP V/I output control mode should be used.
- For rise-up from power save mode, decreased lock up time mode should be used.
- Charge pump switch resistance should be chosen at (D10, D13) = (1, 1), (D14, D15) = (0, 0).
- After charge pump switch resistance is fixed, polarity reverse time should be chosen.

Note: On passive filter application, FI pin should be used as a charge pump switch output pin.

SCHEMATICS FOR LOCKUP MOVEMENT



NOTICE FOR DESIGNING LOOP FILTER

For automatic switching on decreased lock up time mode, loop filter should be designed to suppress fluctuation of the loop gain among three modes. For example, the CP-FI resistor (R'_1) may be determined as 10 kΩ to 30 kΩ.

TEST MODE SETTING

1. Test mode can be set at (V_{CC2} – other bias) ≥ 1.5 V
   For example, other bias = 2 V, V_{CC2} = 3.5 V.
2. Test mode gives us operation monitoring of each block as follows:

<1> Test mode 1

- PLL 1ch's prescaler – Output frequency of IN_1 input/65 can be monitored at TEST pin.

<2> Test mode 2

- PLL 2ch's prescaler – Output frequency of IN_2 input/65 can be monitored at TEST pin.

<3> Test mode 3

- This test mode can make PLL Lock and following operation monitor.
  - Charge pump circuit - Enforced high impedance outputs from CP pin to measure the leakage.
  - Charge pump switch circuit - When 16 or more signals are input to the CLK pin, the Charge pump switch (FI pin) changes from ON to OFF (open).

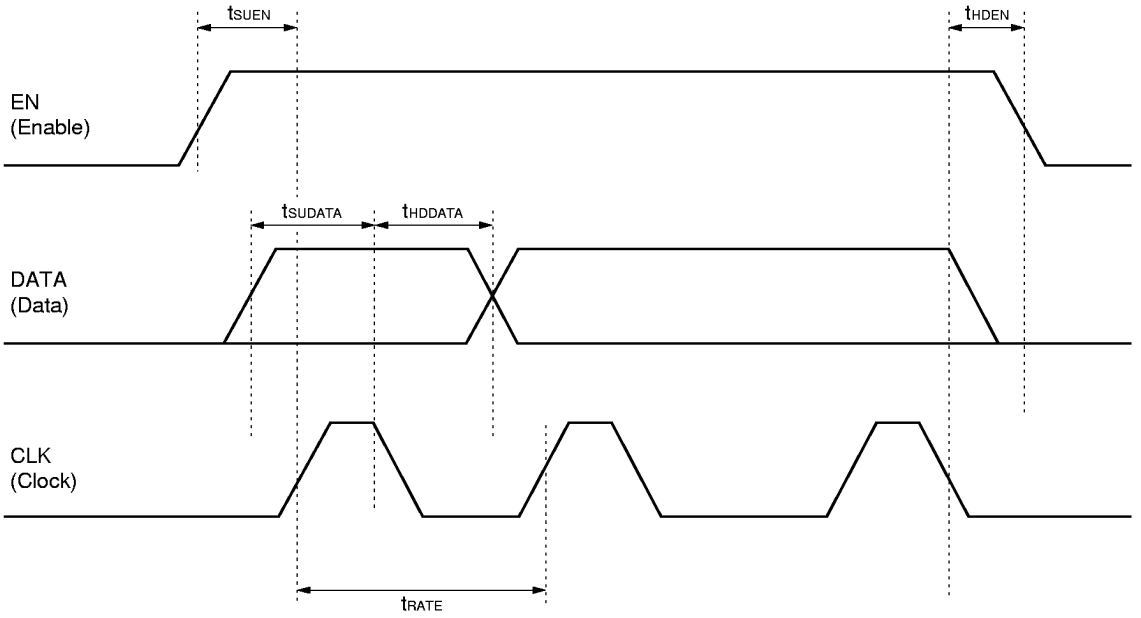
CLK pin input count signal	CPSW (FI pin)	LOK pin
16 or over	OFF (open)	Low
less than 16	ON	High

  - Lock detection circuit - When 16 or more signals are input to the CLK pin, the lock pin turns ON (L).

TEST MODES SETTING TABLE

Block name	Test mode condition setting			CLK pin	TEST pin	Other monitor pin
	Setting mode	EN pin	DATA pin			
PLL 1 ch's prescaler	Test Mode 1	H	L	–	IN_1/65	–
PLL 2 ch's prescaler	Test Mode 2	L	H	–	IN_2/65	–
Change pump circuit	Test Mode 3	H	H	–	–	CP pin: High impedance output
Charge pump switch circuit	Test Mode 3	H	H	16 count signal	–	Switch control between CP and FI pins
Lock detection circuit	Test Mode 3	H	H	16 count signal	–	LOK pin : Low at Lock up

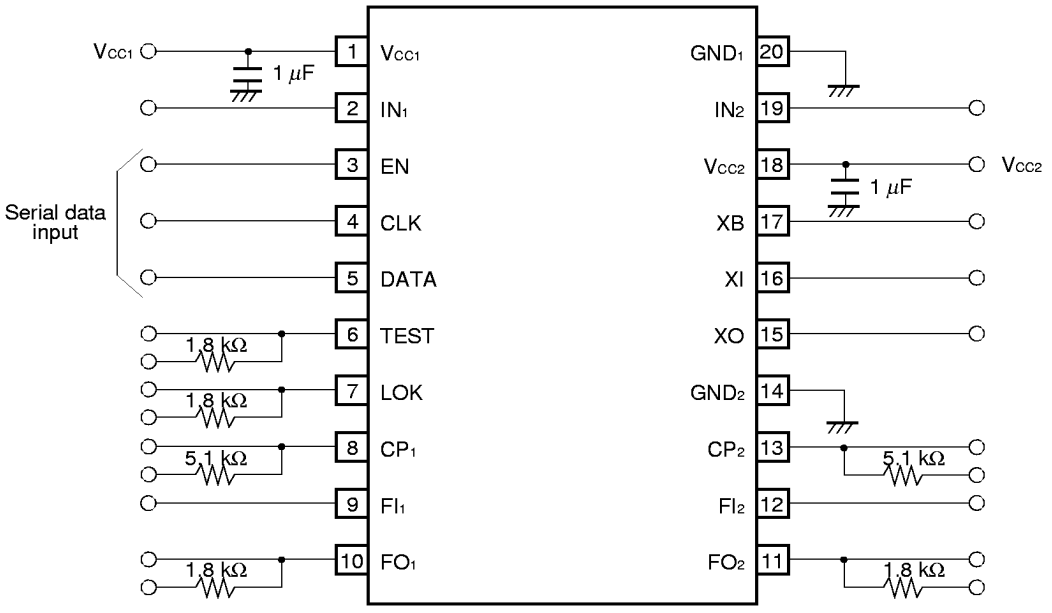
SERIAL DATA INPUT TIMING



Parameter	Specification
EN set up time	$t_{SUEN} \geq 500$ ns
EN hold time	$t_{HDEN} \geq 500$ ns
DATA set up time	$t_{SUDATA} \geq 100$ ns
DATA hold time	$t_{HDDATA} \geq 100$ ns
CLK rate	1 μs $\leq t_{RATE} \leq$ 1 s

TEST CIRCUIT

1. DC measurement circuit

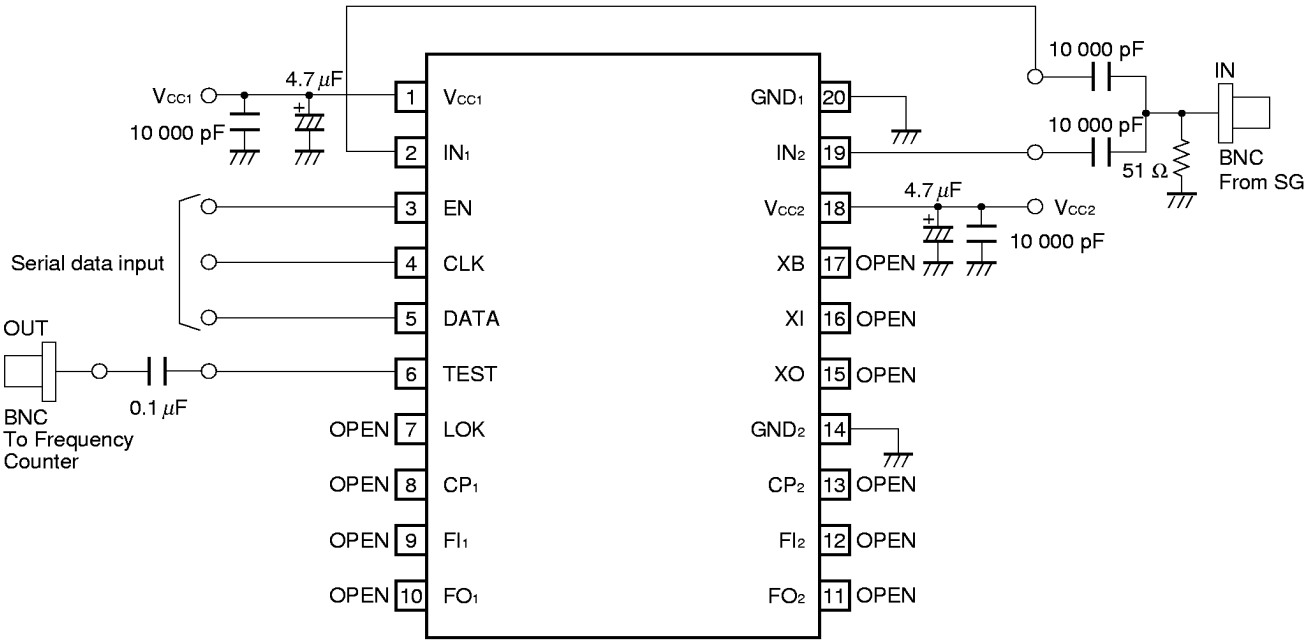


Supply current measurement flow

1. Supply power (V_{CC1}, V_{CC2} ON). Except for V_{CC1}, V_{CC2}, GND_1, GND_2, EN, CLK and DATA pins should be opened.
2. Serial data input to 3, 4, and 5 pin. Prescaler operation should be set with option data D8 and D9.
3. Measure the supply current of V_{CC1} and V_{CC2}.

ATTENTION Serial data must be input for correct measurement. If you did not input serial data, measurement would be failed and show undesired value.

2. AC measurement circuit



Input response of internal prescaler measurement flow.

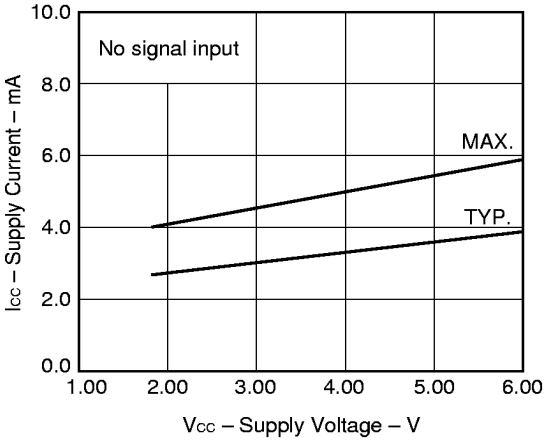
1. Supply power (V_{CC1}, V_{CC2} ON).
2. Serial data input to 3, 4, and 5 pin.
   [Command as dual operation with option data D8 and D9.]
3. Set TEST mode.
   $V_{CC2} = V_{CC1} + 2$ (Other bias = V_{CC1})
4. The 1ch (IN1) or 2ch (IN2) prescaler output can be monitored at TEST pin. (See the table below.)

EN (3 pin) input	DATA (5 pin) input	TEST (6 pin)
H	L	1ch prescaler output
L	H	2ch prescaler output

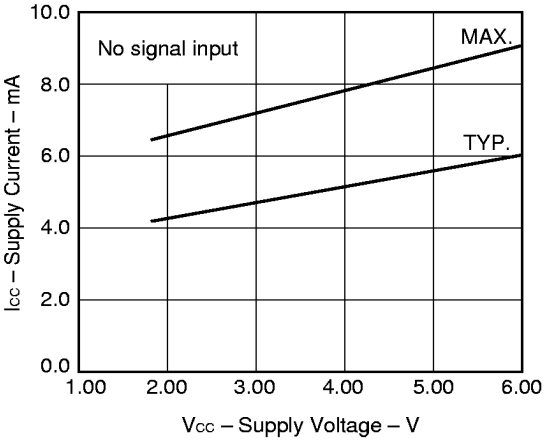
CHARACTERISTICS CURVES (T_A = +25 °C unless otherwise specified)

DC chracteristics

SUPPLY VOLTAGE vs. SUPPLY CURRENT at SINGLE OPERATION

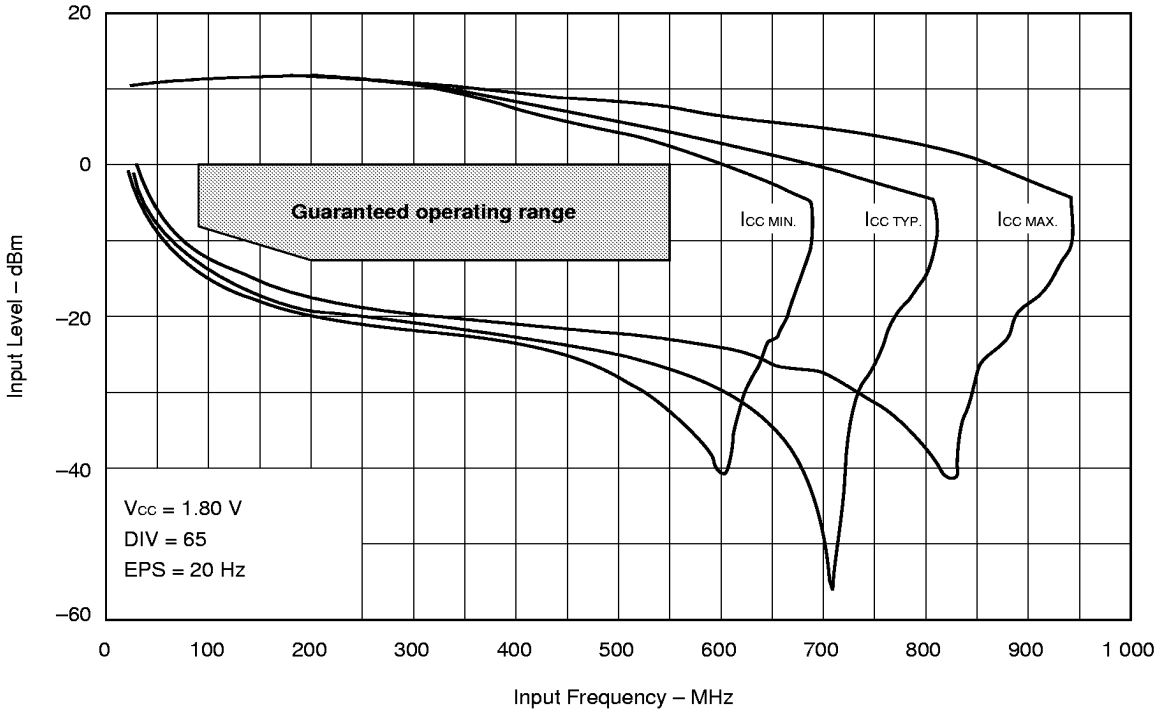


SUPPLY VOLTAGE vs. SUPPLY CURRENT at DUAL OPERATION

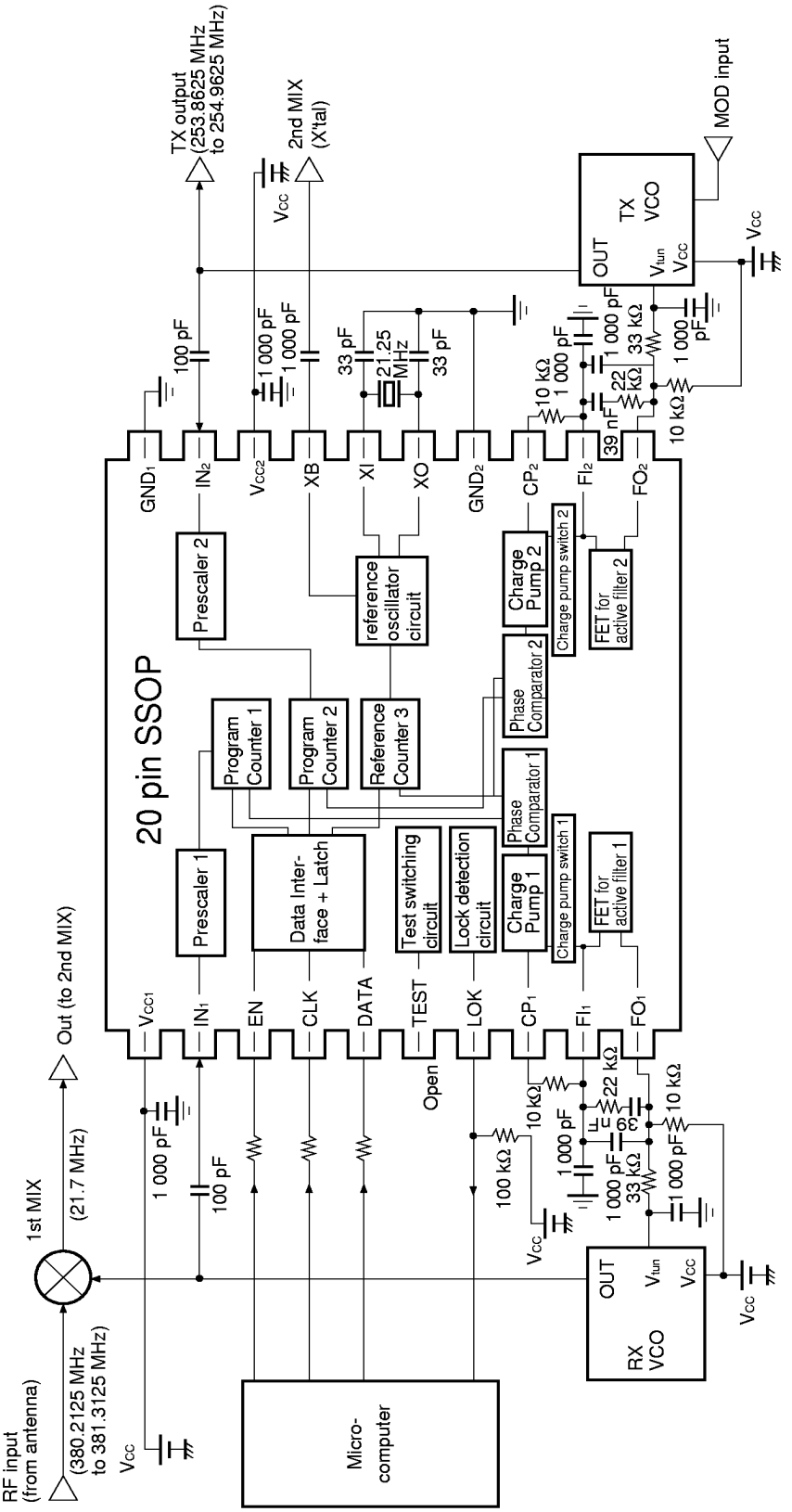


AC characteristics

INPUT RESPONSE OF INTERNAL PRESCALER (PLL1ch, 2ch in common)



APPLICATION CIRCUIT EXAMPLE (Example for hand-held set of analog cordless phone)



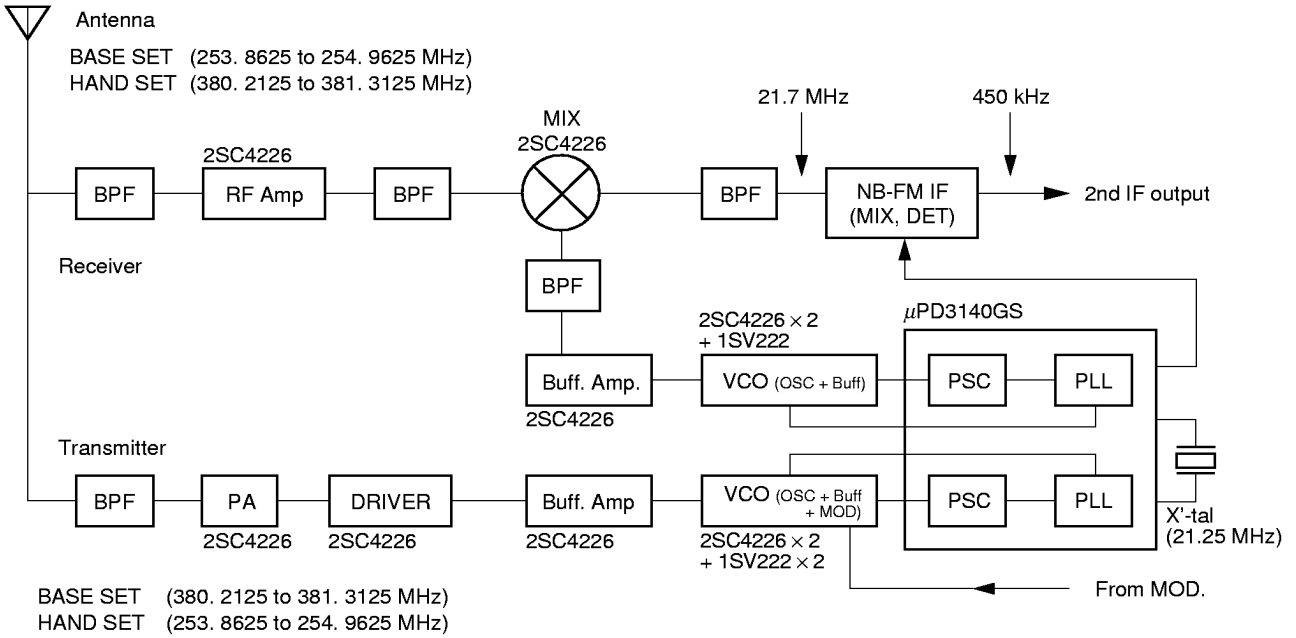
The application circuits and their parameters are for references only and are not intended for use in actual design-in's.

SELECTOR GUIDE OF DUAL PLL FREQUENCY SYNTHESIZER LSI FAMILY FOR CORDLESS TELEPHONE

Item \ IC number		μPD2840GS	μPD2842GS	μPD2843GS	μPD2844BGS	μPD2844BGS(1)	μPD3140GS
Reference counter number		Fixed (1 024)		Variable (2 to 4 096)	Variable (4 to 8 192) **Note**: Even number only.		Variable (64 to 4 094) **Note**: Even number only.
Charge pump output mode		Current output type (Fixed)		Current Output type (Programmable)			Current output Voltage output (Programmable)
Charge pump output phase polarity	Advanced	HIGH	LOW	Polarity can be switched. (Programmable)			
	Delayed	LOW	HIGH				
	Synchronized	High impedance					
External low-pass filter type		• Passive main		• Active • Passive			
Low-pass filter FET (for active filter)		None (External)		Equipped			
Reference oscillator buffer output		None (external if necessary)					Equipped
High-speed lockup charge pump switch		None					Equipped
Lock sensitivity data setting		None (Fixed at 500 ns)					Programmable (4 stages)
Data reset latch type		Yes					No. Stable operation against same N counter data latched.
Supply voltage		2.2 to 5.5 V				2.0 to 5.5 V	1.8 to 5.5 V
Package		20 pin SOP (300 mil)			20 pin SSOP (300 mil)		

μPD3140GS is recommendable due to the most excellent performance.

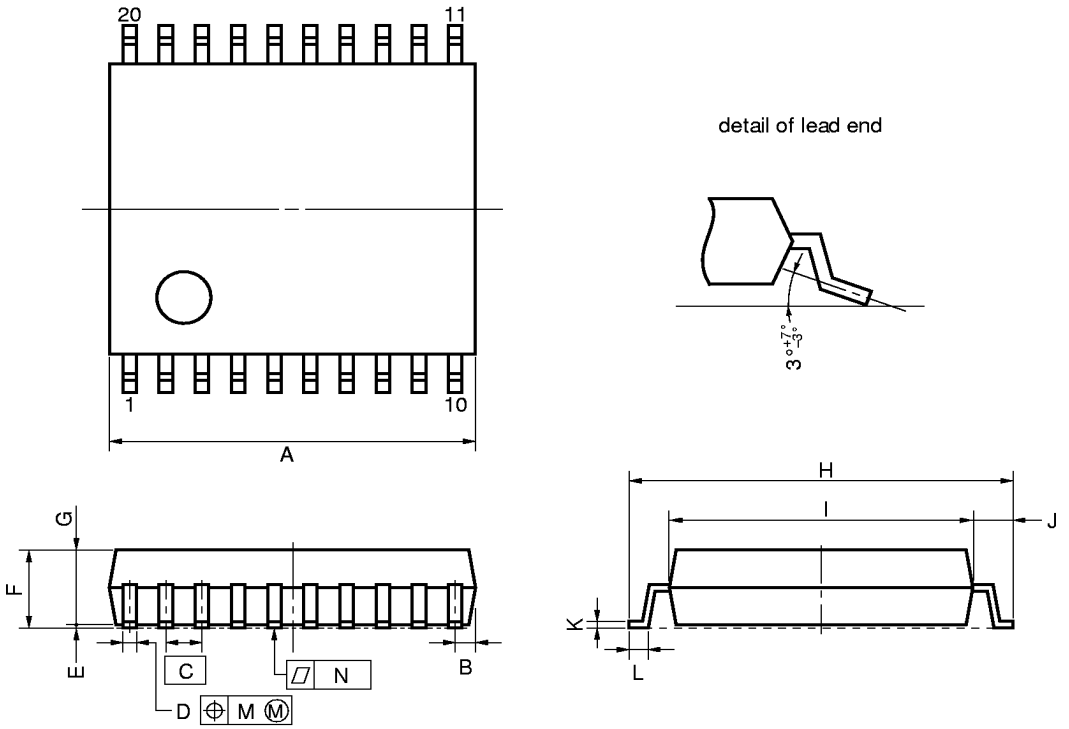
SCHEMATIC BLOCK DIAGRAM FOR 200 MHz to 400 MHz WIRELESS SYSTEM (Example of Japanese analog cordless telephone)



APPLICATION SYSTEM EXAMPLES

- Japanese analog cordless telephone
- Low-power transceiver
- VHF band radio communication system
- RF remote controller
- CT1/CT2 cordless telephone (doubler type)
- PHS/DECT digital cordless telephone (for 2nd PLL)
- Analog/digital cellular (for 2nd PLL)

20 PIN PLASTIC SHRINK SOP (300 mil) (Unit : mm)



P20GM-65-300B-2

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	7.00 MAX.	0.276 MAX.
B	0.575 MAX.	0.023 MAX.
C	0.65 (T.P.)	0.026 (T.P.)
D	0.30±0.10	$0.012^{+0.004}_{-0.005}$
E	0.125±0.075	0.005±0.003
F	2.0 MAX.	0.079 MAX.
G	1.7	0.067
H	8.1±0.3	0.319±0.012
I	6.1±0.2	0.240±0.008
J	1.0±0.2	$0.039^{+0.009}_{-0.008}$
K	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.002}$
L	0.5±0.2	$0.020^{+0.008}_{-0.009}$
M	0.12	0.005
N	0.10	0.004

RECOMMENDED SOLDERING CONDITIONS

This product should be soldered in the following recommended conditions. Other soldering methods and conditions than the recommended conditions are to be consulted with our sales representatives.

μPD3140GS

Soldering method	Soldering conditions	Symbol
Infrared ray reflow	Package peak temperature: 235 °C, Hour: within 30 s. (more than 210 °C), Time: 2 times, Limited days: no. *	IR35-00-2
VPS	Package peak temperature: 215 °C, Hour: within 40 s. (more than 200 °C), Time: 2 times, Limited days: no. *	VP15-00-2
Pin part heating	Pin area temperature: less than 300 °C, Hour: within 3 s./pin. Limited days: no. *	

*: It is the storage days after opening a dry pack, the storage conditions are 25 °C, less than 65 % RH.

Note 1. Apply only a single process at once (except the pin part heating method.)

For details of recommended soldering conditions for surface mounting, refer to information document SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL (C10535EJ7V0IF00)

NOTE ON CORRECT USE

(1) Observe precautions for handling because of electrostatic sensitive devices.

(2) Connect a bypass capacitor (e.g. 1 000 pF) to the V_{CC} pin.

(3) External R, C values of loop filter should be determined according to the VCO specifications.

(4) Form a ground pattern as wide as possible to minimize ground impedance.

(5) After initial V_{CC} supplying, serial data should be input immediately. (Before serial data input, LSI operation is unstable or undesired.)

For details of application circuit example and setting data, refer to application note 'USAGE AND APPLICATION OF μPD3140GS'.