CLA80000 Series
High Density CMOS Gate Arrays

ZARLINK™
SEMICONDUCTOR

INTRODUCTION

The CLA80k gate array series from Zarlink Semiconductor offers advantages in speed and density over previous array series. Improvements in design combined with advances in simulation accuracy allow the implementation of complex systems in excess of 260,000 gates.

FEATURES

- 0.7μ (0.8μ drawn) process
- Typical gate delay 210ps
- Accurate simulation delay (multi platform support)
- Support for industry standard workstations
- Comprehensive cell library
- 3V option for low power operation
- Split rail operation (optional 5V I/O, 3V core logic)
- Low skew clock distribution strategy
- Power and ground distribution grids
- Extensive range of package options

OVERVIEW

The gate array has a comprehensive cell library including RAM generators as well as JTAG circuits. CLA80k is Zarlink Semiconductor's seventh generation CMOS gate array product. The family consists of 22 arrays implemented on a proven 0.7μm (0.8μm drawn) process which offers two or three layer metal.

Zarlink Semiconductor's Design Centres offer support on a variety of design routes customized to individual requirements.

Zarlink supplies design kits for the major industry standard ASIC design tools and all kits support advanced nonlinear delay calculations essential for accurate simulation.

Standard Density Pad Arrays are targeted for use in ceramic packaging and for those applications which require assembly in conformance with MIL STD 883.

ARRAY SIZES

The CLA80k series comprises 9 base arrays and 22 variants ranging from 2816 to 513,136 array elements. The optimum array for your requirement may be selected from the tables below.

Double Layer Metal Arrays (High Density Pads)

Array type	Array elements	Usable gates	Total Pads
CLA81XXX	2816	1400	64
CLA82XXX	8736	4260	88
CLA83XXX	17920	8400	112
CLA84XXX	30784	13600	136
CLA85XXX	54720	22000	168
CLA86XXX	100048	30000	216
CLA87XXX	157872	48000	264

Triple Layer Metal Arrays (High Density Pads)

Array type	Array elements	Usable gates	Total pads
CLT81XXX	2816	1680	64
CLT82XXX	8736	5200	88
CLT83XXX	17920	10700	112
CLT84XXX	30784	18000	136
CLT85XXX	54720	32500	168
CLT86XXX	100048	58000	216
CLT87XXX	157872	90000	264
CLT88XXX	307568	170000	360
CLT89XXX	513136	260000	456

Standard Density Pad Arrays

Array type	Array elements	Usable gates	Total pads
MLA85XXX	54720	22000	144
MLT85XXX	54720	32500	144
MLA87XXX	157872	48000	232
MLT87XXX	157872	90000	232
MLT88XXX	307568	170000	312
MLT89XXX	513136	260000	384

ARCHITECTURE

Core cell

■ Optimized structure for a variety of logic elements

■ Allows routing through cells for compact layout

The basic unit from which all library functions are constructed is called an 'array element'. An array element consists of two P-channel and two N-channel plus a small P-channel transistor. Two basic cell or array elements are illustrated in Figure 1. To achieve the required circuit function, logic designers use a set of cells. Each library component realizes a logic function, ranging in complexity from an inverter to a master-slave 'D' flip-flop. A fixed metal interconnection of the transistors from one or more array elements implements the cell function. A design is specified in terms of cells, macros, modules and their interconnections, which are then simulated using one of the many supported design platforms.

If a design uses only two layers of metal then a set of four masks is required. One for contacts, one for vias (connections between the metal layers) and two for metals. If a design uses three layer metal then six masks are required. One for contacts, two for vias and three for metals.

I/O ARRANGEMENT

■ High density and standard density pads available

■ 4KV ESD and latchup immunity

■ Programmable slew rate control

Around the outside of the array are I/O blocks and pads placed at the chip periphery. All arrays have wide power bus rings situated over the I/O blocks. The partition of the I/O cell is shown in Figure 2. For high density pad arrays three pads are placed every four I/O cells whilst for standard density array pads two pads are placed for every three I/O cells.

Each I/O cell is divided into a number of sections allowing a wide variety of different I/O cells to be constructed. Each I/O block can be customized as an input, output or bi-directional I/O port. In addition any pad location can be used as a positive or negative supply pad.

Electrostatic discharge protection (ESD) is built into the I/O cells. This protection can withstand in excess of 4kV. The structure is also highly resistant to latch-up due to the epitaxial substrate used in the process.

Slew rate control is provided within the I/O cell structure to minimize supply noise transients. This is a useful feature in larger designs where multiple high drive outputs need to be switched simultaneously.
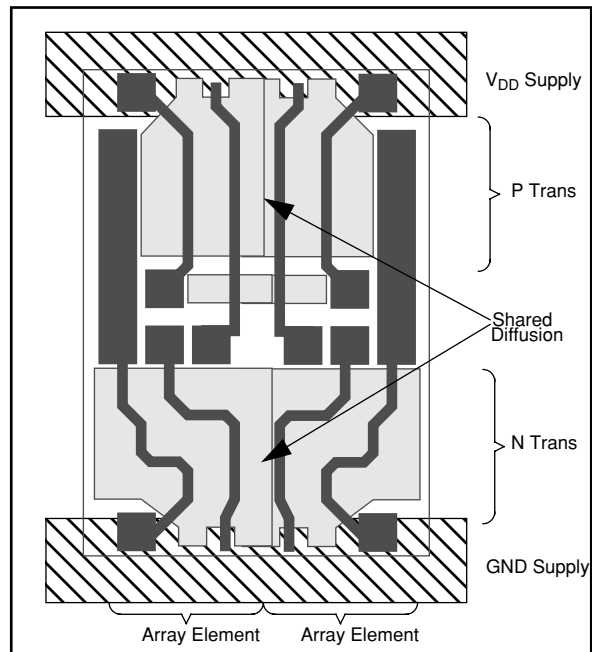

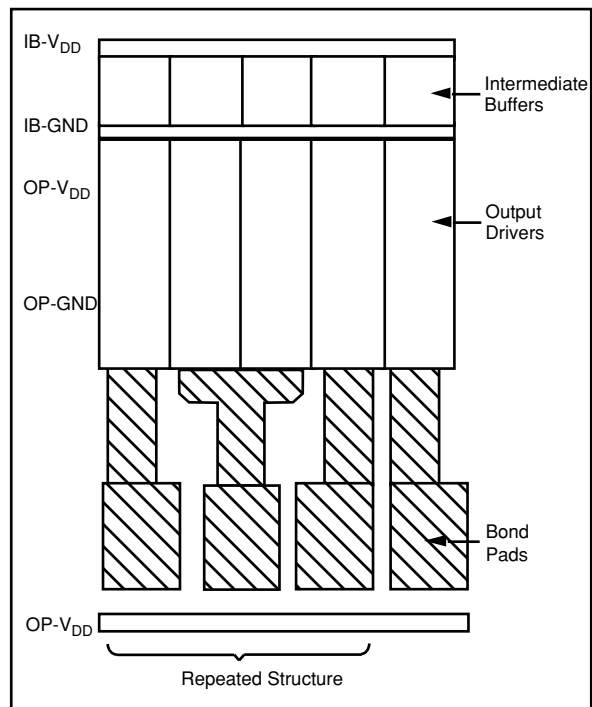Figure 1 Pair of array elements

Figure 2 High density pad spacing

CLOCK AND POWER DISTRIBUTION

■ Low skew clock distribution strategy

■ Power grid to minimize voltage drop

In large complex designs working at high speed, on chip clock and power distribution is vital to successful operation of the design. Zarlink has a number of techniques to minimize potential problems which can occur with clocking and powering the chip.

Clock Distribution

The clock distribution network must ensure that skew is minimized and that long term failure does not occur due to metal migration. Three solutions available from ZarlinkZarlink are:

Large buffer

Balanced Tree

Clock Grid

Distributed clock buffer cells are supported for the CLA80k family to minimise clock skew effects across a die. The use of these cells is restricted to three layer metal designs. Each array size from CLT84 upwards has its own unique buffer cell (CLKB8*).   Each of the cells occupy one I/O block but with the output drive distributed across the die. The clock signal is routed at layout either as a grid, ring or spine structure to maintain clock skew within acceptable limits. These clock buffer cells are entered in the circuit schematic at the top level of the and all registers and latches should be driven directly from the clock buffer output.

Power Distribution

The power distribution metal in the array must be designed to avoid excessive voltage drops and long term failure due to electromigration.

Metal 1 V_{DD} and V_{SS} tracks pass through all the array cells. At regular intervals across the array the metal 1 supply rails are fed by vertical metal 2 straps. For designs using three layers of metal additional straps can be added in metal 3. Fig 4 shows a representation of the grid arrangement.

MANUFACTURING

■ Computer aided manufacturing

■ Class 10 or better clean room conditions

■ Vibration free for reliable manufacture

The CLA80k product is manufactured near Plymouth England in a purpose built factory for sub-micron process geometry. The factory uses the latest automated equipment for 6-inch wafers in vibration free class 10 clean room conditions. Computer Aided Manufacture in the above environment ensures production efficiency and the lowest possible defect level. In addition to the world class wafer facility there are excellent probe and final test areas equipped with the latest analog and digital testers.

This continued investment demonstrates Zarlink Semiconductor's commitment to providing state-of-the-art CMOS ASICS.
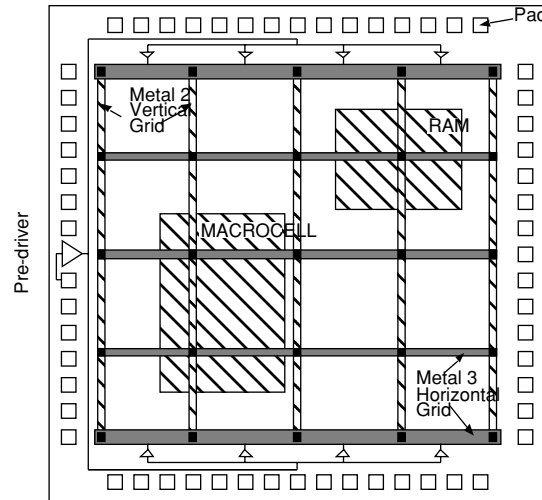

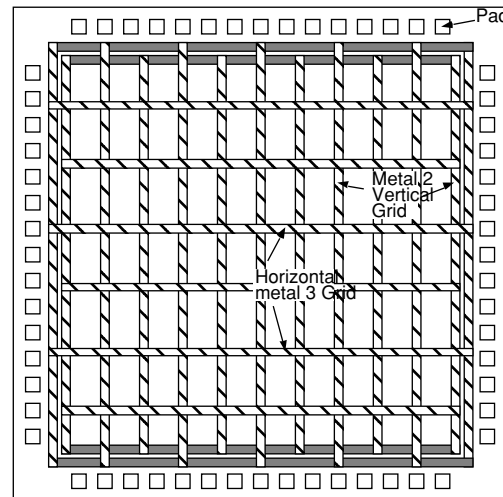Figure 3 Example of distributed clock buffer using a grid structure

Figure 4 Example of three layer metal power grid

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CELL LIBRARY

■ Comprehensive range of cells

■ JTAG and Paracell libraries

A comprehensive cell library is available for the CLA80k series. It contains libraries that may be used in specific applications areas such JTAG boundary scan.

Buffers and Inverters

BUFX3	Non-inverting driver with x3 drive
BUFX7	Non-inverting driver with x7 drive
DELAY	Timing delay
INVX1	Inverter
INVX2	Inverter with x2 drive
INVX4	Inverter with x4 drive
INVX6	Inverter with x6 drive
INVX8	Inverter with x8 drive

NAND Gates

NAND2	2 input NAND gate
NAND2X2	2 input NAND gate with x2 drive
NAND3	3 input NAND gate
NAND3X2	3 input NAND gate with x2 drive
NAND4	4 input NAND gate
NAND4X2	4 input NAND gate with x2 drive

NOR Gates

NOR2	2 input NOR gate
NOR2X2	2 input NOR gate with x2 drive
NOR3	3 input NOR gate
NOR3X2	3 input NOR gate with x2 drive
NOR4	4 input NOR gate
NOR4X2	4 input NOR gate with x2 drive

AND Gates

AND2	2 input AND gate
AND2X2	2 input AND gate with x2 drive
AND3	3 input AND gate
AND3X2	3 input AND gate with x2 drive
AND4	4 input AND gate

OR Gates

OR2	2 input OR gate
OR2X2	2 input OR gate with x2 drive
OR3	3 input OR gate
OR3X2	3 input OR gate with x2 drive
OR4	4 input OR gate

Complex Gates

A2A2O2I	2 2-IP AND's into 2-IP NOR gate
O2O2A2I	2 2-IP OR's into 2-IP NAND gate
A2O2I	2-IP AND gate into 2-IP NOR gate
O2A2I	2-IP OR gate into 2-IP NAND gate
A2O3I	2-IP AND gate into 3-IP NOR gate
O2A3I	2-IP OR gate into 3-IP NAND gate
A3O2I	3-IP AND gate into 2-IP NOR gate
O3A2I	3-IP OR gate into 2-IP NAND gate
A2O2A2I	2-IP AND gate into 2-IP OR gate into 2-IP NAND gate
O2A2O2I	2-IP OR gate into 2-IP AND gate into 2-IP NOR gate

Exclusive ORs and Adders

EXOR	Exclusive OR gate
EXNOR	Exclusive NOR gate
HADD	Half adder
FADD	1 bit full adder
FADD2	2 bit full adder

Multiplexers

MUX2TO1	2 to 1 multiplexer
MUX4TO1	4 to 1 multiplexer
MUX8TO1	8 to 1 multiplexer

Tristate Drivers

BDRX4	Tristate bus driver with x4 drive
BDRX8	Tristate bus driver with x8 drive
BHOLD	Tristate bus hold

Clock Drivers

Cell Name	Cell Function
CLKP	Positive edge clock driver
CLKPX2	Positive edge clock driver with x2 drive
CLKPX3	Positive edge clock driver with x3 drive
CLKN	Negative edge clock driver
CLKNX2	Negative edge clock driver with x2 drive
CLKNX3	Negative edge clock driver with x3 drive

Clock Grid Drivers

CLKB84	Clock Grid Driver for CLT84000
CLKB85	Clock Grid Driver for CLT85000, MLT85000
CLKB86	Clock Grid Driver for CLT86000
CLKB87	Clock Grid Driver for CLT87000, MLT87000
CLKB88	Clock Grid Driver for CLT88000, MLT88000
CLKB89	Clock Grid Driver for CLT89000, MLT89000

Latches

SRLATCH	Set-Reset latch
DL	Data latch
DLR	Data latch with reset
BDL	Buffered data latch
BDLR	Buffered data latch with reset

Registers

DF	Master-slave D-type flip-flop
DFRS	Master-slave D-type flip-flop with set and reset
MDF	Multiplexed master-slave D-type flip-flop
MDFRS	Multiplexed master-slave D-type flip-flop with set and reset
SDF	Buffered clock master-slave D-type flip-flop
SDFR	Buffered clock master-slave D-type flip-flop with reset
SDFRS	Buffered clock master-slave D-type flip-flop with set and reset
SDFS	Buffered clock master-slave D-type flip-flop with set
SMDF	Buffered clock multiplexed master-slave D-type Flip-Flop
SMDFRS	Buffered clock multiplexed master-slave D-type flip-flop with set and reset
BDF	Buffered master-slave D-type flip-flop
BDFRS	Buffered master-slave D-type flip-flop with set and reset
BMDF	Buffered multiplexed master-slave D-type flip-flop
BMDFRS	Buffered multiplexed master-slave D-type flip-flop with set and reset

Input Cells

IPNR	Input with no pullup/pulldown resistor
IPR2P	Input with 2KOhms pullup resistor
IPR4P	Input with 100KOhms pullup resistor
IPR2M	Input with 2KOhms pulldown resistor
IPR4M	Input with 100KOhms pulldown resistor

Level Shifter Cells

DRV6	Multiple output driver cell
IBST1	CMOS schmitt trigger, 5 volt supply
IBST2	TTL schmitt trigger, 5 volt supply
IBST3	CMOS & TLL schmitt trigger, 3 volt supply
IBTTL1	TTL input: 5 volt supply
IBTTL2	TTL input: 3 volt supply
IBCMOS1	CMOS input: 5 volt supply
IBLEVELS	3 volt to 5 volt signal interface

Output Driver Controllers

IBCOP	Controller for push-pull, open source, and open drain output driver
IBCOP3	Controller for push-pull, open source, and open drain output driver
IBTRID	Controller for tristate output driver
IBTRID3	Controller for tristate output driver

Output Driver Cells

OPT1	Small output driver
OPT2	Small output driver
OPT3	Small output driver
OPT6	Standard output driver
OPT12	Large output driver

CLA8PARA LIBRARY

SPRAM	Single port RAM register file
DPRAM	Dual port RAM register file

CLA8JTAG LIBRARY

GGJTAP	JTAG Interface Controller
GGIDREG	JTAG identification register
GGJTREG	JTAG boundary scan register

Oscillator Cells

OSC32K	32kHz Crystal Oscillator
OSCHIGH	10 to 16MHz Crystal Oscillator
OSCMID	1 to 10MHz Crystal Oscillator
OSCVHIGH	15 to 25MHz Crystal Oscillator

DSP Macrocell Library

BMA8X8	Mixed Mode multiplier (8 by 8 bits)
BMA16X16	Mixed Mode multiplier (16 by 16 bits)

DESIGN SUPPORT

Design Route

■ Flexible design route

■ Proven right first time design

Design and layout support for the CLA80k arrays is available from many centres worldwide each of which is connected to our headquarters via high speed data links. A design centre engineer is assigned to each customer's circuit to ensure the best assistance, and a smooth and efficient design flow.

Zarlink offers a variety of formal design routes as illustrated in Figure 5. A choice of routes allow for varying levels of customer involvement in a manner which complements individual customers' design styles, whilst maintaining Zarlink's responsibility to ensure first time working devices.

The design process incorporates a design audit procedure to verify compliance with customer specification and to ensure manufacturability. The procedure includes four review meetings with the customer held at key stages of the design.

Review 1: Held at the beginning of the design cycle to check and agree on performance, packaging, specifications and design timescales.

Review 2: Held after Logic Simulation but prior to layout to ensure satisfactory functionality, timing performance, and adequate fault coverage.

Review 3: Held after Layout and Post Layout Simulation Verification of satisfactory design performance after insertion of actual track loads. Final check of all device specifications before prototype manufacture.

Review 4: Held after Prototype Delivery to confirm that devices meet all specifications and are suitable for full scale production.

CAE Support

■ Synthesis with Synopsys, Mentor or Cadence

■ Sign-off simulation with Mentor or Cadence

■ VIEWlogic VCS simulator supported

■ VITAL compliant library

■ Full top-down design flow support

■ Point tools supported, including Zycad and Powermill

■ Direct route to layout and test

■ Advanced delay modelling and netlist checking

It is Zarlink policy to fully support industry-standard CAE systems that enable a customer to sign off their design without resimulation on a golden simulator. This has the benefit to the customer of not having to learn new tools, and to use the tools they prefer and are familiar with. There is no overhead in engineering effort or time taken rechecking simulation results.

Zarlink offers libraries for synthesis tools such as Synopsys, Mentor Autologic II, and Cadence Synergy. This allows a full hierarchical or top-down approach to logic design. The Zarlink's Universal Delay Compiler (UDC) is supplied with all design kits for advanced delay modelling and comprehensive netlist checking. The UDC matches Synopsys and Mentor native delay calculation.

The advanced features of the synthesis and simulation tools are used for nonlinear delay modelling for better simulation accuracy. This is implemented for optimum speed depending on the particular tool. Other advanced features are supported where they are available.

The information supplied by the customer in the approved CAE vendor format is used as a direct input to the tools that perform the layout and generate the test program.

SOFTWARE TOOLS

RESPONSIBILITY

Concept — **CUSTOMER**

Assessment

DESIGN REVIEW 1 — **CUSTOMER AND Zarlink**

Design capture/compilation or synthesis

INDUSTRY STANDARD DESIGN SOFTWARE AND Zarlink LIBRARIES

Testability analysis → Improve testability

Functional simulation → Correct design errors

Test vectors simulation → Improve testability

CUSTOMER OR Zarlink

Zarlink VERIFICATION TOOLS

Netlist handover — **Zarlink**

DESIGN REVIEW 2 — **CUSTOMER AND Zarlink**

Zarlink OR INDUSTRY-STANDARD LAYOUT TOOLS

Place and route ← Netlist modification

Post-layout simulation

CUSTOMER OR Zarlink

INDUSTRY-STANDARD SOFTWARE

DESIGN REVIEW 3 — **CUSTOMER AND Zarlink**

Prototype manufacture — **Zarlink**

APPROVAL — **CUSTOMER AND Zarlink**
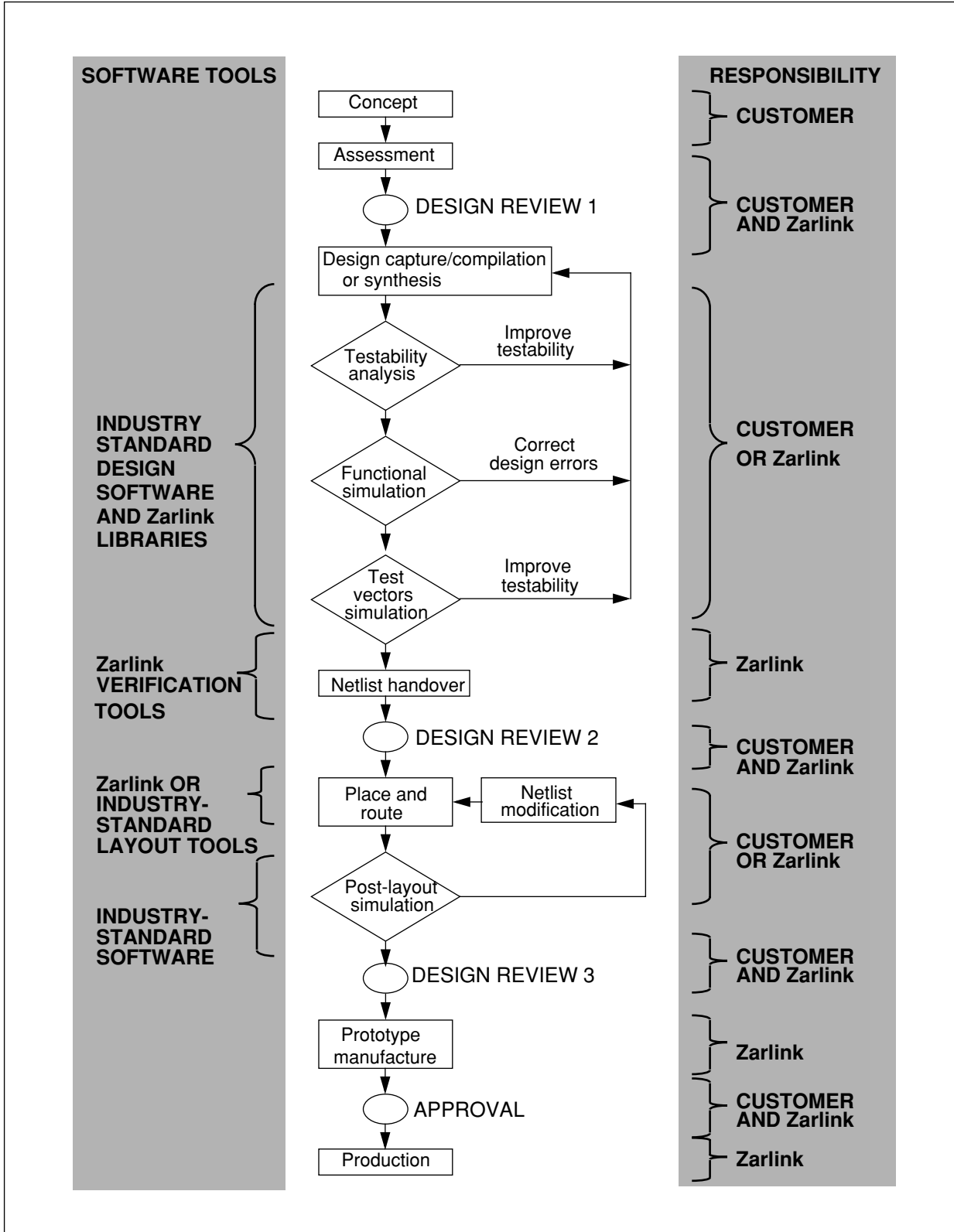
Production — **Zarlink**

Figure 5 Design Flow

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THERMAL MANAGEMENT

- Low power CMOS for better thermal management
- 1.3μW per gate per MHz (3V supply)
- High pinout power packages available

The increase in speed and density available through advanced CMOS processes, results in a corresponding increase in power dissipation. SemiCustom designers now have the ability to design circuits of 260,000 gates and over, and chip power consumption is a very important concern.

The logic core of 260k plus gates is the dominant factor in power dissipation at this complexity. It is essential to offer ultra low power core logic to maintain an acceptable overall chip power budget.

To minimize this problem Zarlink's CLA80k arrays offer low power factors and a selection of power packages. Dissipation of 1.3μW per gate per MHz (3V supply) is lower than most competitive arrays, with the reduced junction temperatures having the added advantage of improved performance and reliability.

CLA80k POWER DISSIPATION CALCULATION

CLA80k series power dissipation for any array can be estimated by following the example for the CLA87XXX at a typical voltage of 5V.

Number of available gates	157872
Gates used	40%
Gates switching	15%
Power dissipation/gate/MHz (μW) (gate fanout typically 2 loads, at 5V)	4.1
Frequency (MHz)	10
Total core dissipation (mW)	388
Number of I/O pads used as Outputs	122
Outputs switching each cycle	20%
Dissipation/output buffer/MHz/pF (μW)	25
Output loading in pF	50
Output buffer power (mW)	305
Total Power at 10MHz clock rate (W)	0.7

ADVANCED DELAY MODELLING

- Accurate delay calculation
- Edge speed modelling
- Pin to pin timings
- Non-linear delay modelling
- Accurate delay derating

The accuracy of the delay modelling is demonstrated by the results shown in the table over.

Pin to Pin Delays

Delay models use pin to pin times for both rising and falling delays between each input and output pin.
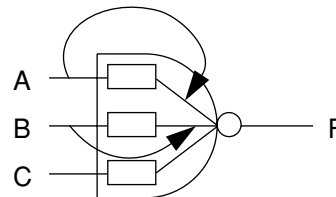

Figure 6 Path dependent delays

The use of pin to pin delays improves simulation accuracy as there can be considerable variation in delay between different input pins. For complex gates (e.g. AND-NOR gates or adders) the variation is up to 40%. For simple NAND and NOR logic gates the typical variation is 20%.

Non-linear curve fitting

Figure 7 and Figure 8 show the rising and falling delay through an inverter. For fast input edges (0.5ns) delay time increases linearly with the output load. For high output loads delay increases linearly with edge speed. Delay for slow input edges and light input loads do not follow the linear model. A simple linear model cannot represent delay accurately. The following equation is used to model delay for CLA80k

$$Delay = K_1 + K_2 Load + K_3 Edge - \left(\frac{K_4 Edge}{e^{\left(\frac{K_5 Load}{Edge} \right)}} \right)$$

K_1 -Intrinsic delay. The delay with load and input edge speed set to zero.

K_2 -Delay sensitivity to load.

K_3 -Delay sensitivity to input edge speed.

K_4 & K_5 - These coefficients reduce the effect of edge for light output loadings.

Cell	Conditions	CLA80k delay (ps)	SPICE (ps)	Accuracy
8 stage ripple carry adder	Typical process, 5V, 25°C	4872	4679	4.0%
8 stage ripple carry adder	Slow process, 4.5V, 70°C	7696	7455	3.2%
10 NAND2 gates, lightly loaded	Slow process, 4.5V, 70 ° C	3463	3464	0.0%
10 NAND2 gates mixed heavy then light loading	Slow process, 4.5V, 70°C	12825	12479	2.8%
10 NAND2 gates heavy loading	Slow process, 4.5V, 70°C	27421	28606	4.1%
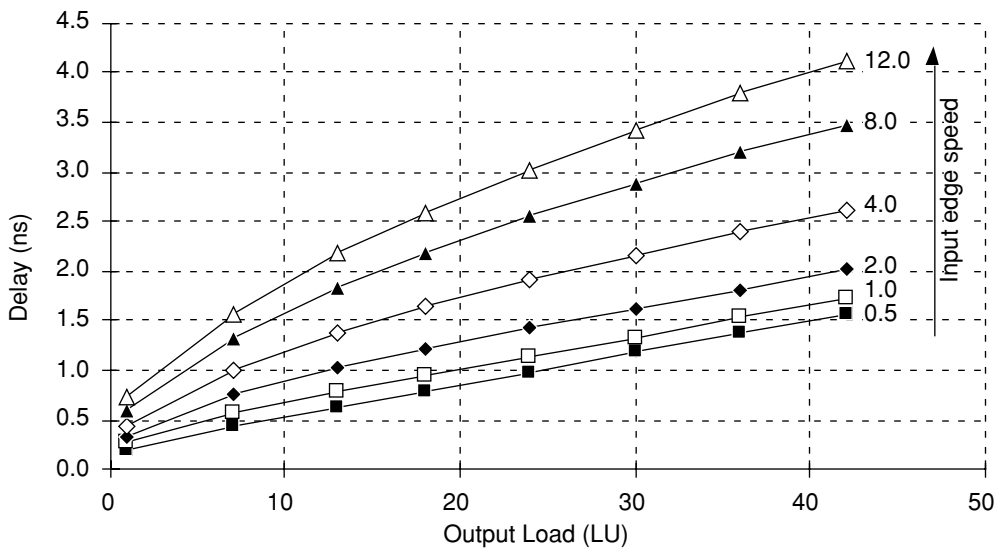
Figure 7 Inverter falling delay

Figure 8 Inverter rising delay

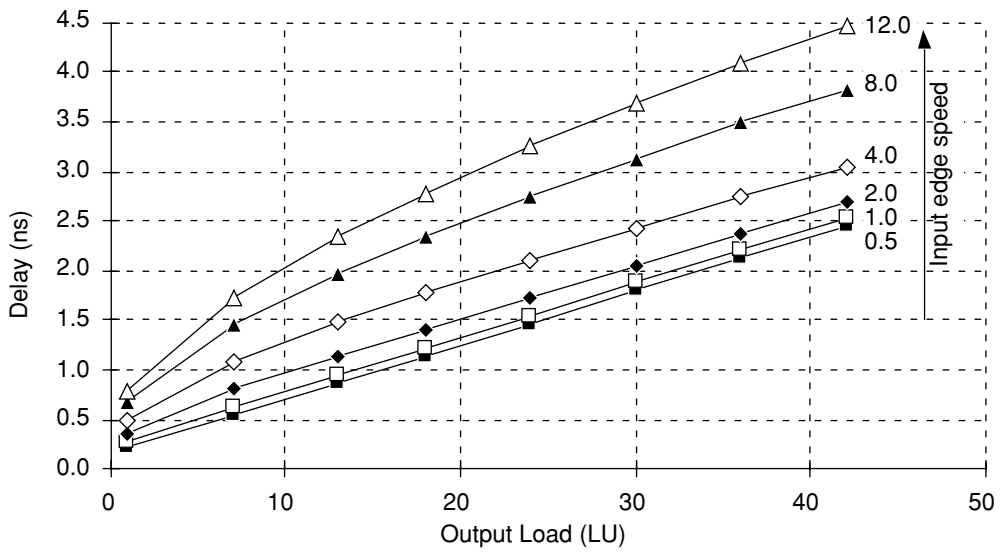## Derating for Supply Voltage

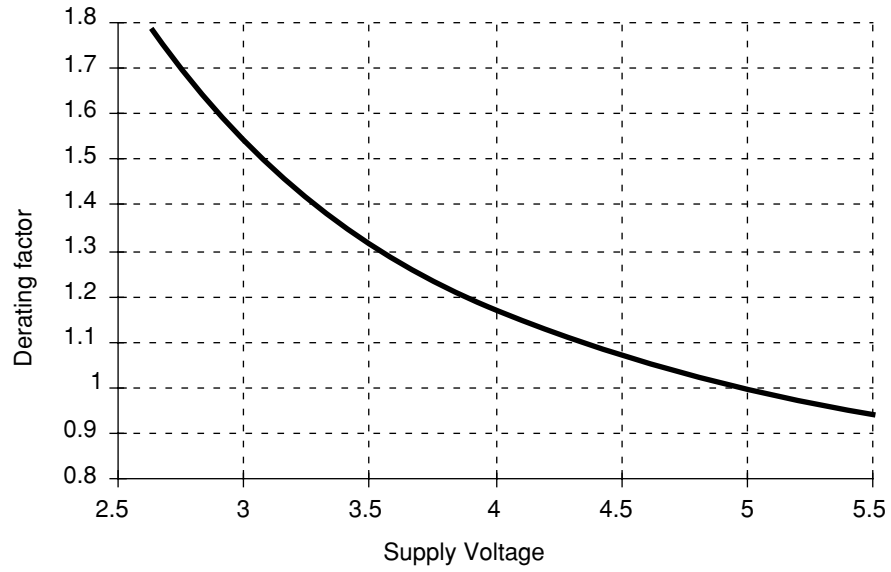Figure 9 shows the increase in gate delay as supply voltage is reduced.

Figure 9 Derating with supply voltage

Derating for Temperature

Figure 10 shows the increase in gate delay as the chip junction temperature is increased. It is important to use the junction and not the ambient temperature for worst case simulations
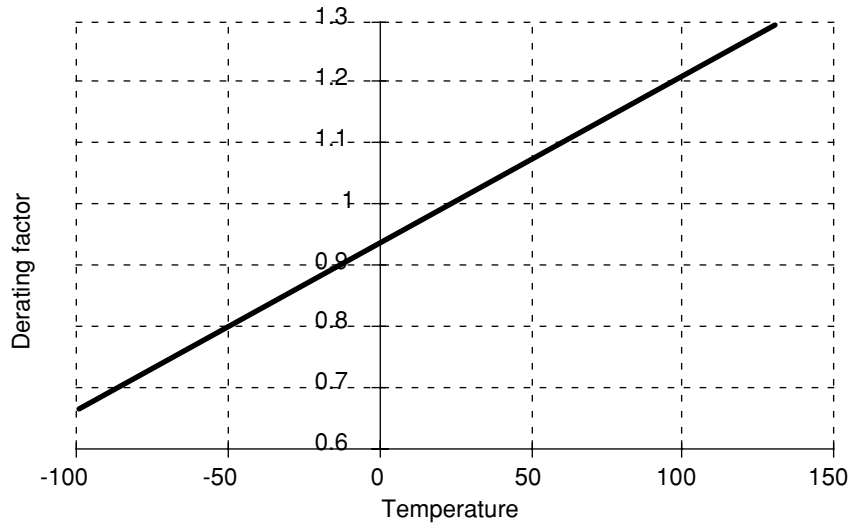

Figure 10 Derating with Temperature

AC ELECTRICAL CHARACTERISTICS

GATES		3V		4.5V	
		2 load units	4 load units	2 load units	4 load units
INVX1	tpLH	590 ps	889 ps	421 ps	613 ps
	tpHL	283 ps	391 ps	197 ps	272 ps
NAND2X2	tpLH	528 ps	683 ps	392 ps	490 ps
	tpHL	291 ps	398 ps	200 ps	269 ps
NOR2x2	tpLH	752 ps	1065 ps	476 ps	664 ps
	tpHL	249 ps	303 ps	162 ps	205 ps
DF	tpLH	1068 ps	1412 ps	689 ps	910 ps
	tpHL	970 ps	1117 ps	584 ps	685 ps

INPUTS		3V		4.5V	
		2 load units	4 load units	2 load units	4 load units
TTL I/P	tpLH	767 ps	922 ps	708 ps	810 ps
	tpHL	704 ps	761 ps	114 ps	1168 ps
CMOS I/P	tpLH	791 ps	872 ps	547 ps	599 ps
	tpHL	629 ps	659 ps	433 ps	454 ps
CMOS SCHMITT	tpLH	1413 ps	1592 ps	1114 ps	1223 ps
	tpHL	1703 ps	1778 ps	786 ps	831 ps

OUTPUT		3V		4.5V	
		2 pF	4 pF	2 pF	4 pF
6mA BISTATE	tpLH	3615 ps	8811 ps	2320 ps	5700 ps
	tpHL	2472 ps	4549 ps	1538 ps	2886 ps
12mA BISTATE	tpLH	4672 ps	7286 ps	2842 ps	4552 ps
	tpHL	3814 ps	5106 ps	2315 ps	3073 ps
24mA OPEN DRAIN	tpLH	5500 ps	6917 ps	3306 ps	4321 ps
	tpHL	5011 ps	6463 ps	2915 ps	3860 ps

Notes: Assumes worst case process, temperature = 70°C, input edge = 0.5 nS

ABSOLUTE MAXIMUM RATINGS

PARAMETER	Min.	Max.	Units
Supply Voltage	-0.5	7.0	V
Input Voltage	-0.5	V_{DD}+0.5	V
Output Voltage	-0.5	V_{DD}+0.5	V
Static discharge voltage (HBM)		4	kV
Storage Temperature			
Ceramic	-65	150	°C
Plastic	-40	125	°C

Exceeding the absolute maximum ratings may cause permanent damage to the device. Extended exposure at the maximum ratings will affect device reliability. HBM stands for Human Body Model.

NORMAL OPERATING CONDITIONS

Neither performance nor reliability is guaranteed outside these limits. Extended operation above these limits may affect device reliability.

PARAMETER	Min.	Max.	Units
Supply Voltage	2.7	5.5	V
Input Voltage	V_{SS}	V_{DD}	V
Output Voltage	V_{SS}	V_{DD}	V
Current per pad		100	mA
Junction Temperature	-55	150	∞°C
Ambient Temperature			
Commercial Grade	0	70	∞°C
Industrial Grade	-40	85	°C
Military Grade	-55	125	°C

DC ELECTRICAL CHARACTERISTICS

All characteristics are for -55 to150°C and 2.7 to 5.5V unless otherwise specified
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Characteristic	Sym	Value			Unit	Conditions
		Min.	Typ.	Max.		
Operating Power	P_{DD}		1.3		µW/ MHz	V_{DD} = 3V, for NAND2 with 2 standard loads
			4.1			V_{DD} = 5V, for NAND2 with 2 standard loads
Input capacitance	C_I		5		pF	Any input, excluding package
Output capacitance	C_{OUT}		6		pF	Any output, excluding package
Bidirectional capacitance	C_{BI}		6		pF	Any I/O pin, excluding package

Input Characteristics

Characteristic	Sym	Value			Unit	Conditions
		Min.	Typ.	Max.		
TTL input - IBTTL1						$4.5 \leq V_{DD} \leq 5.5V$
Input low voltage	V_{IL}			0.8	V	
Input high voltage	V_{IH}	2.0			V	
TTL input - IBTTL2						$2.7 \leq V_{DD} \leq 3.6V$
Input low voltage	V_{IL}			0.8	V	
Input high voltage	V_{IH}	2.0			V	
CMOS input - IBCMOS1						$2.7 \leq V_{DD} \leq 5.5V$
Input low voltage	V_{IL}			$0.2V_{DD}$	V	
Input high voltage	V_{IH}	$0.7V_{DD}$			V	
CMOS Schmitt - IBST1						$4.5 \leq V_{DD} \leq 5.5V$
Input low voltage	V_{IL}			$0.2V_{DD}$	V	
Input high voltage	V_{IH}	$0.7V_{DD}$			V	
Hysteresis	V_H	400			mV	
TTL Schmitt - IBST2						$4.5 \leq V_{DD} \leq 5.5V$
Input low voltage	V_{IL}			0.8	V	
Input high voltage	V_{IH}	2.0			V	
Hysteresis	V_H	300			mV	
Low voltage Schmitt - IBST3						$2.7 \leq V_{DD} \leq 3.6V$
Input low voltage	V_{IL}			$0.2V_{DD}$	V	
Input high voltage	V_{IH}	$0.7V_{DD}$			V	
Hysteresis	V_H	80			mV	
Input current or resistance						
Pullup - IPR2P	R_1	1	2	4	kΩ	
Pullup - IPR4P	R_2	50	110	220	kΩ	
Pulldown - IPR2M	R_3	1	2	4	kΩ	
Pulldown - IPR4M	R_4	50	110	220	kΩ	

Output Characteristics

Characteristic	Sym	Value			Unit	Conditions
		Min.	**Typ.**	**Max.**		
High output voltage						$2.7 \leq V_{DD} \leq 3.6V$
All outputs	V_{OH}		V_{DD}-0.05		V	I_{OH} = -1µA
OPT1	V_{OH}	$0.8V_{DD}$	$0.9V_{DD}$		V	I_{OH} = -0.8mA
OPT2	V_{OH}	$0.8V_{DD}$	$0.9V_{DD}$		V	I_{OH} = -1.6ma
OPT3	V_{OH}	$0.8V_{DD}$	$0.9V_{DD}$		V	I_{OH} = -2mA
OPT6	V_{OH}	$0.8V_{DD}$	$0.9V_{DD}$		V	I_{OH} = -4mA
OPT12	V_{OH}	$0.8V_{DD}$	$0.9V_{DD}$		V	I_{OH} = -8mA
Low output voltage						$2.7 \leq V_{DD} \leq 3.6V$
All outputs	V_{OL}		V_{SS}-0.05		V	I_{OL} = 1µA
OPT1	V_{OL}		0.2	0.4	V	I_{OL} = 1mA
OPT2	V_{OL}		0.2	0.4	V	I_{OL} = 2mA
OPT3	V_{OL}		0.2	0.4	V	I_{OL} = 3mA
OPT6	V_{OL}		0.2	0.4	V	I_{OL} = 6mA
OPT12	V_{OL}		0.2	0.4	V	I_{OL} = 12mA
High output voltage						$4.5 \leq V_{DD} \leq 5.5V$
All outputs	V_{OH}		V_{DD}-0.05		V	I_{OH} = -1µA
OPT1	V_{OH}	$0.8V_{DD}$	$0.9V_{DD}$		V	I_{OH} = -2mA
OPT2	V_{OH}	$0.8V_{DD}$	$0.9V_{DD}$		V	I_{OH} = -4mA
OPT3	V_{OH}	$0.8V_{DD}$	$0.9V_{DD}$		V	I_{OH} = -6mA
OPT6	V_{OH}	$0.8V_{DD}$	$0.9V_{DD}$		V	I_{OH} = -12mA
OPT12	V_{OH}	$0.8V_{DD}$	$0.9V_{DD}$		V	I_{OH} = -24mA
Low output voltage						$4.5 \leq V_{DD} \leq 5.5V$
All outputs	V_{OL}		V_{SS}-0.05		V	I_{OL} = 1µA
OPT1	V_{OL}		0.2	0.4	V	I_{OL} = 2mA
OPT2	V_{OL}		0.2	0.4	V	I_{OL} = 4mA
OPT3	V_{OL}		0.2	0.4	V	I_{OL} = 6mA
OPT6	V_{OL}		0.2	0.4	V	I_{OL} = 12mA
OPT12	V_{OL}		0.2	0.4	V	I_{OL} = 24mA

Characteristic	Sym	Value			Unit	Conditions
		Min.	Typ.	Max.		
Tristate output leakage						-55 to 100°C
OPT1	I_{OZ}	-1		1	μA	$V_{OUT} = V_{SS}$ or V_{DD}
OPT2	I_{OZ}	-1		1	μA	$V_{OUT} = V_{SS}$ or V_{DD}
OPT3	I_{OZ}	-1		1	μA	$V_{OUT} = V_{SS}$ or V_{DD}
OPT6	I_{OZ}	-1		1	μA	$V_{OUT} = V_{SS}$ or V_{DD}
OPT12	I_{OZ}	-1		1	μA	$V_{OUT} = V_{SS}$ or V_{DD}
Tristate output leakage						-55 to 150°C
OPT1	I_{OZ}	-2		2	μA	$V_{OUT} = V_{SS}$ or V_{DD}
OPT2	I_{OZ}	-2		2	μA	$V_{OUT} = V_{SS}$ or V_{DD}
OPT3	I_{OZ}	-2		2	μA	$V_{OUT} = V_{SS}$ or V_{DD}
OPT6	I_{OZ}	-2		2	μA	$V_{OUT} = V_{SS}$ or V_{DD}
OPT12	I_{OZ}	-4		4	μA	$V_{OUT} = V_{SS}$ or V_{DD}
Output short circuit current						$4.5 \le V_{DD} \le 5.5V$
OPT1	I_{OS}	14	28	55	mA	V_{DD} = max., $V_O = V_{DD}$
OPT2	I_{OS}	28	55	110	mA	V_{DD} = max., $V_O = V_{DD}$
OPT3	I_{OS}	41	82	164	mA	V_{DD} = max., $V_O = V_{DD}$
OPT6	I_{OS}	82	164	328	mA	V_{DD} = max., $V_O = V_{DD}$
OPT12	I_{OS}	164	328	656	mA	V_{DD} = max., $V_O = V_{DD}$
Output short circuit current						$4.5 \le V_{DD} \le 5.5V$
OPT1	I_{OS}	6	12	25	mA	V_{DD} = max., $V_O = V_{SS}$
OPT2	I_{OS}	12	25	50	mA	V_{DD} = max., $V_O = V_{SS}$
OPT3	I_{OS}	19	38	76	mA	V_{DD} = max., $V_O = V_{SS}$
OPT6	I_{OS}	38	76	152	mA	V_{DD} = max., $V_O = V_{SS}$
OPT12	I_{OS}	76	152	304	mA	V_{DD} = max., $V_O = V_{SS}$
Output short circuit current						$2.7 \le V_{DD} \le 3.6V$
OPT1	I_{OS}	5	11	21	mA	V_{DD} = max., $V_O = V_{DD}$
OPT2	I_{OS}	10	22	42	mA	V_{DD} = max., $V_O = V_{DD}$
OPT3	I_{OS}	16	32	64	mA	V_{DD} = max., $V_O = V_{DD}$
OPT6	I_{OS}	32	64	128	mA	V_{DD} = max., $V_O = V_{DD}$
OPT12	I_{OS}	64	128	256	mA	V_{DD} = max., $V_O = V_{DD}$
Output short circuit current						$2.7 \le V_{DD} \le 3.6V$
OPT1	I_{OS}	1.5	5	10	mA	V_{DD} = max., $V_O = V_{SS}$
OPT2	I_{OS}	3	10	20	mA	V_{DD} = max., $V_O = V_{SS}$
OPT3	I_{OS}	7	15	30	mA	V_{DD} = max., $V_O = V_{SS}$
OPT6	I_{OS}	15	30	60	mA	V_{DD} = max., $V_O = V_{SS}$
OPT12	I_{OS}	30	60	120	mA	V_{DD} = max., $V_O = V_{SS}$

QUALITY AND RELIABILITY

■ Statistical process control used in manufacture
■ Regular sample screening and reliability testing
■ Screening to MIL and other recognized standards

At Zarlink quality and reliability are built into the product by statistical control of all of processing operations and by minimizing random uncontrolled effects in all manufacturing operations. Process management involves full documentation of procedures, recording of batch by batch data using traceable procedures. This is preformed using the latest equipment to perform sample screening and conformance testing on finished product.

A common information management system is used to monitor the manufacturing of Zarlink CMOS and bipolar processes and operations. All product benefit from the use of this integrated monitoring system resulting in the highest quality standards for all technologies.

Further information is contained in the Quality Brochure, available from Zarlink Sales Offices.

PACKAGING

■ Wide range of surface mount and through board packages
■ Ceramic equivalents to most plastic packages for fast prototyping
■ Ongoing commitment to new package development

Packaging Options

The package style and pin count information is intended only as a guide. Detailed package specifications are available from Zarlink design centres on request. New packages are being continually introduced, so if a particular package is not listed, please enquire through your Zarlink Sales Representative.

The tables below indicate the preferred array size to package combinations. A stock is held of a preferred packages to insure a fast prototype assembly turn around. Alternative array size to package combinations are available, however these packages are not held in stock and extended lead times may adversely affect prototype delivery schedules.

KEY:

1234	Format Number of Preferred Array/Qualified Package Combination
1234	Format Number of Physical Fit only - requires Marketing approval prior to quotation

†	In development
1234*	Maximum number of ceramic prototypes is 10 ONLY
1234^	NO footprint compatible ceramic prototypes are available

Note: Package dimensions implicit in the 'Code' description, pitch and height dimensions are for guidance only and therefore are approximate.

HIGH DENSITY PAD ARRAY PRODUCTION PACKAGING OPTIONS

Metric Quad Flat Pack - plastic.													
Style	Leads	Code	Pitch	Height	81	82	83	84	85	86	87	88	89
M Q F P	44	MQFP44-GP-1010	0.80	2.0	2152	2152	2152	2152					
	52	MQFP52-GP-1010	0.65	2.0	1710	1710	1710	1710	1710^				
	64	MQFP64- GP-1420	1.00	2.8	1755	1755	1755	1755	1755				
	64	MQFP64-GP-1414	0.80	2.8	1835^	1835^	1835^	1835					
	64	MQFP64-GP-1414	0.80	2.0	2172^	2172^	2172^	2172	2172	2172			
	80	MQFP80-GP-1420	0.80	2.8	2157	2157	2157	2157	2157				
	80	MQFP80-GQ-1414	0.65	2.0	1807^	1807	1807	1807	1807	1808			
	100	MQFP100-GP-1420	0.65	2.8	2166	2166	2166	2158	2158	2158			
	120	MQFP120-GP-2828	0.80	3.4		1730^	1899	1899	1899	1899	1732		
	128	MQFP128-GP-2828	0.80	3.4		2100^	2100	2100	2100	2100	1713^		
	144	MQFP144-GP-2828	0.65	3.4		2159^	2159^	2159	2159	2159			
	160	MQFP160-GP-2828	0.65	3.4			1882^	1882^	1882^	1882	1882	2118^	

FQFP (Fine Pitch) - plastic.													
Style	Leads	Code	Pitch	Height	81	82	83	84	85	86	87	88	89
F	100	FQFP100-FP-1414	0.50	2.0	1810	1810	1810	2156	2156	2156^			
Q	208	FQFP208-FP-2828	0.50	3.4				2160^	2160^	2160^	2160		
F	240	FQFP240-FP-3232	0.50	3.4							2163^	2163	
P	304	FQFP304-FP-4040	0.50	3.8								1880^	

LQFP (Low profile) - plastic.													
Style	Leads	Code	Pitch	Height	81	82	83	84	85	86	87	88	89
L Q F	48	LQFP48-FP-0707	0.50	1.4	2168^	2168^							
	64	LQFP64-FP-1010	0.50	1.4	2130	2130	2130	2130^	2130^				
	80	LQFP80- GP-1414	0.65	1.4	1889	1889	1889	1889	1889				
	100	LQFP100-FP-1414	0.50	1.4	1887	1887	1887	1888	1888	1888			

P	144	LQFP144-FP-2020	0.50	1.4	2164^	2164^	2164^	2164	2164	2237	2237^		
	176	LQFP176-FP-2424	0.50	1.4		2165^	2165^	2165^	2165^	2165			

PLCC (Plastic J - Leaded Chip Carrier).													
Style	Leads	Code	Pitch	Height	81	82	83	84	85	86	87	88	89
P	28	PLCC28-HP-1212	1.27	4.57	1613	1613	1613	1629					
L	44	PLCC44-HP-1717	1.27	4.57	1491	1491	1491	1491	1491				
C	68	PLCC68-HP-2525	1.27	5.08	1659	1659	1659	1659					
C	84	PLCC84-HP-3030	1.27	5.08	1660	1660	1660	1660	1660				

PSOP (Plastic Small Outline package).													
Style	Leads	Code	Pitch	Height	81	82	83	84	85	86	87	88	89
P	16	PSOP16-MP-0811	1.27	2.64	1575								
S	20	PSOP20-MP-0813	1.27	2.64	1583								
O	24	PSOP24-MP-0816	1.27	2.64	1587								
P	28	PSOP28-MP-0818	1.27	2.64	1768	1768^							

P2QFP ('PowerQuad 2') - plastic with copper heat slug.													
Style	Leads	Code	Pitch	Height	81	82	83	84	85	86	87	88	89
	100	P2QFP100-GH-1420	0.65	2.8		2202	2202	2202	2202				
P	120	P2QFP120-GH-2828	0.80	3.4			3002	3002	3002	3002	2200	2200^	
2	128	P2QFP128-GH-2828	0.80	3.4			2221	2221	2221	2221	2221^	2203^	
Q	144	P2QFP144-GH-2828	0.65	3.4			2222^	2222	2222	2222	2222	2226^	
F	160	P2QFP160-GH-2828	0.65	3.4			2223^	2223^	2223	2223	2223^	2196^	
P	208	P2QFP208-GH-2828	0.50	3.4						2225^	2225	2218	2218^
	240	P2QFP240-GH-3232	0.50	3.4								2229	2229
	304	P2QFP304-GH-4040	0.50	3.4								2219^	2219^

HIGH DENSITY PAD ARRAY PROTOTYPING PACKAGING OPTIONS

Important: CQFP/CSOP is for prototyping only, it is not available for production.

Style	Leads	Code	Pitch	Height	81	82	83	84	85	86	87	88	89
					Prototypes for MQFP's and P2 & P4 MQFP's.								
	44	CQFP44-GG-1010	0.80	3.2	1735	1735	1735	1799					
	52	CQFP52-GG-1010	0.65	3.2	1800	1800	1800	1800					
	64	CQFP64- GG-1420	1.00	2.8	1773	1773	1773	1773	1772				
C	64	CQFP64-GG-1414	0.80	2.8				2169	2169	2169			
Q	80	CQFP80-GG-1420	0.80	2.8	1740	1740	1740	1740	1771				
F	80	CQFP80-GG-1414	0.65	2.8	2102	2102	2102	2102	2102	1863			
P	100	CQFP100-GG-1420	0.65	2.8	1865	1865	1865	1865	1865	1864			
	120	CQFP120-GG-2828	0.80	3.6	1736	1736	1736	1736	1736	1737	1737		
	128	CQFP128-GG-2828	0.80	3.6			1861	1861	1861	1861			
	144	CQFP144-GG-2828	0.65	3.6				1816	1816	1816	1770		
	160	CQFP160-GG-2828	0.65	3.6						1769	1769		

Style	Leads	Code	Pitch	Height	81	82	83	84	85	86	87	88	89
					"Prototypes for FQFP, LQFP & P2 MQFP's. "								
	64	CQFP64-FG-1010	0.50	3.2	2103	2103	2103						
C	100	CQFP100-FG-1414	0.50	2.8	1860	1860	1860	1860	1860	2101			
Q	144	CQFP144-FG-2020	0.65	3.6				2104	2104	2104			
F	176	CQFP176-FG-2424	0.50	3.77						2217	2217		
P	208	CQFP208-FG-2828	0.50	3.6							2141	2141	
	240	CQFP240-FG-3232	0.50	3.6								2143	
	304	CQFP304-FG-4040	0.50	3.6									2144

Prototypes for PLCC													
Style	Leads	Code	Pitch	Height	81	82	83	84	85	86	87	88	89
C	28	CcLCC28-HC-1212	1.27	4.11	1623	1623	1623	1623					
c	44	CcLCC44-HC-1717	1.27	3.43	1453	1453	1453	1453	1453				
L	68	CcLCC68-HC-2525	1.27	3.43	1625	1625	1625	1625					
C	84	CcLCC84-HC-3030	1.27	3.43	1626	1626	1626	1626	1626				
C													

Prototypes for PSOP													
Style	Leads	Code	Pitch	Height	81	82	83	84	85	86	87	88	89
C	16	CSOP16-MC-0811	1.27	2.75	1697								
S	20	CSOP20-MC-0813	1.27	2.75	1698								
O	24	CSOP24-MC-0816	1.27	2.75	1699								
P	28	CSOP28-MC-0818	1.27	2.75	1875								

STANDARD DENSITY PAD ARRAY PACKAGING OPTIONS, MILITARY ARRAYS

		PLCC						
Style	Leads	Code	Pitch	Height	MLA85	MLA87	MLT88	MLT89
C	68	CcLCC68-HC-2525	1.27	3.43	1621			
c	84	CcLCC84-HC-3030	1.27	3.43	1626			
L								
C								
C								

		LdCC						
Style	Leads	Code	Pitch	Height	MLA85	MLA87	MLT88	MLT89
L	132	LdCC132-GCA-2424	0.635	2.57	1840	1662		
d	172	LdCC172-GCA-3030	0.635	2.82		1668	1680	
C	196	LdCC196-GCA-3535	0.635	2.82		1672	1831	
C								

		LdCC & TLdCC (Power)						
Style	Leads	Code	Pitch	Height	MLA85	MLA87	MLT88	MLT89
L	132	LdCC132-GCP-2424	0.635	3.33	2146	1841		
d	172	LdCC172-GCP-3030	0.635	3.58		1836	1762	2147
C	196	LdCC196-GCP-3535	0.635	3.58		1839	1739	1832
C	256	LdCC256-GCP-3737	0.51	3.66			1834	
T	132	TLdCC132-YCP-2424	0.62	3.33			2127	
L	172	TLdCC172-YCP-3030	0.62	3.61			2215	
d	320	TLdCC320-YCP-4444	0.5	2.64			2206	2205

		PGA						
Style	Leads	Code	Pitch	Height	MLA85	MLA87	MLT88	MLT89
	84	PGA84-ACA-2828	2.54	4.14	1479	1671		
	100	PGA100-ACA-3434	2.54	4.14	1480	1465		
P	120	PGA120-ACA-3434	2.54	4.14	1481	1466		
G	144	PGA144-ACA-4040	2.54	4.14		1483		
A	180	PGA180-ACA-4040	2.54	4.14		1484		
	181	PGA181-ACA-4040	2.54	4.14			1844	
	257	PGA257-ACA-5151	2.54	4.14			1824	2149

		PGA (Power)						
Style	Leads	Code	Pitch	Height	MLA85	MLA87	MLT88	MLT89
P	84	PGA(P)84-ACB-2828	2.54	6.15		1815	1692	
G	144	PGA(P)144-ACB-4040	2.54	6.15	2151	1812	1693	2148
A	208	PGA(P)208-ACB-4545	2.54	4.45			1838	2145
(P)	209	PGA(P)209-ACB-4545	2.54	4.45		1811		

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