8251/Am9551

Programmable Communication Interface iAPX86 Family MILITARY INFORMATION

DISTINCTIVE CHARACTERISTICS

- Separate control and transmit register input buffers
- Synchronous or asynchronous serial data transfer
- Parity, overrun, and framing errors detected
- Half- or full-duplex signaling
- Character length of 5, 6, 7, or 8 bits

- Internal or external synchronization
- Odd parity, even parity, or no parity bit
 - Modem interface controlled by processor Programmable Sync pattern
 - Fully TTL-compatible logic levels

GENERAL DESCRIPTION

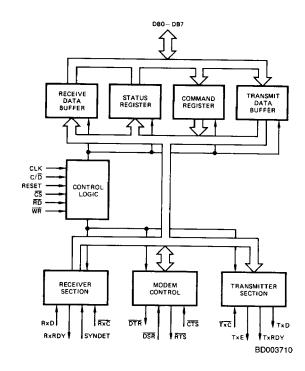
The 8251/Am9551 is a programmable serial data communication interface that provides a Universal Synchronous/Asynchronous Receiver/Transmitter (USART) function. It is normally used as a peripheral device for an associated processor and may be programmed by the processor to operate in a variety of standard serial communication formats.

The device accepts parallel data from the CPU, formats and serializes the information based on its current operating mode, and then transmits the data as a serial bit stream.

Simultaneously, serial data can be received, converted into parallel form, deformatted, and then presented to the CPU. The USART can operate in an independent full-duplex mode.

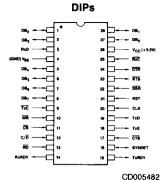
Data, control, operation, and format options are all selected by commands from an associated processor. This provides an unusual degree of flexibility and allows the 8251/ Am9551 to service a wide range of communication disciplines and applications.

BLOCK DIAGRAM



Publication # Rev. Amendment / 09233 A /0
Issue Date: November 1987

CONNECTION DIAGRAM Top View



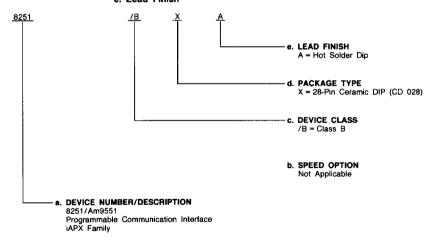
Note: Pin 1 is marked for orientation.

MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of: a. Device Number

- b. Speed Option (if applicable)
- c. Device Class
- d. Package Type
- e. Lead Finish



Valid Combinations 8251 AM9551 /BXA

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature65°C to +150°C
V _{CC} with Respect to V _{SS} ~0.5 to +7.0 V
All Signal Voltages
with Respect to VSS0.5 V to +7.0 V
Power Dissipation1.0 W

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Military (M) Devices				
Temperature (T _C)	55	to	+ 1	25°C
Supply Voltage (V _{CC})		5 V	±	10%

Operating ranges define those limits between which the functionality of the device is guaranteed.

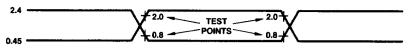
DC CHARACTERISTICS over operating range (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description		8251		Am9551		
		Test Conditions	Min.	Max.	Min.	Max.	Unit
V _{OH} Output HiGH Volta	Output HIGH Voltage	$I_{OH} = -200 \mu A, V_{CC} = 4.5 V$		885	2.4		
	- Tonage	I _{OH} = -100 μA	2	The T			· ·
VOL	Output LOW Voltage	I _{OL} = 1.6 mA, V _{CC} = 4.5 V		45		0.45	V
V _{IH}	Input HIGH Voltage	V _{CC} = 5 V ± 10	2.2	V _{CC} *	2.2	Vcc*	v
VIL	Input LOW Voltage	Vcc 5 V 10%	-0.5*	0.8	-0.5*	0.8	v
ել	Input Load Current	VCt = 5.5 = 5 V-0 V		±10		±10	μА
I _{DL} Data Rus Luckath	Data Bus I Mada	$V_{OU} = 0.25 \text{ V}, V_{CC} = 5.5 \text{ V}$		-50		-50	
	OUT = 5.5 V, V _{CC} = 5.5 V		10		10	μΑ	
lcc	V _{CC} Su pro Coren			120		120	mA
Co t	Output Capacitance			15*		15*	pF
C _I †	Input Capacitance	- 10 MHz (0.14		10*	 	10*	ρF
Ci/O †	I/O Capacitance	fc = 1.0 MHz, Inputs = 0 V		20*		20*	pF

^{*} Guaranteed by design; not tested. † Not included in Group A tests.

Notes: 1. ICC is measured in a static condition with outputs in the worst-case condition with all outputs unloaded.

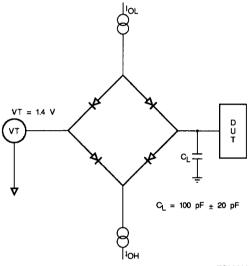
SWITCHING TEST INPUT/OUTPUT WAVEFORM



WF006490

AC testing inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0." Timing measurements are made at 2.0 V for a logic "1" and 0.8 V for a logic "0."

SWITCHING TEST CIRCUIT



TC003851

This test circuit is the dynamic load of a Teradyne J941.

SWITCHING CHARACTERISTICS over operating range (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted) (Note 4)

Symbol Description	Parameter	<u> </u>		8	251	Am9551		
AR	Symbol			Min.	Max.	Min.	Max.	Unit
CA	tAR	CS, C/D Stable to READ LOW Setup Time		50	 	50	 	ns
ICY Clock Period 0.420 1.35 0.380 1.35 LoF READ HIGH to Data Bus Off Delay 25 200 25 200 LoTX TXC LOW to TXD Delay 1.0 1.0 1.0 LDW Data to WRITE HIGH Setup Time 200 150 LES External SYNDET to RxC LOW Setup Time 16 16 LHRX Sampling Pulse to Rx Data Hold Time (Note 5) 2.0 2.0 2.0 LHRX Sampling Pulse to Rx Data Hold Time (Note 5) 2.0 3.0 30 30 LW Clock Pulse Width 220 0.6tcy 175 0.	t _{AW}	CS, C/D Stable to WRITE LOW Setup Time		20		20		ns
tcy Clock Period 0.420 1.35 0.380 1.35 tbF READ HIGH to Data Bus Off Delay 25 200 25 200 tbTx TXC LOW to TxD Delay 1.0 1.0 1.0 tbW Data to WRITE HIGH Setup Time 200 150 tls External SYNDET Delay 20 2.0 tls Data Bit (Center) to Internal SYNDET Delay 30 30 tbW Clock Pulse Width 220 0.61cy 175 0.6tcy tbA READ HIGH to CS, C/D Hold Time 5.0 5.0 5.0 5.0 tbA READ LIGH to CS, C/D Hold Time 1x Baud Rate 1 15 15 tbA READ LIGH to CS, C/D Hold Time 1x Baud Rate 1 1 1 tbAD Receiver Clock HIGH Time 1x Baud Rate 12 12 12 tbAD Receiver Clock LOW Time 1x Baud Rate 1 1 1 tbAD Time Between WRITE Pulses During Initialization (Note 1) 6.0 6.0	tcr	DSR, CTS to READ LOW Setup Time			16	 	16	tcy
Top In Pack High High to Data Bus Off Delay 25 200 25 200 In Tox LOW to TxD Delay 1.0 1.0 1.0 1.0 1.0 In Word Data to WRITE High Setup Time 200 150 1.0 1.0 1.0 Is Set External SYNDET to RxC LOW Setup Time 16	tcy			0.420	1.35	0.380		μs
Tox TxC LOW to TxD Delay 1.0 1.0 1.0 tow Data to WRITE HIGH Setup Time 200 150 150 Les External SYNDET to RxC LOW Setup Time 16 16 16 LHRX Sampling Pulse to Rx Data Hold Time (Note 5) 2.0 2.0 2.0 ts Data Bit (Center) to Internal SYNDET Delay 30 30 30 tsW Clock Pulse Width 220 0.6tcy 175 0.6tcy tRA READ HIGH to CS, C/D Hold Time 5.0 5.0 5.0 150 tRPD RECEIVER Clock HIGH Time 1x Baud Rate 1 15 15 tRPD Receiver Clock LOW Time 1x Baud Rate 1 1 1 1 tRPW Receiver Clock LOW Time 1x Baud Rate 1 1 1 1 1 tRR READ Pulse Width 430 380 3 3 3 3 3 3 3 3 3 3 3 2 1 1<	tDF	READ HIGH to Data Bus Off Delay		25	200		+	ns
Data DWRITE HIGH Setup Time	t _{DTx}	TxC LOW to TxD Delay			1.0	 		μs
External SYNDET to RxC LOW Setup Time	t _{DW}	Data to WRITE HIGH Setup Time		200	1	150	1.0	ns
HHRX Sampling Pulse to Rx Data Hold Time (Note 5) 2.0 2.0 3.0 </td <td>tES</td> <td>External SYNDET to RxC LOW Setup Time</td> <td>9</td> <td></td> <td> </td> <td></td> <td> </td> <td>+</td>	tES	External SYNDET to RxC LOW Setup Time	9		 		 	+
ts Data Bit (Center) to Internal SYNDET Delay toW Clock Pulse Width READ HIGH to CS, C/D Hold Time tro READ LOW to Data Bus On Delay tripo Receiver Clock HIGH Time 1x Baud Rate 1 15 16x 8 64x Baud Rate 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	tHRx	Sampling Pulse to Rx Data Hold Time (No	te 5)	2.0	 	 		tc\ μs
Clock Pulse Width 220	t _{IS}	Data Bit (Center) to Internal SYNDET Dela	у		30	1-2.0	30	— <u> </u>
READ HIGH to CS, C/D Hold Time 5.0, 5.0 5.0	tφW	Clock Pulse Width		220	ļ	175		t _{CY}
READ LOW to Data Bus On Delay	t _{RA}	READ HIGH to CS, C/D Hold Time			0.04,7		O.GICY	
Table Tabl	t _{RD}	READ LOW to Data Bus On Delay			350	3.0	250	ns
Transmitter Clock LOW Time			1x Baud Rate		1	15	230	ns
Transmitter Clock LOW Time Transmitter Clock LOW Time Transmitter Clock LOW Time Transmitter Clock Frequency Transmi	^t RPD	Receiver Clock HIGH Time				+	 	tcy
Tansmitter Clock LOW Time 16x & 64x 8aud Rate 1			Baud Rate	3	İ	3		
Transmitter Clock LOW Transmitter Clock LOW Transmitter Clock Frequency Transmitter Cloc	topw	Beceiver Clock LOW Time	1x Baud Rate	12		12		tcy
tRV Time Between WRITE Pulses During Initialization (Note 1) 6.0 6.0 t tRx Data Bit (Center) to RxRDY Delay 20 20 t tSRx Rx Data to Sampling Pulse Setup Time (Note) 2.0 2.0 2.0 tTPD Transmitter Clock HiGH Time Baud Rate 15 15 tTPW Transmitter Clock LOW Time 1x Baud Rate 12 12 tTPW Transmitter Clock LOW Time 1x Baud Rate 1 1 tTX Data Bit (Center) Tx Dx Delay 16 16 16 tTx Data Bit (Center) Tx Dx Delay 16 16 16 tTx Data Bit (Center) Tx Dx Delay 16 16 16 16 tTx Data Bit (Center) Tx Dx Delay 16 16 16 16 tTx Data Bit (Center) Tx Dx Delay 16 16 16 16 tTx Data Bit (Center) Tx Dx Delay 16 16 16 16 tTx Data Bit (Center) Tx Dx Dx Delay 16 16	THPW NO	HOCEWEI CIOCK FOW TIME		1		1		
Transmitter Clock HIGH Time Transmitter Clock LOW Time Transmitter Clock Company Transmitter Clock Frequency	trr		4.3	430		380		ns
tSRx Rx Data to Sampling Pulse Setup Time (No) 2.0 2.0 2.0 1 tTPD Transmitter Clock HIGH Time Baud Rate 15 15 15 tTPW Transmitter Clock LOW three 1x Baud Rate 12 12 12 tTX Data Bit (Center) Delay 16 16 16 16 tTXE Data Bit (Center) MPTY Delay 16 <td>t_{RV}</td> <td>Time Between WRITE Pulses During Initializ (Note 1)</td> <td>zation</td> <td>6.0</td> <td></td> <td>6.0</td> <td></td> <td>tcy</td>	t _{RV}	Time Between WRITE Pulses During Initializ (Note 1)	zation	6.0		6.0		tcy
Transmitter Clock HIGH Time Baud Rate 15 15 15	t _{Rx}	Data Bit (Center) to RxRDY Delay	- W		20		20	tcy
Transmitter Clock HIGH Time	tSRx	Rx Data to Sampling Pulse Setup Time (No	3	2.0		2.0		μS
Transmitter Clock LOW Tipe		Transmitter Clock HIGH Time 16x & 64x	Baud Rate	15				tcy
tTpW Transmitter Clock LOW the Baud Rate 1	^t TPD			3		3		
Transmitter Clock LOW Teamsmitter Clock Low Team			1x Baud Rate	12		12		<u> </u>
trxE Data Bit (Center) to the MPTY Delay 16	TPW	Transmitter Clock LOW Time		1		1		tcy
trxE Data Bit (Center) MPTY Delay 16 t <th< td=""><td>t_{TX}</td><td>145, 165, 16, 169</td><td></td><td></td><td>16</td><td></td><td>16</td><td>tcy</td></th<>	t _{TX}	145, 165, 16, 169			16		16	tcy
twa WRITE HIGH to CS, 7/D Hold Time 20 20 r twc WRITE HIGH to TXE, DTR, RTS Delay 16 16 temporaria two WRITE HIGH to Data Hold Time 40 40 r tww WRITE Pulse Width 430 380 r fRx Receiver Clock Frequency 1x Baud Rate DC 56 DC 56 fTx Transmitter Clock Frequency 1x Baud Rate DC 520 DC 520 fTx Transmitter Clock Frequency 1x Baud Rate DC 56 DC 56 ftx Baud Rate DC 56 DC 56	t _{TxE}				16			tcy
twc WRITE HIGH to TXE, DTR, RTS Delay 16 16 type two WRITE HIGH to Data Hold Time 40 40 r tww WRITE Pulse Width 430 380 r fRx Receiver Clock Frequency 1x Baud Rate DC 56 DC 56 fRx Baud Rate DC 520 DC 520 fTx Transmitter Clock Frequency 1x Baud Rate DC 56 DC 56 fTx Transmitter Clock Frequency 1x Baud Rate DC 56 DC 56	t _{WA}	WRITE HIGH to CS, C/D Hold Time		20		20	- 1	ns
two WRITE HIGH to Data Hold Time 40 40 r tww WRITE Pulse Width 430 380 r fRx Receiver Clock Frequency 1x Baud Rate DC 56 DC 56 16x & 64x Baud Rate DC 520 DC 520 bc fTx Transmitter Clock Frequency 1x Baud Rate DC 56 DC 56 f0x & 64x DC 56 DC 56 kl	twc	WRITE HIGH to TxE, DTR, RTS Delay			16		16	tcy
tww WRITE Pulse Width 430 380 r f _{Rx} Receiver Clock Frequency 1x Baud Rate DC 56 DC 56 16x & 64x Baud Rate DC 520 DC 520 bc f _{Tx} Transmitter Clock Frequency 1x Baud Rate DC 56 DC 56 16x & 64x DC 56 DC 56 bc	two	* · · · · · · · · · · · · · · · · · · ·		40		40		ns
In the contract of the	tww	WRITE Pulse Width	· · · · · · · · · · · · · · · · · · ·	430				ns
Receiver Clock Frequency		Receiver Clock Frequency	1x Baud Rate		56		56	kHz
Transmitter Clock Frequency 16x & 64x DC CO	f _{Rx}		16x & 64x	-+-+				
Transmitter Clock Frequency	T T			DC	56	DC	56	kHz
	f⊤x	Transmitter Clock Frequency	16x & 64x					

Notes: 1. This time period between write pulses is specified for initialization purposes only when MODE, SYNC 1, SYNC 2, COMMAND, and first DATA BYTE are written into the Am9551. Subsequent writing of both COMMAND and DATA are only allowed when TxRDY = 1. t_{RV} after internal Reset = 8 ° t_{CY}.

2. Reset Pulse Width = 6t_{CY} Min.

Switching Characteristics parameters are listed in alphabetical order.
 Clock Rise and Fall times are controlled by the Teradyne J941 tester. Measurement of typical signals generated by the J941 showed t_R = t_F = 5 ns.
 Sampling pulse is internal and not tested; guaranteed by design.