8251/Am9551

Programmable Communication Interface
iAPX86 Family
MILITARY INFORMATION

DISTINCTIVE CHARACTERISTICS

- Separate control and transmit register input buffers
- Synchronous or asynchronous serial data transfer
- Parity, overrun, and framing errors detected
- Half- or full-duplex signaling
- Character length of 5, 6, 7, or 8 bits
- Internal or external synchronization
- Odd parity, even parity, or no parity bit
- Modem interface controlled by processor
  - Programmable Sync pattern
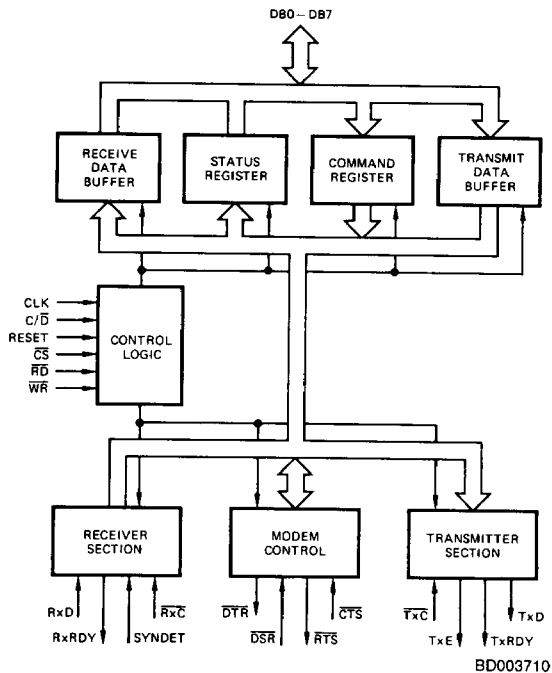 - Fully TTL-compatible logic levels

GENERAL DESCRIPTION

The 8251/Am9551 is a programmable serial data communication interface that provides a Universal Synchronous/Asynchronous Receiver/Transmitter (USART) function. It is normally used as a peripheral device for an associated processor and may be programmed by the processor to operate in a variety of standard serial communication formats.

The device accepts parallel data from the CPU, formats and serializes the information based on its current operating mode, and then transmits the data as a serial bit stream.

Simultaneously, serial data can be received, converted into parallel form, deformatted, and then presented to the CPU. The USART can operate in an independent full-duplex mode.
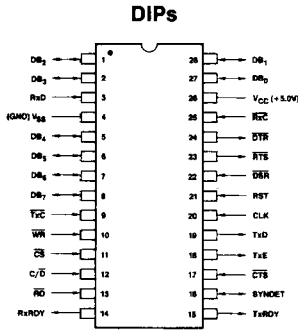
Data, control, operation, and format options are all selected by commands from an associated processor. This provides an unusual degree of flexibility and allows the 8251/Am9551 to service a wide range of communication disciplines and applications.

BLOCK DIAGRAM

BD003710

www.DataSheet4U.com

CONNECTION DIAGRAM
Top View

DIPs

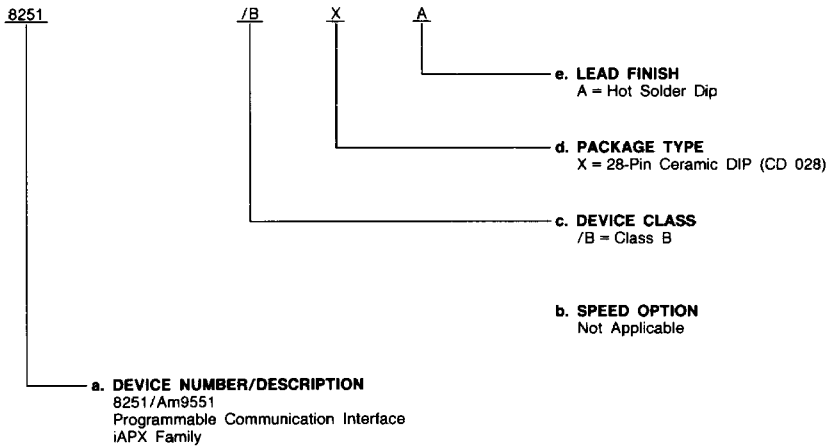|				
DB$_2$	1		28	DB$_1$
DB$_3$	2		27	DB$_0$
RxD	3		26	V$_{CC}$ (+5.0V)
(GND) V$_{SS}$	4		25	RxC
DB$_4$	5		24	DTR
DB$_5$	6		23	RTS
DB$_6$	7		22	DSR
DB$_7$	8		21	RST
TxC	9		20	CLK
WR	10		19	TxD
CS	11		18	TxE
C/D	12		17	CTS
RD	13		16	SYNDET
RxRDY	14		15	TxRDY

CD005482

Note: Pin 1 is marked for orientation.

MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of:
a. Device Number
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish

8251   /B X A

e. LEAD FINISH
A = Hot Solder Dip

d. PACKAGE TYPE
X = 28-Pin Ceramic DIP (CD 028)

c. DEVICE CLASS
/B = Class B

b. SPEED OPTION
Not Applicable

a. DEVICE NUMBER/DESCRIPTION
8251/Am9551
Programmable Communication Interface
iAPX Family

Valid Combinations	
8251	/BXA
AM9551	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups
1, 2, 3, 7, 8, 9, 10, 11.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature .... −65°C to +150°C
V_{CC} with Respect to V_{SS} .... −0.5 to +7.0 V
All Signal Voltages
  with Respect to V_{SS} .... −0.5 V to +7.0 V
Power Dissipation .... 1.0 W

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Military (M) Devices
  Temperature (T_C) .... −55 to +125°C
  Supply Voltage (V_{CC}) .... 5 V ± 10%

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions	8251 Min.	8251 Max.	Am9551 Min.	Am9551 Max.	Unit
V_{OH}	Output HIGH Voltage	$I_{OH} = -200\ \mu A$, $V_{CC} = 4.5$ V			2.4		V
		$I_{OH} = -100\ \mu A$	2.4				
V_{OL}	Output LOW Voltage	$I_{OL} = 1.6$ mA, $V_{CC} = 4.5$ V		0.45		0.45	V
V_{IH}	Input HIGH Voltage	$V_{CC} = 5$ V ± 10%	2.2	V_{CC}^*	2.2	V_{CC}^*	V
V_{IL}	Input LOW Voltage	$V_{CC} = 5$ V ± 10%	−0.5*	0.8	−0.5*	0.8	V
I_{LI}	Input Load Current	$V_{CC} = 5.5$ V, 5 V 0 V		±10		±10	μA
I_{DL}	Data Bus Leakage	$V_{OUT} = 0.45$ V, $V_{CC} = 5.5$ V		−50		−50	μA
		$V_{OUT} = 5.5$ V, $V_{CC} = 5.5$ V		10		10	
I_{CC}	V_{CC} Supply Current			120		120	mA
C_O †	Output Capacitance			15*		15*	pF
C_I †	Input Capacitance	$fc = 1.0$ MHz, Inputs = 0 V		10*		10*	pF
$C_{I/O}$ †	I/O Capacitance			20*		20*	pF

* Guaranteed by design; not tested.
† Not included in Group A tests.

Notes: 1. I_{CC} is measured in a static condition with outputs in the worst-case condition with all outputs unloaded.
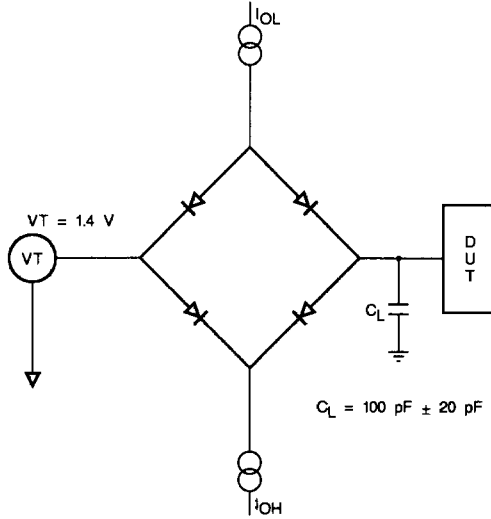
SWITCHING TEST INPUT/OUTPUT WAVEFORM

2.4

2.0 ← **TEST POINTS** → 2.0

0.8 → → 0.8

0.45
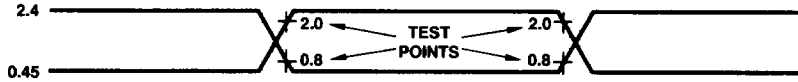
WF006490

AC testing inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0." Timing measurements are made at 2.0 V for a logic "1" and 0.8 V for a logic "0."

SWITCHING TEST CIRCUIT

I_{OL}

$V_T = 1.4$ V

VT

DUT

C_L

$C_L = 100$ pF $\pm$ 20 pF

I_{OH}

TC003851

This test circuit is the dynamic load of a Teradyne J941.

SWITCHING CHARACTERISTICS over operating range (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted) (Note 4)

Parameter Symbol	Parameter Description		8251 Min.	8251 Max.	Am9551 Min.	Am9551 Max.	Unit
tAR	CS, C/D Stable to READ LOW Setup Time		50		50		ns
tAW	CS, C/D Stable to WRITE LOW Setup Time		20		20		ns
tCR	DSR, CTS to READ LOW Setup Time			16		16	tCY
tCY	Clock Period		0.420	1.35	0.380	1.35	µs
tDF	READ HIGH to Data Bus Off Delay		25	200	25	200	ns
tDTx	TxC LOW to TxD Delay			1.0		1.0	µs
tDW	Data to WRITE HIGH Setup Time		200		150		ns
tES	External SYNDET to RxC LOW Setup Time		16		16		tCY
tHRx	Sampling Pulse to Rx Data Hold Time (Note 5)		2.0		2.0		µs
tIS	Data Bit (Center) to Internal SYNDET Delay			30		30	tCY
tφW	Clock Pulse Width		220	0.6tCY	175	0.6tCY	ns
tRA	READ HIGH to CS, C/D Hold Time		5.0		5.0		ns
tRD	READ LOW to Data Bus On Delay			350		250	ns
tRPD	Receiver Clock HIGH Time	1x Baud Rate	15		15		tCY
		16x & 64x Baud Rate	3		3		
tRPW	Receiver Clock LOW Time	1x Baud Rate	12		12		tCY
		16x & 64x Baud Rate	1		1		
tRR	READ Pulse Width		430		380		ns
tRV	Time Between WRITE Pulses During Initialization (Note 1)		6.0		6.0		tCY
tRx	Data Bit (Center) to RxRDY Delay			20		20	tCY
tSRx	Rx Data to Sampling Pulse Setup Time (Note 5)		2.0		2.0		µS
tTPD	Transmitter Clock HIGH Time	1x Baud Rate	15		15		tCY
		16x & 64x Baud Rate	3		3		
tTPW	Transmitter Clock LOW Time	1x Baud Rate	12		12		tCY
		16x & 64x Baud Rate	1		1		
tTX	Data Bit (Center) to TxRDY Delay			16		16	tCY
tTxE	Data Bit (Center) to TxEMPTY Delay			16		16	tCY
tWA	WRITE HIGH to CS, C/D Hold Time		20		20		ns
tWC	WRITE HIGH to TxE, DTR, RTS Delay			16		16	tCY
tWD	WRITE HIGH to Data Hold Time		40		40		ns
tWW	WRITE Pulse Width		430		380		ns
fRx	Receiver Clock Frequency	1x Baud Rate	DC	56	DC	56	kHz
		16x & 64x Baud Rate	DC	520	DC	520	
fTx	Transmitter Clock Frequency	1x Baud Rate	DC	56	DC	56	kHz
		16x & 64x Baud Rate	DC	520	DC	520	

Notes: 1. This time period between write pulses is specified for initialization purposes only when MODE, SYNC 1, SYNC 2, COMMAND, and first DATA BYTE are written into the Am9551. Subsequent writing of both COMMAND and DATA are only allowed when TxRDY = 1. tRV after internal Reset = 8 · tCY.
2. Reset Pulse Width = 6tCY Min.
3. Switching Characteristics parameters are listed in alphabetical order.
4. Clock Rise and Fall times are controlled by the Teradyne J941 tester. Measurement of typical signals generated by the J941 showed tR = tF = 5 ns.
5. Sampling pulse is internal and not tested; guaranteed by design.