Preliminary

WCMA4016U1X

256K x 16 Static RAM

Features

- **Low voltage range: 2.7V–3.6V**
- **Ultra-low active, standby power**
- **Easy memory expansion with $\overline{CE_1}$ and CE_2 and $\overline{OE}$ features**
- **TTL-compatible inputs and outputs**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**

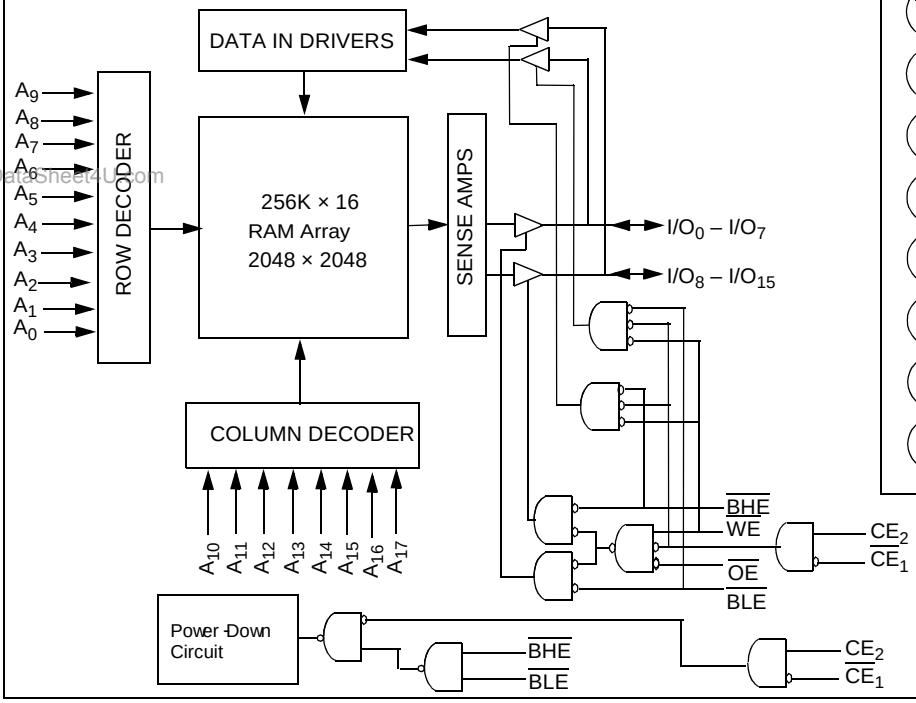
Functional Description[1]

The WCMA4016U1X is a high-performance CMOS static RAM organized as 262,144 words by 16 bits. This device features advanced circuit design to provide ultra-low active current and standby current. This is ideal for providing more battery life in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption by 99% when addresses are not toggling. The device can also be put into standby mode when deselected ($\overline{CE_1}$ HIGH or CE_2 LOW or both $\overline{BHE}$ and $\overline{BLE}$ are HIGH). The input/output pins (I/O_0 through I/O_{15}) are placed in a high-impedance state when: deselected ($\overline{CE_1}$HIGH or CE_2 LOW), outputs are disabled ($\overline{OE}$ HIGH), both Byte High Enable and Byte Low Enable are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or during a write operation ($\overline{CE_1}$ LOW, CE_2 HIGH and $\overline{WE}$ LOW).

Writing to the device is accomplished by taking Chip Enables ($\overline{CE_1}$ LOW and CE_2 HIGH) and Write Enable ($\overline{WE}$) input LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O_0 through I/O_7), is written into the location specified on the address pins (A_0 through A_{18}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{18}).

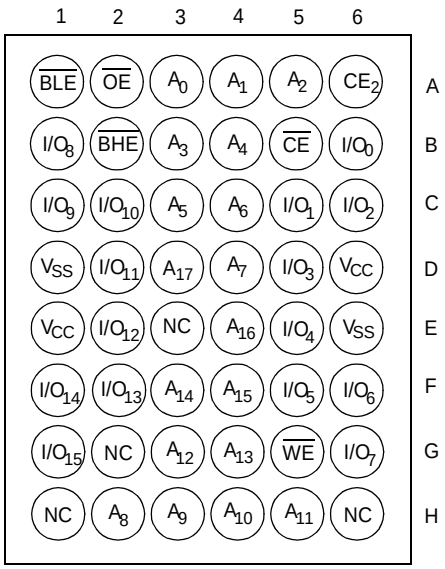
Reading from the device is accomplished by taking Chip Enables ($\overline{CE_1}$ LOW and CE_2 HIGH) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins will appear on I/O_0 to I/O_7. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory will appear on I/O_8 to I/O_{15}. See the truth table at the back of this datasheet for a complete description of read and write modes.

Logic Block Diagram



Pin Configurations

FBGA (Top View)



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied..... –55°C to +125°C

Supply Voltage to Ground Potential..... –0.5V to +4.6V

DC Voltage Applied to Outputs in High Z State[1] .....–0.5V to V_{CC} + 0.5V

DC Input Voltage[1]..... –0.5V to V_{CC} + 0.5V

Output Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage..... >2100V (per MIL-STD-883, Method 3015)

Latch-Up Current..... >200 mA

Operating Range

Device	Range	Ambient Temperature	V_{CC}
WCMA4016U1X	Industrial	–40°C to +85°C	2.7V to 3.6V

Product Portfolio

Product	V_{CC} Range			Power	Speed (ns)	Power Dissipation (Industrial)			
						Operating (I_{CC})		Standby (I_{SB2})	
	$V_{CC(min.)}$	$V_{CC(typ.)}$[2]	$V_{CC(max.)}$			Typ.[2]	Maximum	Typ.[2]	Maximum
WCMA4016U1X	2.7V	3.0V	3.6V	LL	70	7 mA	15 mA	2 µA	20 µA

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions			WCMA4016U1X			Unit
					Min.	Typ.[2]	Max.	
V_{OH}	Output HIGH Voltage	I_{OH} = –1.0 mA	V_{CC} = 2.7V		2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1 mA	V_{CC} = 2.7V				0.4	V
V_{IH}	Input HIGH Voltage		V_{CC} = 3.6V		2.2		V_{CC} + 0.5V	V
V_{IL}	Input LOW Voltage		V_{CC} = 2.7V		–0.5		0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}			–1	±1	+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled			–1	+1	+1	µA
I_{CC}	V_{CC} Operating Supply Current	I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$, CMOS Levels	V_{CC} = 3.6V			7	15	mA
		I_{OUT} = 0 mA, f = 1 MHz, CMOS Levels				1	2	mA
I_{SB1}	Automatic $\overline{CE}$ Power-Down Current—CMOS Inputs	$\overline{CE}_1$ ≥ V_{CC}–0.3V, CE_2≤ 0.3V V_{IN}≥V_{CC}–0.3V, V_{IN}≤0.3V) f = f_{MAX} (Address and Data Only), f = 0 ($\overline{OE}$, $\overline{WE}$, $\overline{BHE}$ and $\overline{BLE}$), V_{CC}=3.60V		LL		2	20	µA
I_{SB2}	Automatic $\overline{CE}$ Power-Down Current—CMOS Inputs	$\overline{CE}_1$ ≥ V_{CC} – 0.3V or CE_2 ≤ 0.3V, V_{IN} ≥ V_{CC} – 0.3V or V_{IN} ≤ 0.3V, f = 0, V_{CC} = 3.60V		LL		2	20	µA

Notes:
1. $V_{IL(min.)}$ = –2.0V for pulse durations less than 20 ns.
2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = $V_{CC(typ.)}$, T_A = 25°C.

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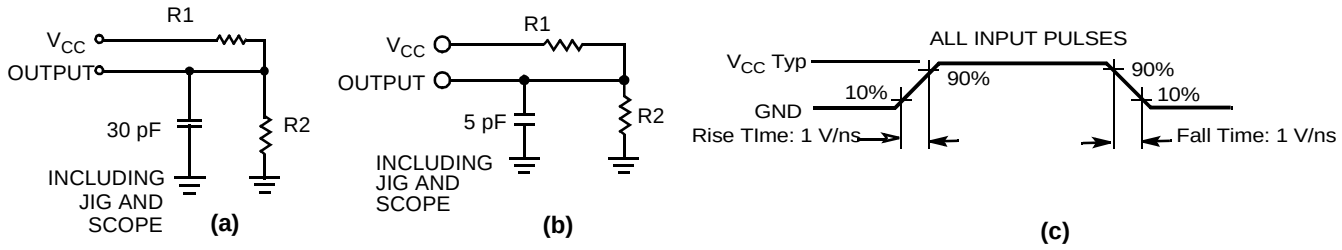
Capacitance[3]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, $V_{CC} = V_{CC(typ.)}$	6	pF
C_{OUT}	Output Capacitance		8	pF

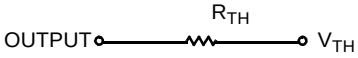
Thermal Resistance

Description	Test Conditions	Symbol	BGA	Units
Thermal Resistance (Junction to Ambient)[3]	Still Air, soldered on a 4.25 x 1.125 inch, 4-layer printed circuit board	Θ_{JA}	55	°C/W
Thermal Resistance (Junction to Case)[3]		Θ_{JC}	16	°C/W

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



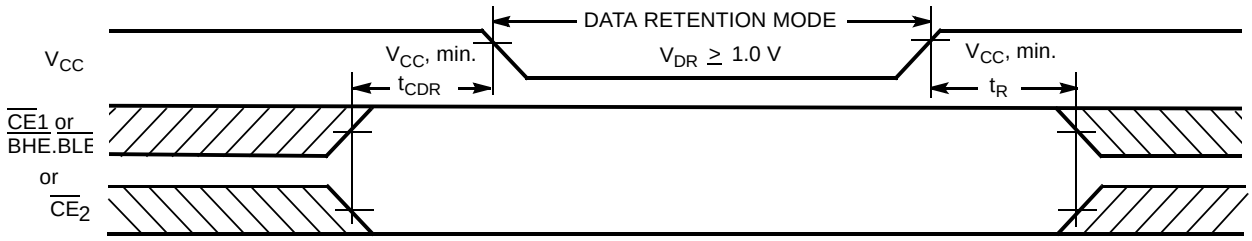
Parameters	3.0V	Unit
R1	1103	Ω
R2	1554	Ω
R_{TH}	645	Ω
V_{TH}	1.75V	V

Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions		Min.	Typ.[2]	Max.	Unit
V_{DR}	V_{CC} for Data Retention			1.0		3.6	V
I_{CCDR}	Data Retention Current	V_{CC}= 1.0V $\overline{CE}_1 \geq V_{CC} - 0.3V$, $CE_2 \leq 0.2V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$	L		1	10	µA
			LL				
t_{CDR}[3]	Chip Deselect to Data Retention Time			0			ns
t_R[4]	Operation Recovery Time			70			ns

Note:
3. Tested initially and after any design or process changes that may affect these parameters.
4. Full Device AC operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)}$ > 10 µs or stable at $V_{CC(min.)}$ >10 µs.

Data Retention Waveform[5]



Switching Characteristics Over the Operating Range[6]

Parameter	Description	70 ns		Unit
		Min.	Max.	
READ CYCLE				
t_{RC}	Read Cycle Time	70		ns
t_{AA}	Address to Data Valid		70	ns
t_{OHA}	Data Hold from Address Change	10		ns
t_{ACE}	$\overline{CE}_1$ LOW and CE_2 HIGH to Data Valid		70	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		35	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[7, 9]	5		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[9]		25	ns
t_{LZCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to Low Z[7]	10		ns
t_{HZCE}	$\overline{CE}_1$ HIGH and CE_2 LOW to High Z[7, 9]		25	ns
t_{PU}	$\overline{CE}_1$ LOW and CE_2 HIGH to Power-Up	0		ns
t_{PD}	$\overline{CE}_1$ HIGH and CE_2 LOW to Power-Down		70	ns
t_{DBE}	$\overline{BHE}$ / $\overline{BLE}$ LOW to Data Valid		70	ns
t_{LZBE}[8]	$\overline{BHE}$ / $\overline{BLE}$ LOW to Low Z	5		ns
t_{HZBE}	$\overline{BHE}$ / $\overline{BLE}$ HIGH to High Z		25	ns
WRITE CYCLE[10, 11]				
t_{WC}	Write Cycle Time	70		ns
t_{SCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to Write End	60		ns
t_{AW}	Address Set-Up to Write End	60		ns
t_{HA}	Address Hold from Write End	0		ns
t_{SA}	Address Set-Up to Write Start	0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	50		ns

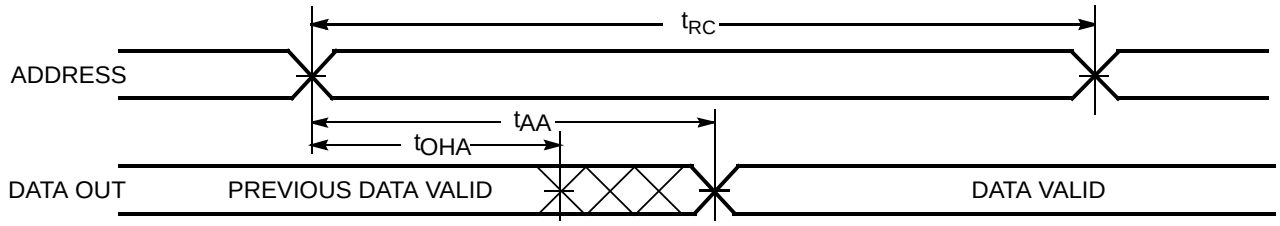
Notes:
5. $\overline{BHE}.\overline{BLE}$ is the AND of both $\overline{BHE}$ and $\overline{BLE}$. Chip can be deselected by either disabling the chip enable signals or by disabling both $\overline{BHE}$ and $\overline{BLE}$.
6. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to $V_{CC(typ.)}$, and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance.
7. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
8. If both byte enables are toggled together this value is 10ns
9. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
10. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
11. The minimum write cycle time for Write Cycle #3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

Switching Characteristics Over the Operating Range[6] (continued)

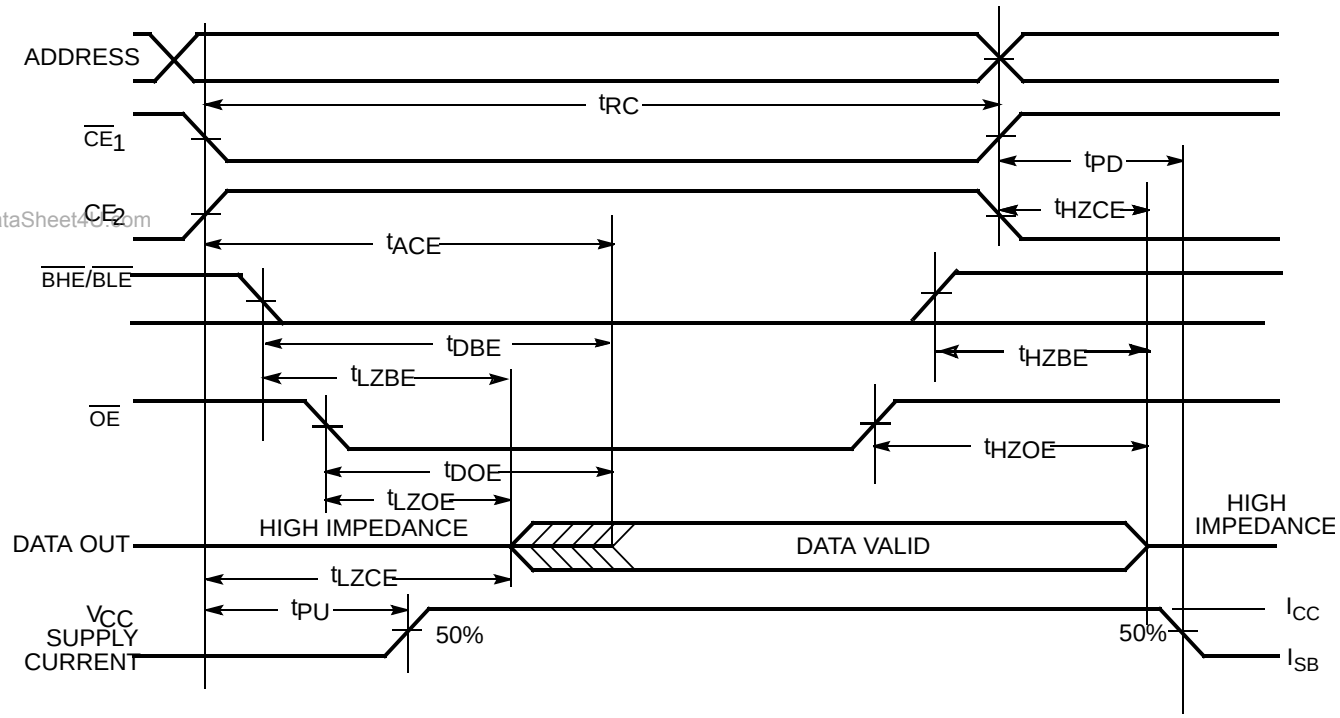
Parameter	Description	70 ns		Unit
		Min.	Max.	
t_{BW}	$\overline{BHE}$ / $\overline{BLE}$ Pulse Width	60		ns
t_{SD}	Data Set-Up to Write End	30		ns
t_{HD}	Data Hold from Write End	0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[7, 9]		25	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[7]	10		ns

Switching Waveforms

Read Cycle 1 (Address Transition Controlled)[12, 13]



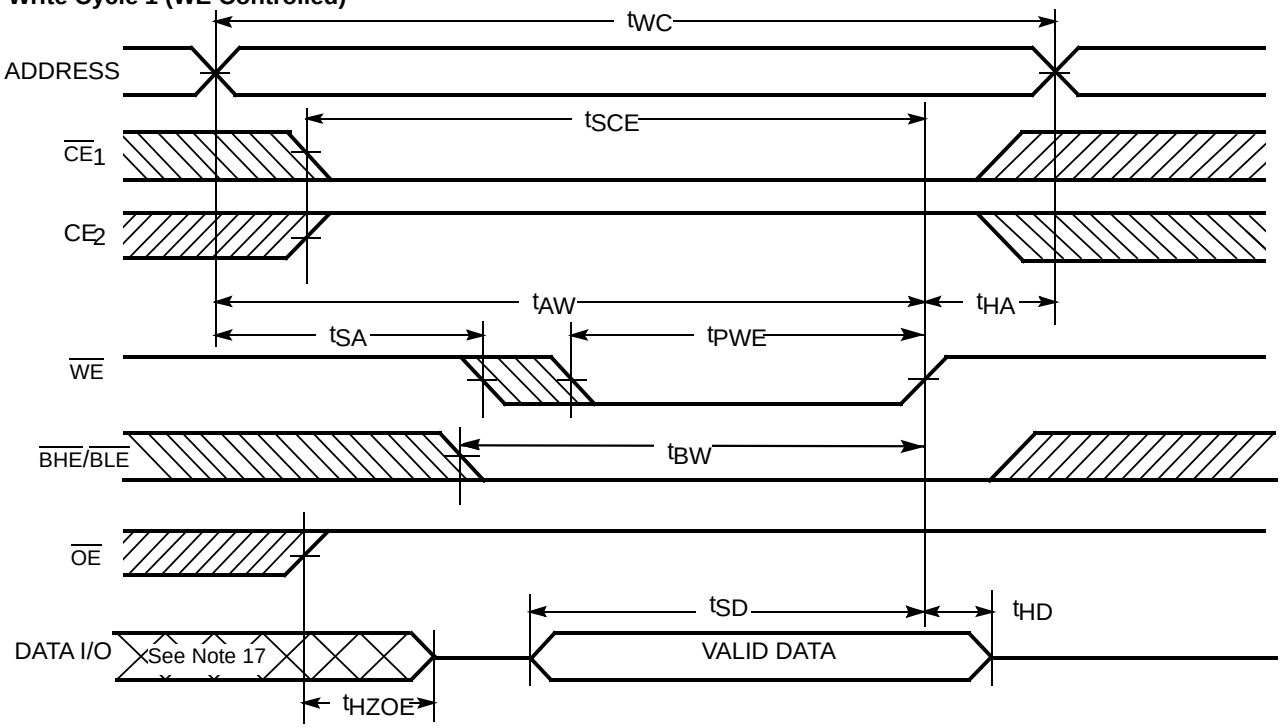
Read Cycle 2 ($\overline{OE}$ Controlled)[13, 14]



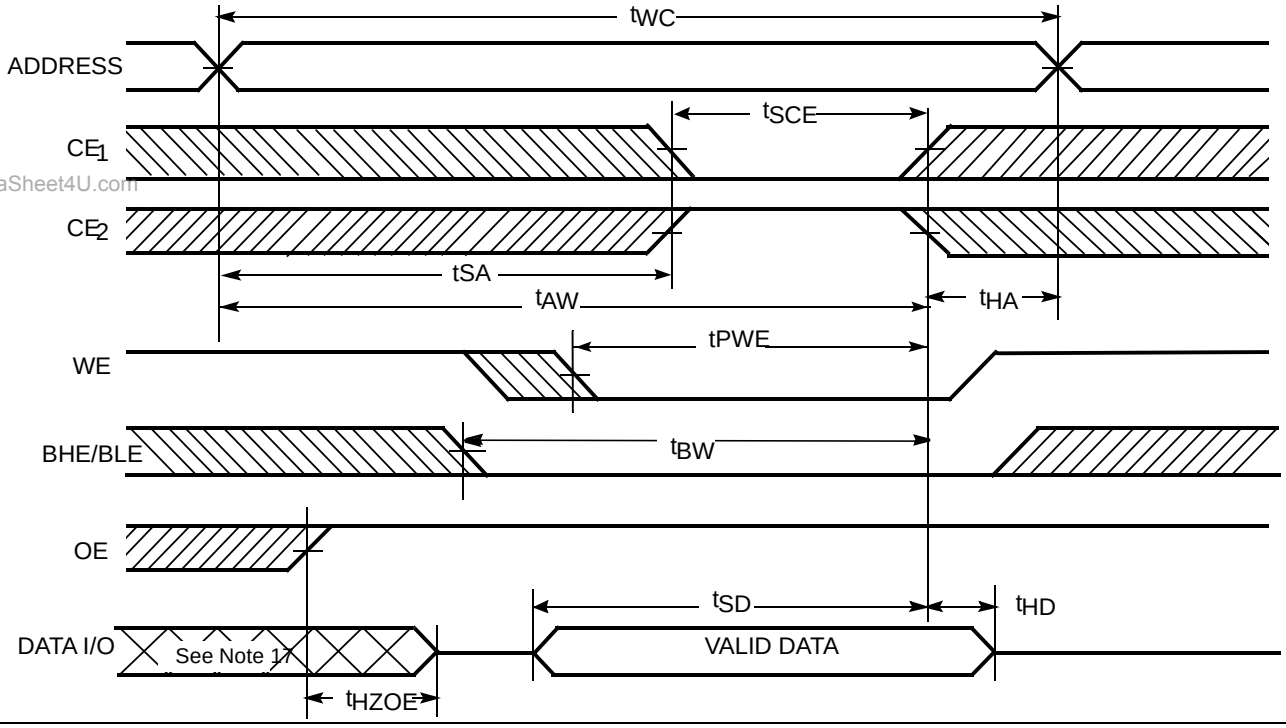
Notes:
12. $\overline{OE}$, $\overline{CE_1}$ = V_{IL}, $\overline{BHE}$ and/or $\overline{BLE}$ = V_{IL}, and CE_2 = V_{IH}.
13. $\overline{WE}$ is HIGH for read cycle.
14. Address valid prior to or coincident with $\overline{CE_1}$, $\overline{BHE}$, $\overline{BLE}$ transition LOW and CE_2 transition HIGH.

Switching Waveforms (continued)

Write Cycle 1 ($\overline{WE}$ Controlled)[10, 15, 16, 17]



Write Cycle 2 ($\overline{CE_1}$ or CE_2 Controlled)[10, 15, 16, 17]

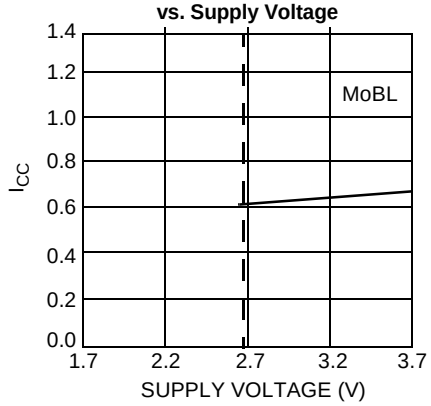


Notes:

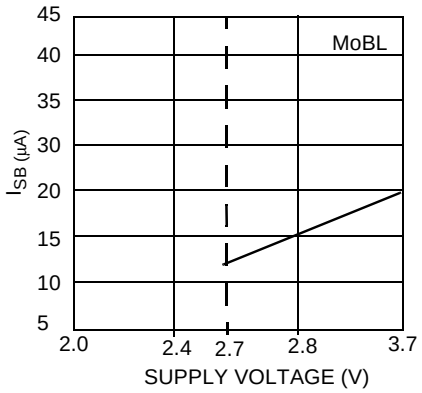
15. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
16. If $\overline{CE_1}$ goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE} = V_{IH}$, the output remains in a high-impedance state.
17. During this period, the I/Os are in output state and input signals should not be applied.

Typical DC and AC Characteristics

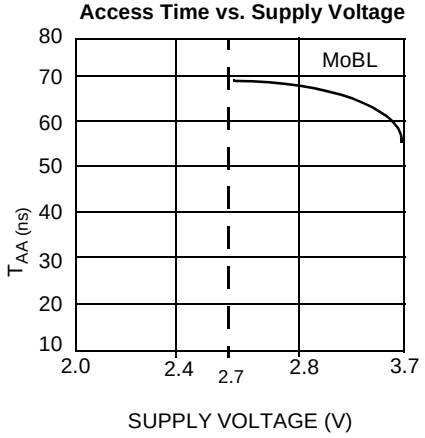
Normalized Operating Current vs. Supply Voltage



Standby Current vs. Supply Voltage



Access Time vs. Supply Voltage



Truth Table

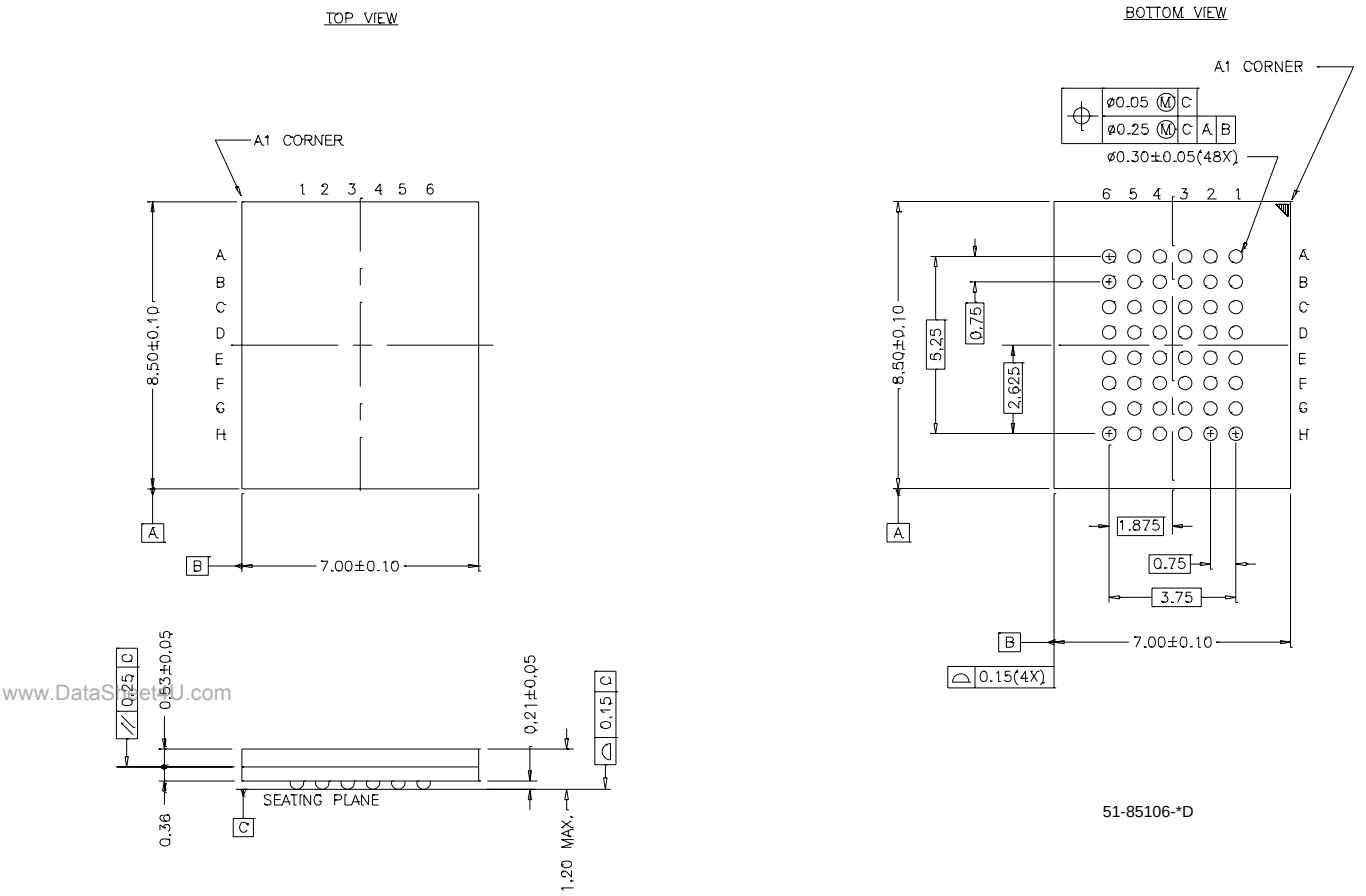
$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power
H	X	X	X	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
X	L	X	X	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
X	X	X	X	H	H	High Z	Deselect/Power-Down	Standby (I_{SB})
L	H	H	L	L	L	Data Out (I/O0 – I/O15)	Read	Active (I_{CC})
L	H	H	L	H	L	Data Out (I/O0 – I/O7); High Z (I/O8 – I/O15)	Read	Active (I_{CC})
L	H	H	L	L	H	High Z (I/O0 – I/O7); Data Out (I/O8 – I/O15)	Read	Active (I_{CC})
L	H	H	H	L	H	High Z	Output Disabled	Active (I_{CC})
L	H	H	H	H	L	High Z	Output Disabled	Active (I_{CC})
L	H	H	H	L	L	High Z	Output Disabled	Active (I_{CC})
L	H	L	X	L	L	Data In (I/O0 – I/O15)	Write	Active (I_{CC})
L	H	L	X	H	L	Data In (I/O0 – I/O7); High Z (I/O8 – I/O15)	Write	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
70	WCMA4016U1X-FF70	BA48	48-Ball Fine Pitch BGA	Industrial

Package Diagrams

48-Ball (7.00 mm x 8.5 mm x 1.2 mm) FBGA BA48B



Document History Page

Document Title: WCMA4016U1X 256K x 16 STATIC RAM Document Number:				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**		See ECN	AJU	New Data Sheet