INTERSIL

ICL8052/ICL7101
3½ Digit A/D Pair

FEATURES

- Guaranteed zero reading for 0 volts input
- Auto-zero; auto polarity
- 5pA input current typical
- Single reference voltage
- Latched parallel (full-time) BCD output for LCDs or data busing
- True polarity at zero count for precise null detection
- On-board clock and reference

ORDERING INFORMATION

Part	Temp. Range	Package	Order Number
8052	0°C to 70°C	14 pin plastic DIP	ICL8052CPD
8052	0°C to 70°C	14 pin ceramic DIP	ICL8052CDD
7101	0°C to 70°C	40 pin plastic DIP	ICL7101CPL
7101	0°C to 70°C	40 pin ceramic DIP	ICL7101CDL

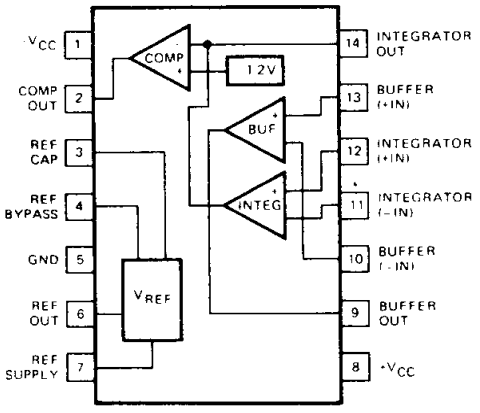
GENERAL DESCRIPTION

The 8052/7101 A/D Pair, with its parallel BCD outputs, is ideally suited for data processing applications or interfacing with 3½-digit Liquid Crystal Displays. No external circuitry is required to demultiplex the information. In addition, it has a "start/reset" input and "busy" output that allows easy synchronization to system requirements. The 8052/7101 provides 4½-digit accuracy in a 3½-digit format with typical system performance like 5pA input leakage, auto-zero to 10μV with less than 1μV/°C drift and Linearity to 0.002%.

The 8052/7101 A/D pair also features conversion rates from 10 seconds to 30 per second, making them ideally suited for a wide variety of applications.

CONNECTION DIAGRAM

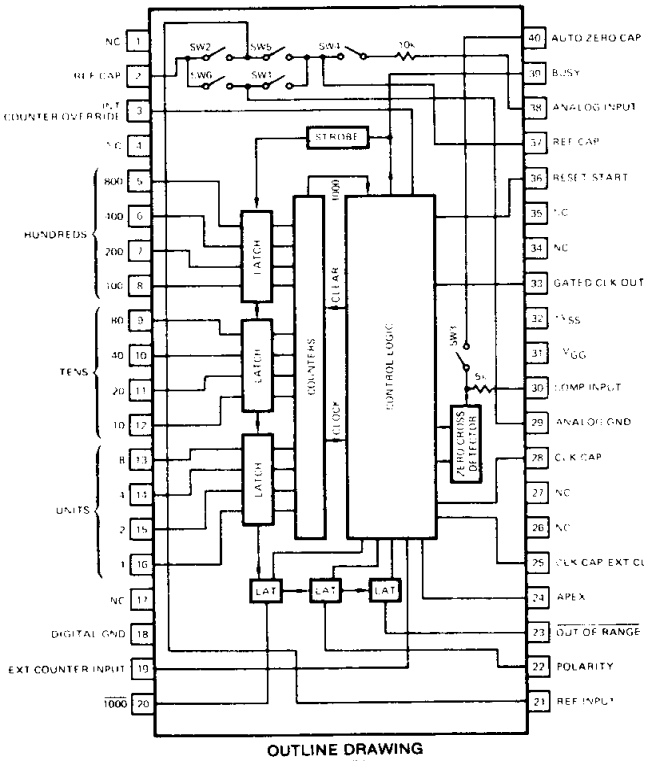
8052 Analog Signal Conditioner



OUTLINE DRAWINGS
DD, PD

CONNECTION DIAGRAM

7101 Digital Processor



OUTLINE DRAWING
DL, PL

ABSOLUTE MAXIMUM RATINGS

Power Dissipation (Note 1)	500mW
Storage Temperature	−65°C to +150°C

8052 ONLY

Supply Voltage	±18V
Differential Input Voltage	±6V
Input Voltage (Note 2)	±15V
Output Short Circuit Duration, All Outputs (Note 3)	Indefinite

Operating Temperature	0°C to +70°C
Lead Temperature (Soldering, 60 Sec.)	300°C

7101 ONLY

Source Current (I_S)	100mA
Drain Current (I_D)	100mA
Digital Inputs	5mA
V^+ to V^-	25V
Digital Input	V^- to V^+

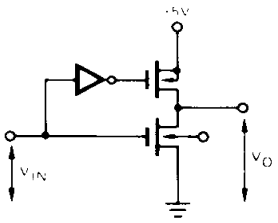
Note 1: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature below +70°C. For higher temperatures, derate 10mW/°C.

Note 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

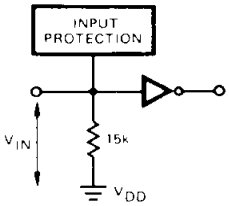
Note 3: Short circuit may be to ground or either supply. Rating applies to +70°C ambient temperature.

7101 ELECTRICAL CHARACTERISTICS ($V^+ = +5.0V$, $V^- = -15V$, $T_A = +25°C$ unless otherwise specified)

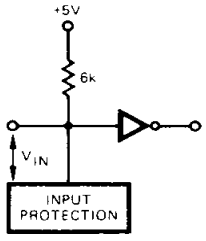
PARAMETER	SYMBOL	CONDITIONS	7101 MIN	7101 TYP	7101 MAX	UNITS
Clock Frequency	f_{IN}	C = 1500 pF		20		kHz
External Clock In	I_{INL}	V_{IN} = 0 V		0.35	1.0	mA
External Clock In	I_{INH}	V_{IN} = +5.0 V		0.35	1.0	mA
Reset/Start	I_{INL}	V_{IN} = 0 V		0.8	2.0	mA
Internal Counter Override External Counter Input	I_{INH}	V_{IN} = +5.0 V		0.35	1.0	mA
BCD	V_{OL}	I_{OL} = 1.6 mA		0.25	0.4	V
BCD	V_{OH}	I_{OH} = −200 μA	2.4	4.5		V
Out-of-Range	V_{OL}	I_{OL} = 3.2 mA		0.25	0.4	V
Out-of-Range	V_{OH}	I_{OH} = 400 μA	2.4	4.5		V
Polarity, Apex, Busy, $\overline{1000}$	V_{OL}	I_{OL} = 0.8 mA		0.25	0.4	
Polarity, Apex, Busy, $\overline{1000}$	V_{OH}	I_{OH} = −200 μA	2.4	4.5		V
Gated Clockout	V_{OL}	I_{OL} = 0.3 mA		0.25	0.4	V
Gated Clockout	V_{OH}	I_{OH} = −200 μA	2.4	4.5		V
Switches 1, 3, 4, 5, 6	$R_{DS(ON)}$			400		Ω
Switch 2	$R_{DS(ON)}$			2500		Ω
+5.0 V Supply Current	I_{CC}^+			15	25	mA
−15 V Supply Current	I_{CC}^-			3.0	5.0	mA



Output



External Counter Input
Internal Counter Override



Start/Reset

TYPICAL INPUT/OUTPUT SCHEMATICS

8052 ELECTRICAL CHARACTERISTICS (V_S = ±15V, T_A = +25°C unless otherwise specified)

CHARACTERISTICS	CONDITIONS	8052 MIN	8052 TYP	8052 MAX	UNITS
OPERATIONAL AMPLIFIER					
Input Offset Voltage	V_{CM} = 0V		20	50	mV
Input Current (either input)	V_{CM} = 0V		5	50	pA
Common-Mode Rejection Ratio	V_{CM} = ±10V	70	90		dB
Non-Linear Component of Common-Mode Rejection Ratio*	V_{CM} = ±2V		110		dB
Large Signal Voltage Gain	R_L = 10kΩ, V_{OUT} = ±10V	20,000			V/V
Slew Rate			6		V/μs
Unity Gain Bandwidth			1		MHz
Output Short-Circuit Current			20	50	mA
COMPARATOR AMPLIFIER					
Small-Signal Voltage Gain	R_L = 30kΩ		4000		V/V
Positive Output Voltage Swing		+12	+13		V
Negative Output Voltage Swing		-2.0	-2.6		V
VOLTAGE REFERENCE					
Output Voltage		1.5	1.75	2.0	V
Output Resistance			5		ohms
Temperature Coefficient			50		ppm
Supply Current Total			6	12	mA

*This is the only component that causes error in dual-slope converter.

SYSTEM ELECTRICAL CHARACTERISTICS

(V_{++} = +15V, V_+ = +5.0V, V_- = -15V, T_A = +25°C, Clock Frequency Set for 3 Reading/Sec)

CHARACTERISTICS	CONDITIONS	8052/7101 (1) MIN	8052/7101 (1) TYP	8052/7101 (1) MAX	UNIT
Zero Input Reading	V_{in} = 0.0V	-0.000	±0.000	+0.000	Digita Readir
Ratiometric Reading	$V_{in} \equiv V_{Ref.}$	+0.998	+1.000	+1.001	Digita Readir
Linearity over ± Full Scale (error off reading from best straight line)	$-2V \leq V_{in} \leq +2V$		0.1	1	Digita Count Error
Rollover error (Difference in reading for equal positive & negative voltage near full scale)	$-V_{in} \equiv +V_{in} \approx 2V$		0.1	1	Digita Count Error
Noise (P-P value not exceeded 95% of time)	V_{in} = 0V, Full scale = 200.0mV		0.2		Digita
	Full scale = 2.000V		0.05		Coun
Leakage Current into Input	V_{in} = 0V		5	30	pA
Zero Reading Drift	V_{in} = 0V, $0° \leq T_A \leq 70°C$		1	5	μV/°
Scale Factor Temperature Coefficient	V_{in} = +2V, $0° \leq T_A \leq 70°C$, (ext. ref. 0 ppm/°C)		3	15	ppm/°

(1) Tested in 3½ digit (2,000 count) circuit shown in Fig. 1 clock frequency 20kHz.

CIRCUIT DESCRIPTION

Figure 1 shows a typical circuit for a DVM. A minimum of external components is required since the chips have an on-board clock and a medium-quality (40ppm/°C) internal reference. The circuit also shows the switching required for two scale factors: 2.000V and 200.0mV full scale.

The system uses the time-proven dual-slope integration with all of its advantages; non-critical components, high rejection of noise and AC signals, non-critical clock frequency and true ratiometric readings. At the same time, it eliminates one of the basic disadvantages of dual-slope conversion: separate positive and negative reference sources. In this system, the negative reference is generated by charging the reference capacitor to the positive reference potential and then switching it into the circuit inverted when a negative reference is required. Due to the very low leakage and charge injection of the FET switches, the positive and negative references track each other to 10μV over a wide temperature range. This assures a very small error between positive and negative scale factor and, thus, excellent linearity from (+) full-scale to (-) full-scale (.002% typical).

4

The measurement cycle for the 8052/7101 has three phases. These are auto-zero, integrate input, and integrate reference. At the end of a measurement the system automatically reverts to the auto-zero mode until a new measurement is initiated. If an over-load has not occurred in the previous measurement, 10 milliseconds of auto-zero is sufficient to null any offsets to 10μV. At power on, or after an overload, 100 milliseconds is required to assure the auto-zero capacitor has charged to the correct value.

Start Conversion

Prior to conversion, the reset-start input must be held low to inhibit conversion (during auto-zero). Conversion is initiated by a positive transition on the start-reset line. (It must therefore return to the low state prior to completion of conversion in order to allow proper auto-zero function.) The positive transition generates a clear pulse which resets all internal logic (counters, etc.) and sets the clock enable, thus initiating the conversion sequence.

Integrate Input

During the first period, switch #4 is closed, (all others open), applying the input potential to the buffer. Since the amplifier offsets are stored on the auto-zero capacitor, the integrator's slope is determined solely by the input voltage. The input voltage is integrated for exactly 1000 counts, thus reaching an integrator output proportional to the integral of the input for a fixed time.

Integrate Reference

At the end of 1000 counts, switch #4 is opened, the polarity flip-flop is set, and the integrate reference period begins. Depending on the polarity, switch #5 or #6 is closed, connecting the buffer input to ground or $2V_{ref}$. This causes the integrator to ramp towards its quiescent (auto-zero) point with a slope proportional to $+V_{ref}$ or $-V_{ref}$. When the integrator crosses its quiescent auto-zero point, the comparator changes state, causing the zero crossing detector to generate a conversion complete signal which inhibits the clock and loads the logic information into the output latches. Switch #5 (or #6) is opened, switches #1, #2, and #3 are closed, and the system returns to a quiescent auto-zero mode, awaiting the next initiate conversion signal. If 2000 counts are received prior to zero crossing, an out-of-range signal is generated which sets the "out-of-range" output and resets the system.

Note 1: Internal reference out ≃ 1.8V, reference input = 1.000 volts for 1.999 volt scale and 100mV for 199.9mV scale.
Note 2: External components shown are suggested for 3 readings/sec.
Note 3: Parallel BCD outputs and other latched outputs are strobed at end of conversion and retain data until completion of next conversion.
Note 4: Start/Reset should remain Low during Auto-Zero. Conversion is initiated by a positive pulse on start pin. (minimum width 100nsec).
Note 5: Component values ±20% typ.

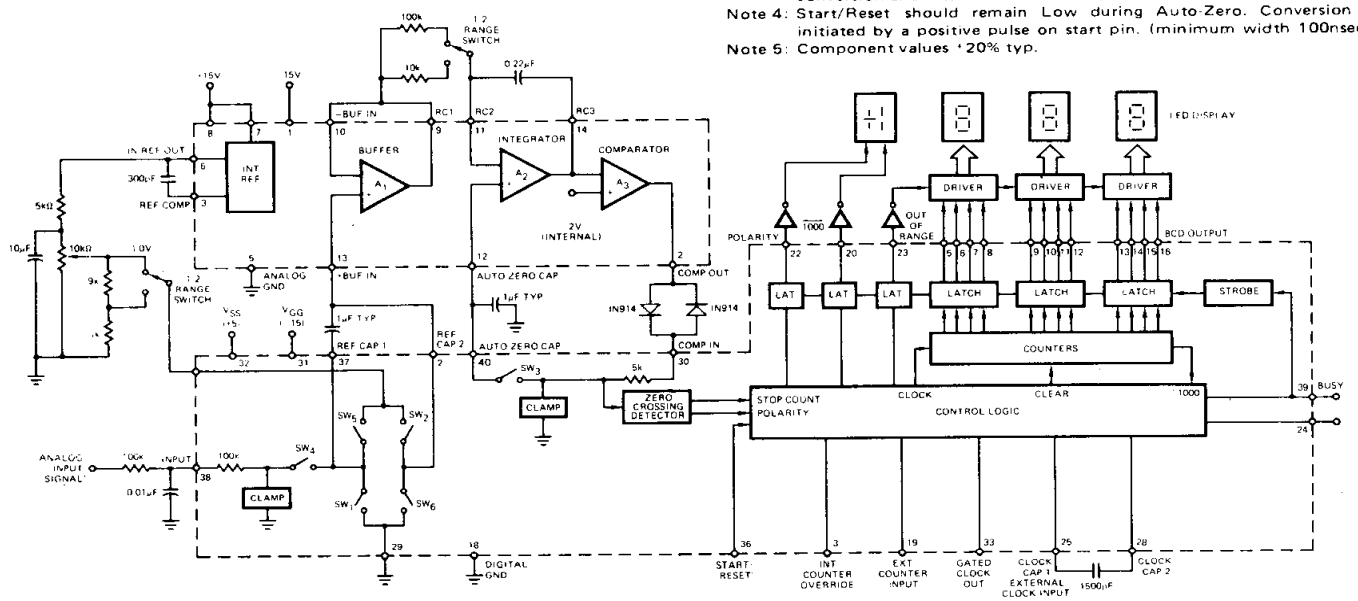


FIGURE 1. 3½ DIGIT A/D CONVERTER FUNCTIONAL DIAGRAM

7101 Digital Processor Controls

Two pins are included on the 7101 that allow the user to externally control the gain of the converter. The first pin, "Internal Counter Override", if held high, will inhibit the carry pulse from the internal counter that switches the converter from signal integrate to reference integrate. As long as this input is high, the converter will remain in the signal integrate mode. At the same time, it enables the other pin, External Counter Input, to supply this transition pulse from external sources. One technique for changing the gain of the system would be to hold "Internal Counter Override" high through the first N carry pulses. This would increase the signal integrate time by a factor of N+1 and, thus, the sensitivity of the system by N+1. Since the number of suppressed pulses could be controlled digitally, the system could accomodate signals from ±2.000V to ±200.0mV (or lower, if time permits) without changing the external analog scale factor components. By using more complex external logic and both inputs, the user could digitally set offset (tare) and scale factor to convert voltages to physical units such as "degrees centigrade", "pounds", or "feet".

A "BUSY" pin is provided which permits interrogating the 8052/7101 to determine the status of the conversion. During the signal integrate and reference integrate periods, the "busy" line is high until the conversion is complete, at which time "busy" line goes low. This transition can be used to signal "new data available".

The "Apex" pin provides a digital signal which goes high during the reference integrate period.

"OUT-OF-RANGE" is indicated by a latched "low" on pin 23 for counts over 2000. The BCD digital values are "high" (true), except $\overline{1000}$ which is "low".

A positive polarity of the analog input signal is indicated by a "high" state at the output of the "polarity" latch on pin 22.

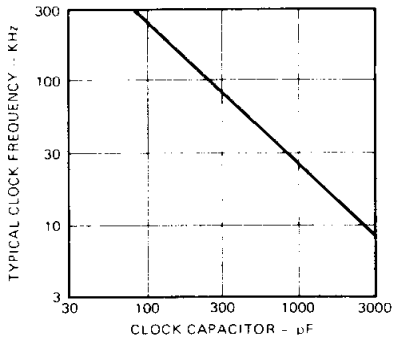


FIGURE 2.

The 7101 has an internal clock which requires a single capacitor between Pins 25 and 28 to operate. Figure 2 shows the typical capacitor value required to give the desired frequency.

During auto-zero, the clock is internally gated-off with Pin 28 high and Pin 25 low. When "start-reset" goes high, starting a measurement cycle, the clock starts counting with Pins 25 and 28 immediately changing phase. The counting continues until the end of the measurement cycle, at which time the clock is returned to its auto-zero condition.

In a typical application where visual readings are required three readings per second is near the optimum speed. Faste readings make it difficult to resolve individual readings while at slower rates the reader has to wait too long betwee measurements. In this application, 40% of the time (133mS could be allocated to auto-zero and 60% (200mS) to signa and reference integrate. Since a measurement cycle consist of 3,000 clock pulses maximum, this dictates a cloc frequency of 15kHz. Also, since the dual-slope techniqu of A/D conversion is not first-order dependent on cloc frequency, the ±20% variation of clock frequency fror unit-to-unit would result in no measurable error. Howeve in some applications, a more precise clock frequency woul be desired. For instance, if precise rejection of 60Hz required, the signal integrate phase (1,000 counts) woul have to contain an integral number of 60Hz periods. Fo these applications, an external clock can be used by deletir the capacitor and connecting the external clock to Pin 2 However, if the clock is run asynchronously with start/rese there will be one clock pulse of uncertainty in the integrat signal time, depending on where in the clock pulse perio the start/reset went high. This will show up as one cour of noise for signal near full-scale. This noise or jitter can b avoided by synchronizing the start/reset pulse to th negative-going edge of the external clock. Pin 33, Gate Clock Out, is a buffered output of the clock (internal o external) that is off (low) during auto-zero and in pha with Pin 25 during measurement.

Component Selection

Except for the reference voltage, none of the componer values are first order important in determining the accurac of the instrument. While this is undoubtedly an advantag of this approach, it does make the selection of nomin component values arbitrary at best. For instance, th reference capacitor and auto-zero capacitor are each show as 1.0μfd. These relatively large values are selected to giv greater immunity to PC board leakage since much small capacitors are adequate for charge injection errors o leakage errors from the 8052/7101.

The ratio of integrating resistor and capacitor is selected t give 9-volt swing for full-scale inputs. This is a compromi between possibly saturating the integrator (at ±14V) du to tolerance build-up between the resistor, capacitor, ar clock and the errors a lower voltage swing could induc due to offsets referred to the output of the comparato Again, the .22μfd value for the integrating capacitor selected for PC board considerations alone since the ver small leakage at the integrator input is nulled at auto-zer A very important characteristic of the integrating capacito is low dielectric absorption. A polypropylene capacito gave excellent results. In fact, a good test for dielectr absorption is to use the capacitor in this circuit with th input tied to reference. This ratiometric condition shou read 1.000 and any deviation is probably due to dielectr absorption. In this ratiometric condition, a polycarbona capacitor contributed an error of approximately 0.8 digi polystyrene about 0.3 digit, and polypropylene less tha 0.05 digit. The increased T.C. of polypropylene is of r consequence in this circuit. The dielectric absorption of th reference capacitor and auto-zero capacitor are only impo tant at power on or when the circuit is recovering from a overload. Thus, smaller or cheaper capacitors can be use here if accurate readings are not required for the first fe seconds of recovery.

The back-to-back diodes on the comparator output are recommended in the 200.0mV range to reduce the noise effects. In the normal operating mode, they offer a high impedance and long integrating time constant to any noise pulses charging the auto-zero capacitor. At start-up or recovery from an overload, their impedance is low to large signals so the capacitor can be charged in one auto-zero cycle. If only the 2.000V range is used, a 100k resistor in place of the back-to-back diodes is adequate for noise effects.

Maximum Clock Frequency

The maximum conversion rate of most dual-slope A/D converters is limited by the frequency response of the comparator. Even though the comparator in this circuit is all NPN with an open loop gain-bandwidth product of 300MHz, it is no exception. The comparator output follows the integrator ramp with a 3μS delay. At a clock frequency of 160kHz (6μS period), half of the first reference integrate period is lost in delay. This means that the meter reading will change from 0 to 1 with 50μV in, 1 to 2 with 150μV, 2 to 3 at 250μV, etc. This transition at mid-point is considered desirable by most users. However, if the clock frequency is increased appreciably above this, the instrument will flash 1 on noise peaks even when the input is shorted.

Some circuits use positive feedback or a latch to solve the delay problem. However, unless the comparator voltage swing, the comparator gain, and the integrator gain are carefully controlled, this circuit can generate **anticipation** errors that greatly exceed the 3μS **delay** error. Also, it is very susceptible to noise spikes. A more controlled approach for extending the conversion rate is the use of a small resistor in the integrator feedback loop. This feeds a small pulse to the comparator to get it moving quickly and partially compensate for its delay.

The minimum clock frequency is established by leakage on the auto-zero and reference capacitor. With most devices, measurement cycles as long as 10 seconds gave no measurable leakage error.

4 APPLICATIONS

8052/7101 3½ Digit LCD DPM/DVM

Figure 3 illustrates an application where the 8052/7101 interfaces with a Liquid Crystal Display. The CD4054 and CD4055s are Liquid Crystal Display Drivers (4-segment and 7-segment, respectively) which provide the level shifting (up to $30V_{p-p}$ at $V_{DD}-V_{EE}$ = 15V) necessary to drive the LCD. Overrange is indicated by a special character. If blanking of any part of the display is required on overload, Pin 23 (7101) can be used to drive Pin 7 on those display drivers via an inverter and level shift such as CD4009 or 74C903 or another CD4054. Display applications requiring a plus sign rather than a blank indication for positive analog input levels (i.e., +1.999 versus 1.999) need to invert the "polarity" logic output level which is normally high for positive analog input signals.

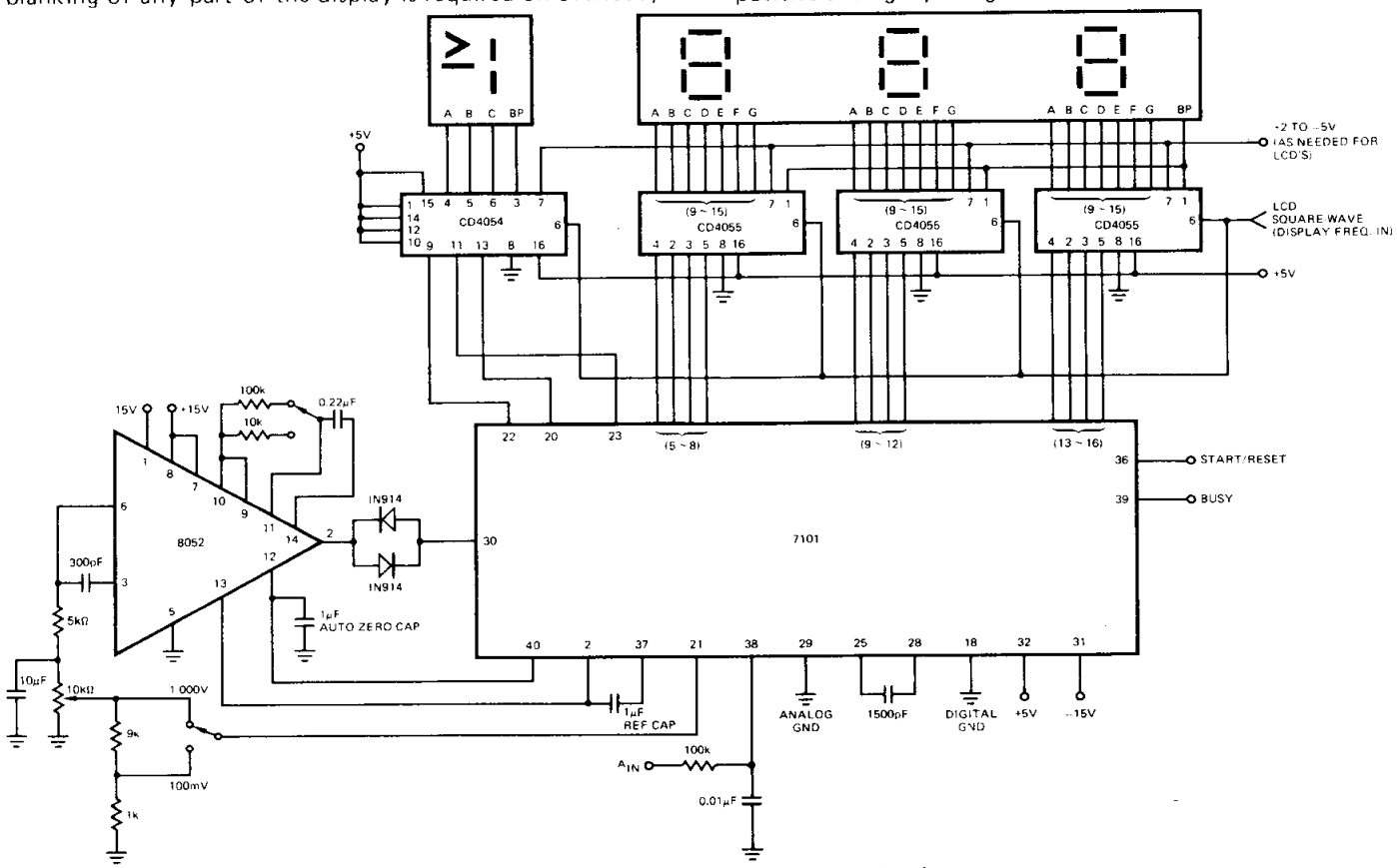


FIGURE 3. 8052/7101 3½ DIGIT LCD DPM/DVM

8052/7101/6100/6101 Set

The circuit in Figure 4 interfaces the 8052/7101 A-to-D converter chip set to an IM6100* microprocessor, using the 6101* Parallel Interface Element. Hex Tri-state Buffers (e.g., MM80C95*) are used to control bus access from the 7101 during read operations.

Conversion is initiated by activating the WRITE 1 line (positive going). The converter pair will then convert the analog input to digital form, and latch the data in the 7101. The busy line will go low as the conversion ends, and this transition is sensed by the SENSE 1 line, triggering an interrupt. The interrupt routine should read the 12-line data word, and then the polarity, $\overline{1000}$ and out-of-range lines.

Sufficient time must be allowed for the auto-zero loop to settle before retriggering a conversion. Ten milliseconds of auto-zero is sufficient to null any offsets to 10 microvolts. At power-on or after an overload, 100 milliseconds is required to assure the auto-zero capacitor has charged to the correct value. This time delay may be implemented conveniently using the IM6102 (Memory Extender/Time Delay Device).

Some skeletal service routines for this connection are given on page 7 and 8.

*References:
Intersil IM6100 CMOS 12 bit Microprocessor
Intersil IM6101 Parallel Interface Element
National MM80C95 Hex CMOS Tri State Buffers

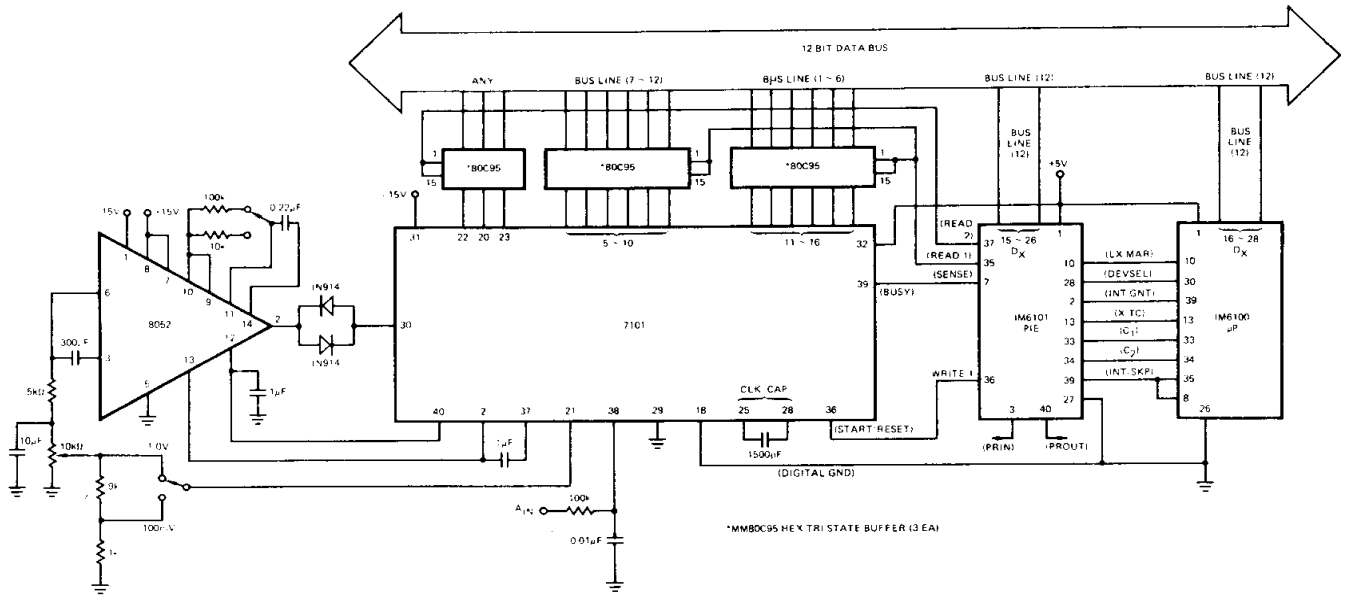


FIGURE 4. 3½ DIGIT PARALLEL BCD DATA ACQUISITION SYSTEM

8052/7101/6100/6101 APPLICATION PROGRAM

A possible set-up and service routine for the connection is given below.

```
/ASSUME PIE SELECT IS SET TO 54, INTERRUPT VECTOR TO 2000
        (OCTAL)
/INITIALIZE ROUTINE: SET-UP FOR NO INTERRUPT

1200    7200            CLA
1201    1240            TAD SSCRA
1202    6545            WCRA 54         /SET-UP CONTROL REGISTER A
1203    7200            CLA
1204    1241            TAD SSCRB
1205    6555            WCRB 54         /SET-UP CONTROL REGISTER B
1206    7200            CLA
1207    1242            TAD SSVV
1210    6556            WVR 54          /SET-UP VECTOR REGISTER

1220    0000  CONVERT,  Ø               /INITIATE CONVERSION SUBROUTINE
1221    1243            TAD SSCRAI
```

```
1222    6545            WCRA 54         /SET-UP CONTROL REGISTER A
1223    6541            WRITE1 54       /THE WRITE PULSE STARTS CONVERSION

1224    5620            JMP I CONVERT   /RETURN

1240    0040    SSCRA,  0040            /WP 1 SET HI, IE1 SET LO
1241    0000    SCRRB,  0000            /SL1, SP1 SET LP, NEGATIVE EDGE SENSE
1242    2000    SSVV,   2000            /VECTOR ADDRESS
1243    0041    SSCRAI, 0041            /WPI SET HI, IE1 SET HI

0000    0000    INTRPT, Ø               /ENTRY POINT FOR INTERRUPT
0001    6002            IOF             /DISABLE INTERRUPT, JUMP TO VECTOR ADDRESS

0140    0000    AD1,    Ø               /FIRST WORD OF DATA
0141    0000    AD2,    Ø               /SECOND WORD OF DATA
0160    0000    TEMP1,  Ø               /TEMPORARY STORAGE

2000    5210    VV,     JMP ATOD        /JUMP TO SERVICE POINT

2010    3160    ATOD,   DCA TEMP1       /SAVE AC
2011    6540            READ1 54        /READ BCD LINES
2012    3140            DCA AD1         /AND STORE
2013    6550            READ2 54        /READ POLARITY, 1000, AND OVERRANGE
2014    7040            CMA             /COMPLEMENT TO THE TRUE
2015    3141            DCA AD2         /AND STORE
/       __      ___     ____            /ANY OTHER WORK
2020    1160            TAD TEMP1       /RESTORE AC
2021    6001            ION             /RESTORE INTERRUPT
2022    5400            JMP I INTRPT    /RETURN
```