M02169

-5.2 or +5.0 Volt EAM and DML Driver IC for Applications to 10.7 Gbps

This device is a highly integrated, programmable electro-absorptive modulator (EAM) and directly modulated laser (DML) driver intended for SONET/SDH applications to 10.7 Gbps.

Using differential CML data and clock inputs, this part supplies offset, bias and modulation for driving an EAM or DML.

The modulation output is designed to be DC-coupled to the modulator or laser. In EAM applications, user controlled offset adjustment is integrated into the signal output. Automatic power control allows for optimization of either DML or EAM applications.

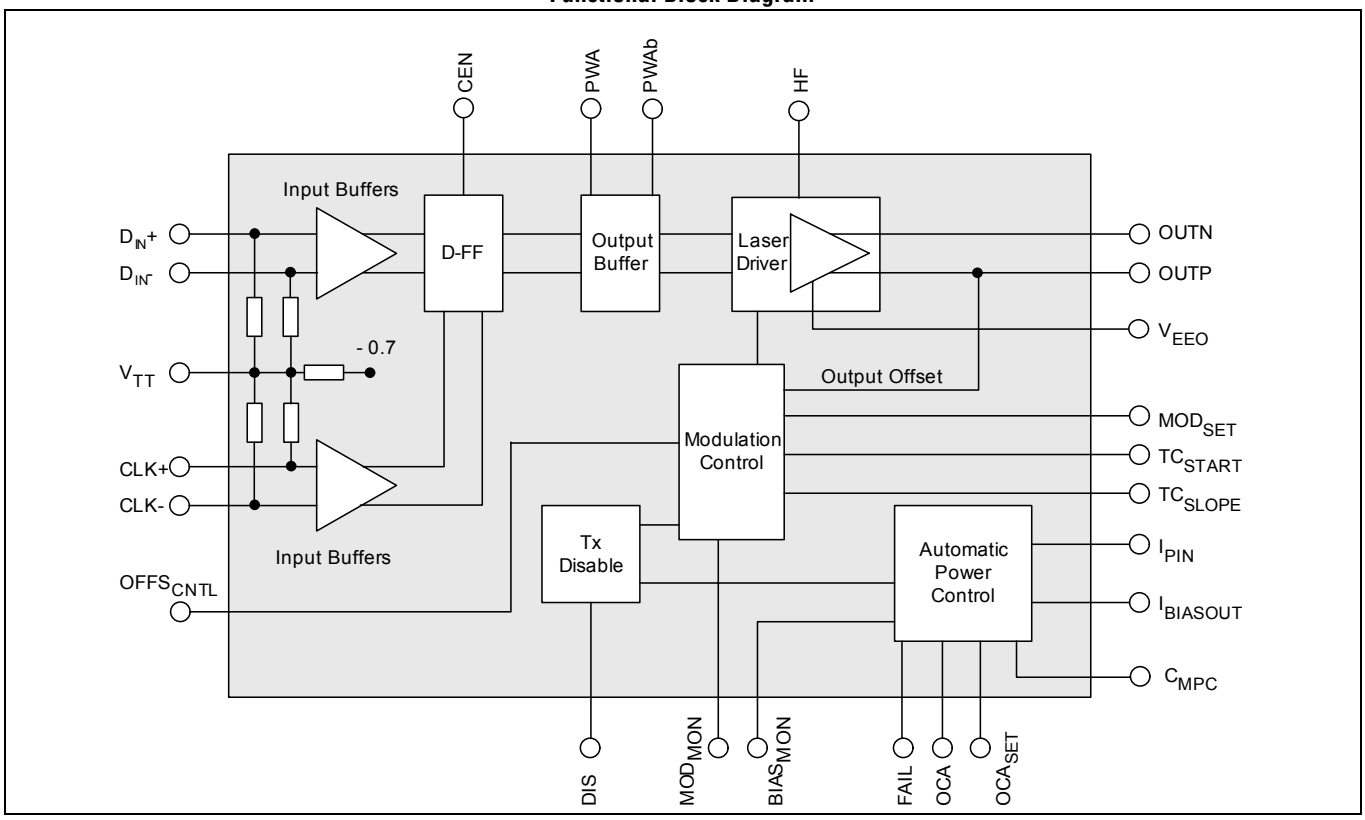
Applications

- SONET OC-192 Optical Transmitters
- SDH STM-64 Optical Transmitters
- OC-192/STM-64 Optical Transmitters with FEC
- 10 Gigabit Ethernet Transmitters
- 10 Gigabit Fibre Channel Transmitters
- Optical Transmitter applications to 10.7 Gbps

Features

- High speed operation; suitable for applications to 10.7 Gbps. Rise/fall times < 30 ps
- DC-coupled modulation output
- Differential CML data and clock inputs to minimize pattern dependent jitter (retiming is optional). Can be AC- or DC-coupled CML or AC-coupled PECL
- Independently programmable modulator offset and modulation voltages for EAM applications. Offset voltage to 1 V and modulation to 3 Vpp into 50 Ω at V_{EE} = -5.2 V
- In EAM applications, offset integrated into signal output without using external components, facilitating a clean high-speed signal path
- Automatic power control for DML applications - laser bias current to 100 mA, usable for EAM applications with an external current mirror
- Pulse width adjust to ± 20 ps
- Bias and modulation current monitors
- Available in 32 pin 5 x 5 mm QFN package

Functional Block Diagram



Ordering Information

Part Number	Number of Channels	Package	Operating Temperature
M02169Q32-xx	...	32 pin QFN	–40 °C to 85 °C
NOTE: xx represents the revision number. Please contact your local sales office for correct digit(s).			

Revision History

Revision	Level	Date	ASIC Revision	Description
A	Advance	February 2002	-11	Initial Release
B	Preliminary	February 2003	-12	
C	Released	January 2004	-13	

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1.0 Functional Description

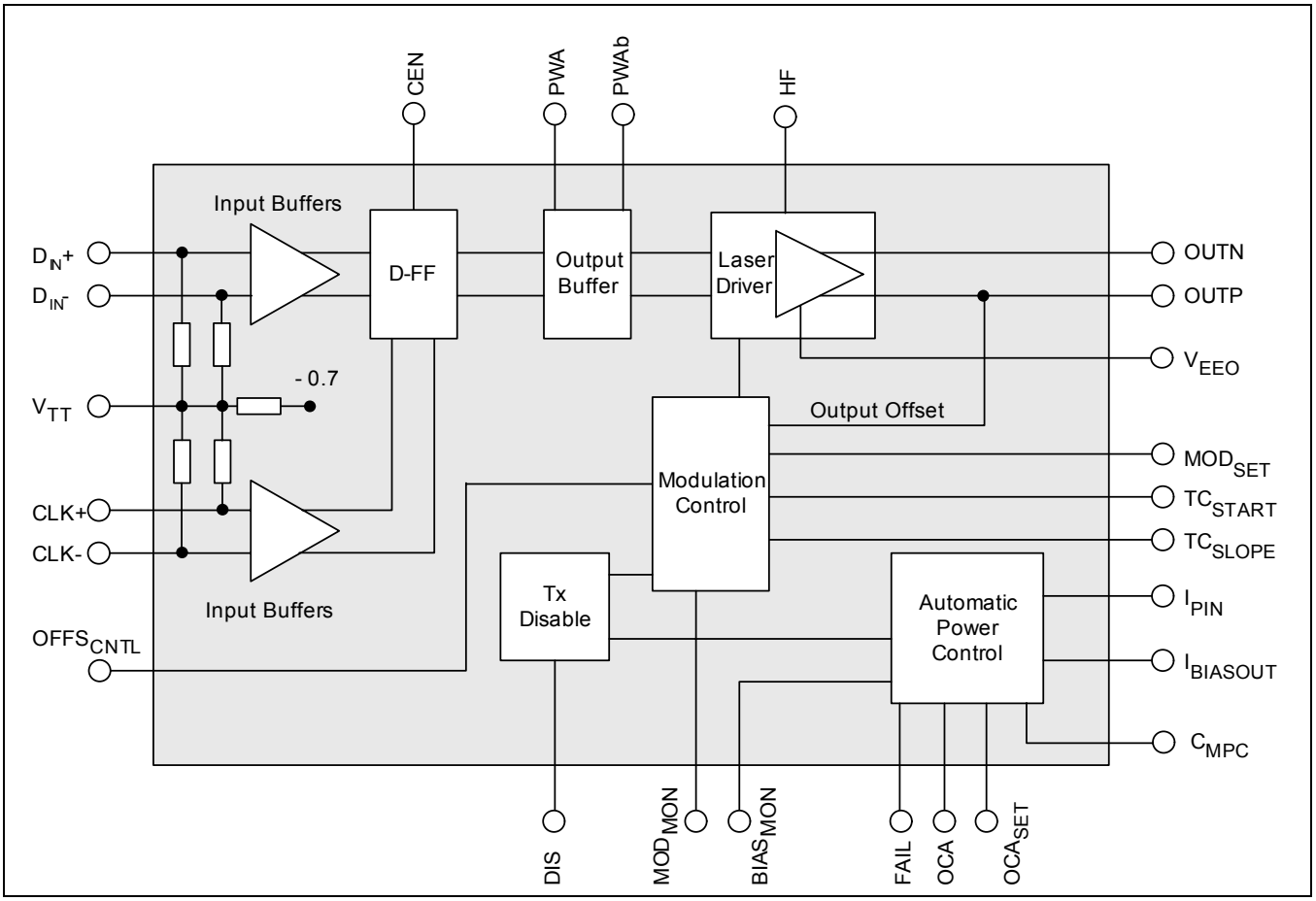
1.1 Overview

This device is a highly integrated, programmable electro-absorptive modulator (EAM) and directly modulated laser (DML) driver intended for SONET/SDH applications to 10.7 Gbps.

Using differential CML data and clock inputs, this part supplies offset, bias and modulation for driving an EAM or DML.

The modulation output is designed to be DC-coupled to the modulator or laser. In EAM applications, user controlled offset adjustment is integrated into the signal output. Automatic power control allows for optimization of either DML or EAM applications.

Figure 1-1. M02169 Block Diagram Example



1.2 Features

- High speed operation; suitable for applications to 10.7 Gbps. Rise/fall times < 30 ps
- DC-coupled modulation output
- Differential CML data and clock inputs to minimize pattern dependent jitter (retiming is optional). Can be AC- or DC-coupled CML or AC-coupled PECL
- Independently programmable modulator offset and modulation voltages for EAM applications. Offset voltage to 1 V and modulation to 3 Vpp into 50 Ω at V_{EE} = -5.2 V
- In EAM applications, offset integrated into signal output without using external components, facilitating a clean high-speed signal path
- Automatic power control for DML applications - laser bias current to 100 mA, usable for EAM applications with an external current mirror
- Pulse width adjust to ± 20 ps
- Bias and modulation current monitors
- Available in 32 pin 5 x 5 mm QFN package

1.3 General Description

The M02169 driver is a highly integrated, programmable electro-absorbtive modulator (EAM), or direct-modulated laser (DML) driver which can deliver a 1 to 3 Vpp voltage swing with a 0 to 1 V offset into a 50 Ω load. On chip 50 Ω source termination is provided to improve signal fidelity at high speeds, easing interfacing design. Designed to operate from a -5.2 V power supply or alternatively a +5V supply, the device is specifically intended to be used with a 50 Ω laser or EAM.

The driver output is DC-coupled to the modulator or laser. An offset adjustment is provided in addition to the automatic power control (APC) to optimize the configuration for either DML or EAM applications. Offset is integrated into the signal output to help minimize external components and provide a clean high-speed interface.

Modulation and bias monitor current mirrors are provided to allow monitoring without disturbing the analog signal path. Pulse width adjust allows the user to compensate for non-symmetric laser or modulator characteristics.

1.3.1 Detailed Description

The M02169 laser driver consists of the following circuitry: A high speed modulator, input buffer, modulation current control with monitor, bias monitor with automatic power control (APC), internal offset supply (no external inductor needed), laser fail indication, disable and over-current alarm for bias current.

1.3.2 Bias Generator and Automatic Power Control

The bias generator is capable of sinking up to 100 mA of current into the driver with a compliance voltage from 0 V to -4.0 V. The slow-start feature assures the bias current does not spike as the bias generator is enabled.

When driving a laser directly, automatic power control (APC) of the laser is realized by using an external monitor photodiode connected to I_{PIN} and a resistor (R_{MPCSET}) from I_{PIN} to V_{EE}. This creates a voltage at I_{PIN} which is one input to an internal comparator and whose other input is a bandgap reference voltage. The output of this comparator, after being low pass filtered by a capacitor connected to C_{MPC}, controls the level of the bias generator current (the laser bias current). This feature can also be used with an external current mirror to provide APC for the integrated DFB laser portion of an EAM.

The value of R_{MPCSET}, the resistor from I_{PIN} to V_{EE}, is calculated as:

$$R_{MPCSET} = 1.28\ V / (I_{PIN})$$

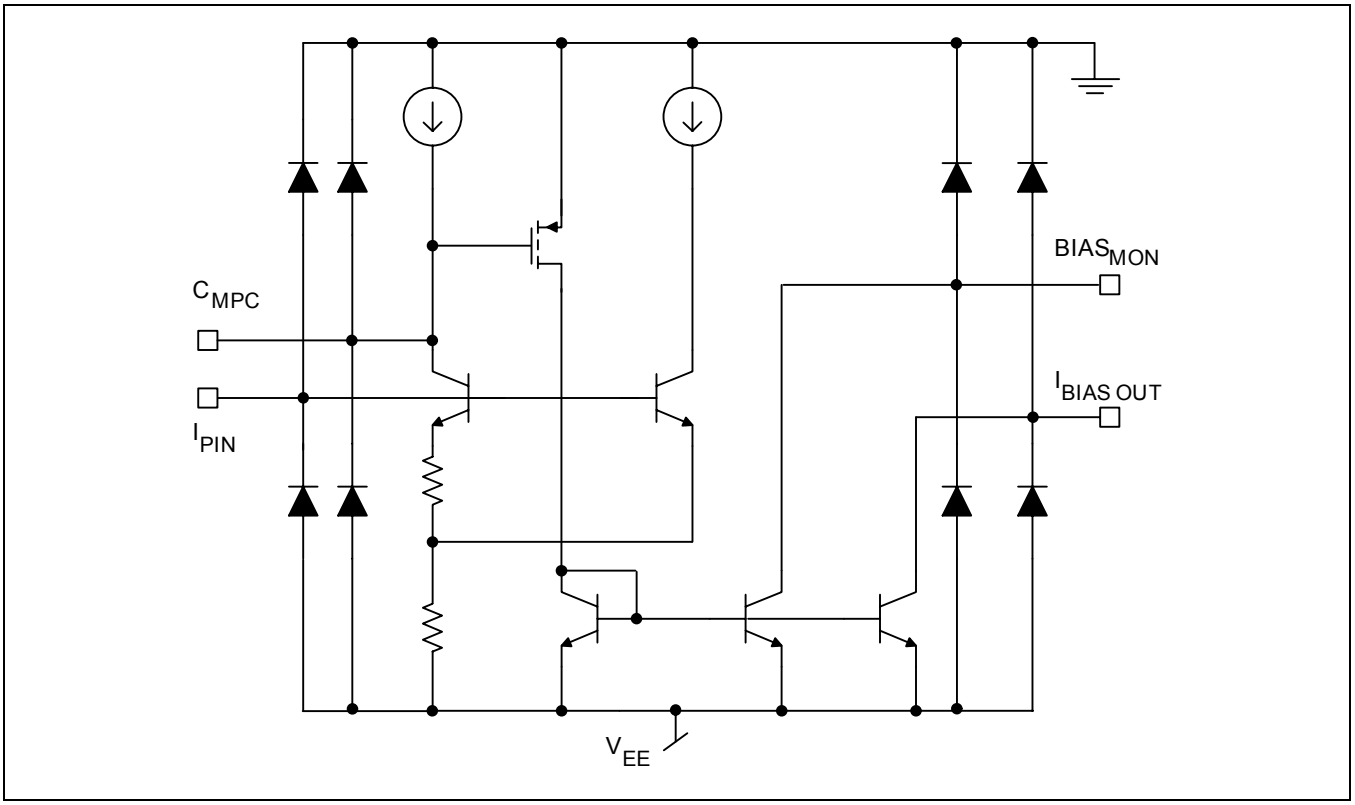
where I_{PIN} is the PIN diode current.

The APC loop time constant is controlled by connecting a capacitor from C_{MPC} to V_{EE}. The minimum value of C_{MPC} is 1 nF, and the formula for APC loop bandwidth is:

$$C_{MPC}\ (nF) = 49.12 / BW\ (kHz)$$

The bias generator also includes a bias current monitor mirror ($BIAS_{MON}$), whose output current is approximately 1/60th of the bias current. Current is sunk into this pad (towards V_{EE}).

Figure 1-2. Automatic Power Control Loop and Bias Monitoring



1.3.3 APC Loop Fail and Overcurrent Alarm (OCA)

The M02169 has two alarm outputs: FAIL and OCA. When the APC loop is unable to maintain the proper voltage at I_{PIN}, the comparator at I_{PIN} will assert the FAIL output indicating that the APC loop is unable to maintain constant power. The part continues to supply modulation and bias current even when FAIL is asserted.

The OCA alarm is asserted when the current at $I_{BIASOUT}$ exceeds the level established by the resistor connected to OCA_{SET}. The OCA alarm output is the result of a comparator that has two inputs: one is the current through a resistor from the OCA_{SET} input to V_{EE} (R_{OCASET}) and the other is a current proportional to the bias generator current. When OCA is asserted, the part continues to supply modulation and bias current. An OCA alarm could be used to indicate laser end of life.

Once the OCA_{SET} level is exceeded, the OCA flag is asserted, but not latched. Internal feedback to I_{PIN} will attempt to limit the bias output current to roughly 10% above the OCA_{SET} level. The OCA flag is de-asserted once

the bias current decreases below the OCA_{SET} level. The temperature coefficient of the OCA_{SET} level is approximately 2000 ppm/°C.

Figure 1-3. OCA Set Input

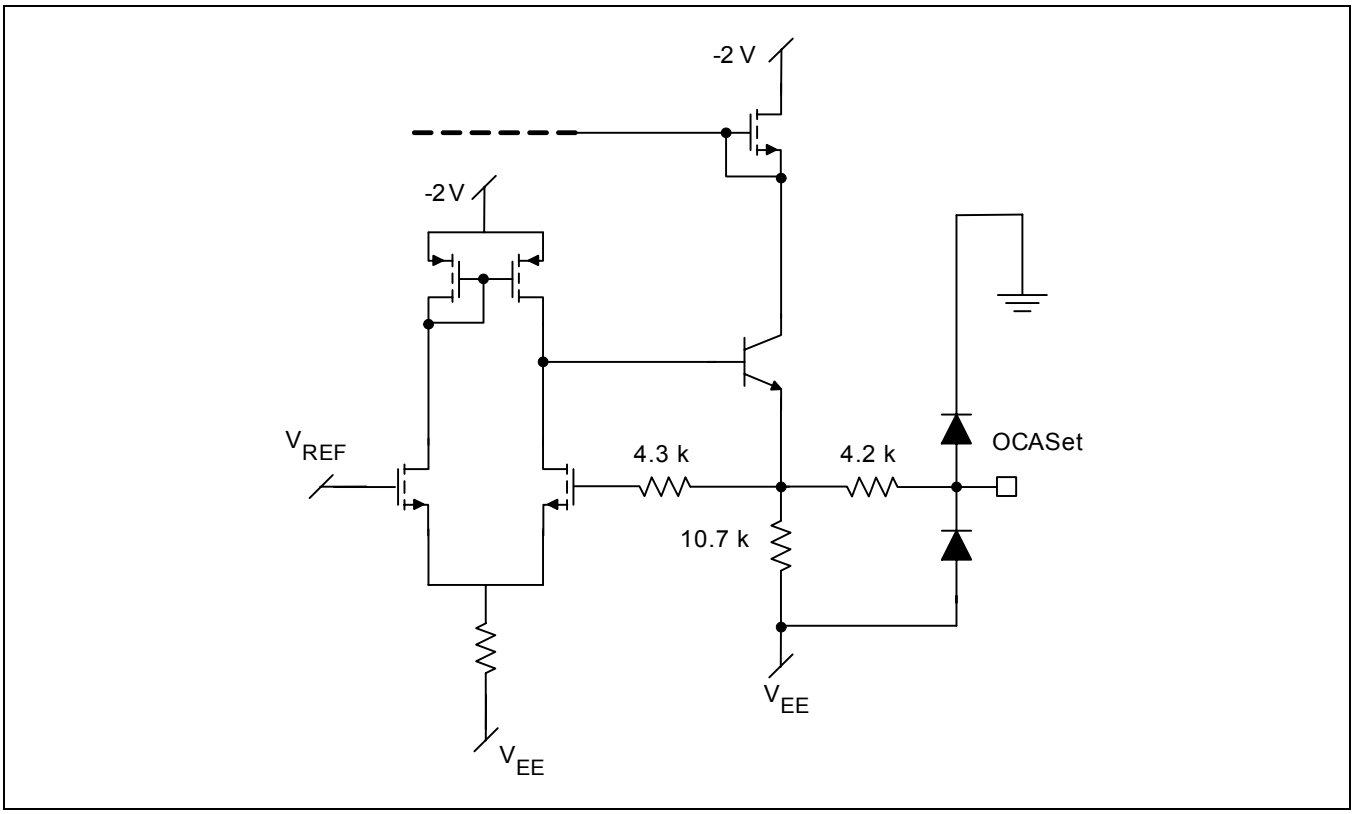
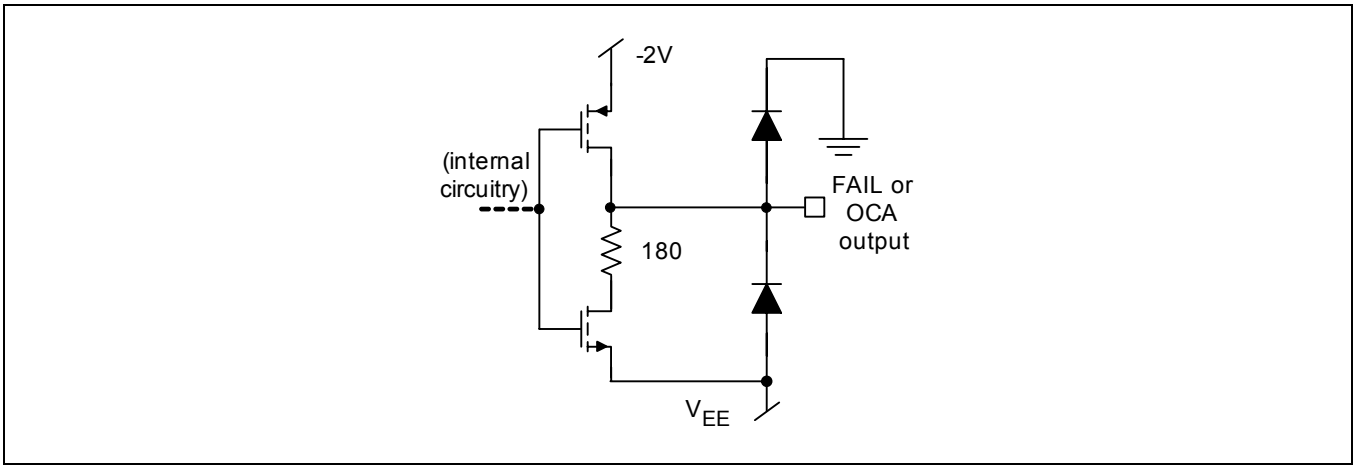


Figure 1-4. Fail and OCA Outputs



1.3.4 Modulator

The modulator consists of the following:

- An output current switch capable of delivering a 1 to 3 Vpp signal into a 50 Ω load
- An offset supply, programmable from 0 to -1V
- Modulation monitoring

The output stage is has two outputs: OUTN and OUTP. There are two OUTN pins, each configured with a 50 Ω series resistor (resulting in 25 Ω equivalent resistance when the pins are connected together). The two OUTN pins should together be directly connected to the highest potential (usually ground). The collector of OUTP has an equivalent internal 60 Ω series resistance which allows a good impedance-match with a 50 Ω transmission line terminated by a 50 Ω load to ground.

The output stage also has a separate current path to V_{EE} labelled V_{EEO}. This allows the isolation of output switching currents from the rest of the system. V_{EEO} should be connected to ground through a ferrite to further improve isolation (Murata BLM18HG471SN1 or equivalent recommended).

The modulator current control includes TC_{START} and TC_{SLOPE} controls which, using resistor programming, sets the compensation of modulation current with temperature (TC_{SLOPE}) and the temperature at which the compensation slope starts to occur (TC_{START}). The details of these functions are described further in the Design Details section of this datasheet.

The modulation current monitor (MOD_{MON}) is a current mirror, whose output current is approximately 1/30th of the modulation current. Current is sunk into this pin (towards V_{EE}).

Modulation output voltage is set by a resistor control (R_{MODSET}) connected between the MOD_{SET} pin and V_{EE}. Current is sourced from the MOD_{SET} pin to V_{EE}. R_{MODSET} is selected as:

$$V_{MOD} = 1.28 / (R_{MODSET} + 3.26\ k\Omega) * 27.3 * 450 \text{ or}$$

$$R_{MODSET} = [(27.3 * 450 * 1.28) / (V_{MOD})] - 3.26\ k\Omega$$

I_{MOD} can be calculated by taking V_{OUT} p-p and dividing it by the 27.3 Ω output load.

Figure 1-5. Modulator Output

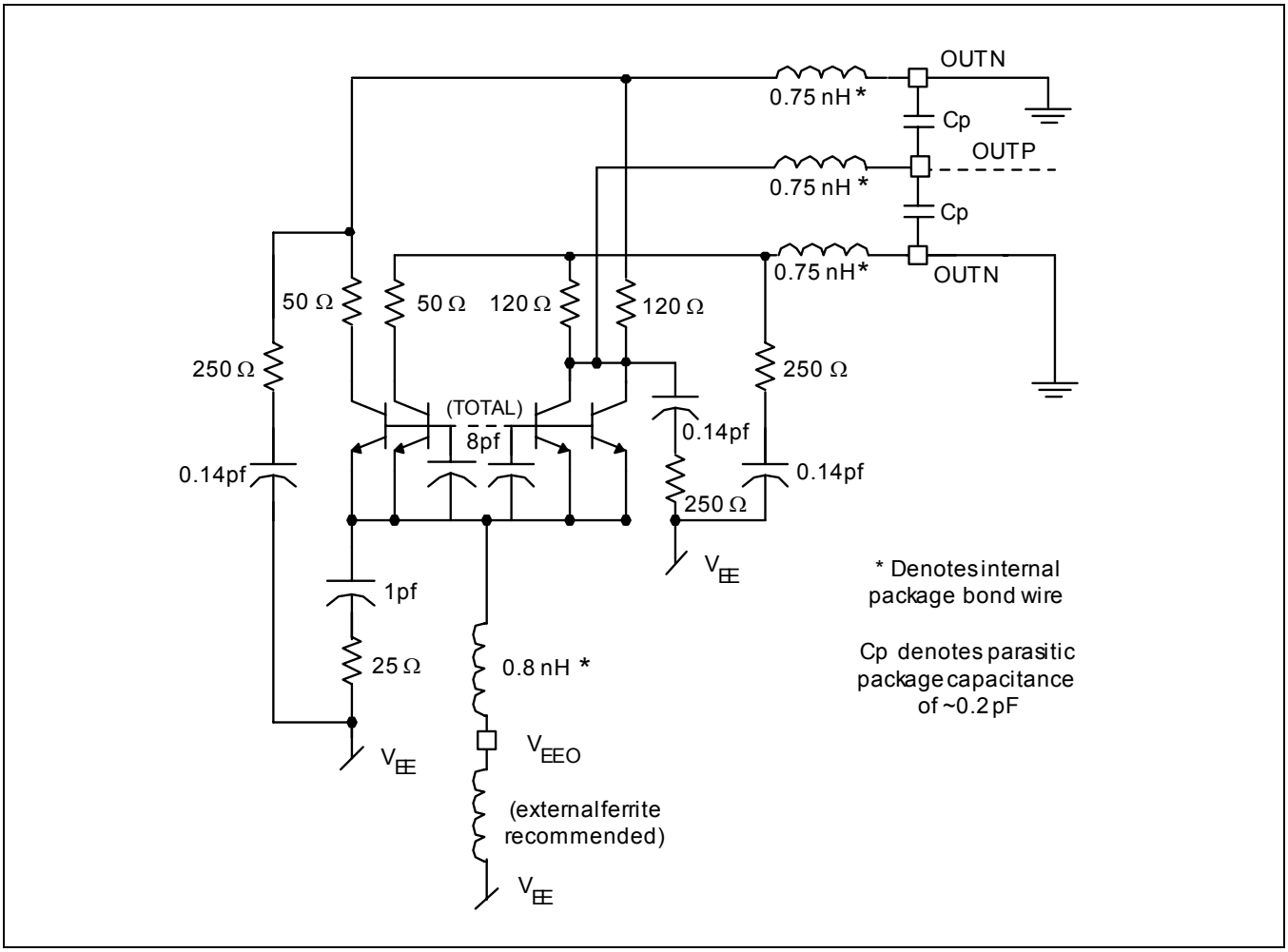
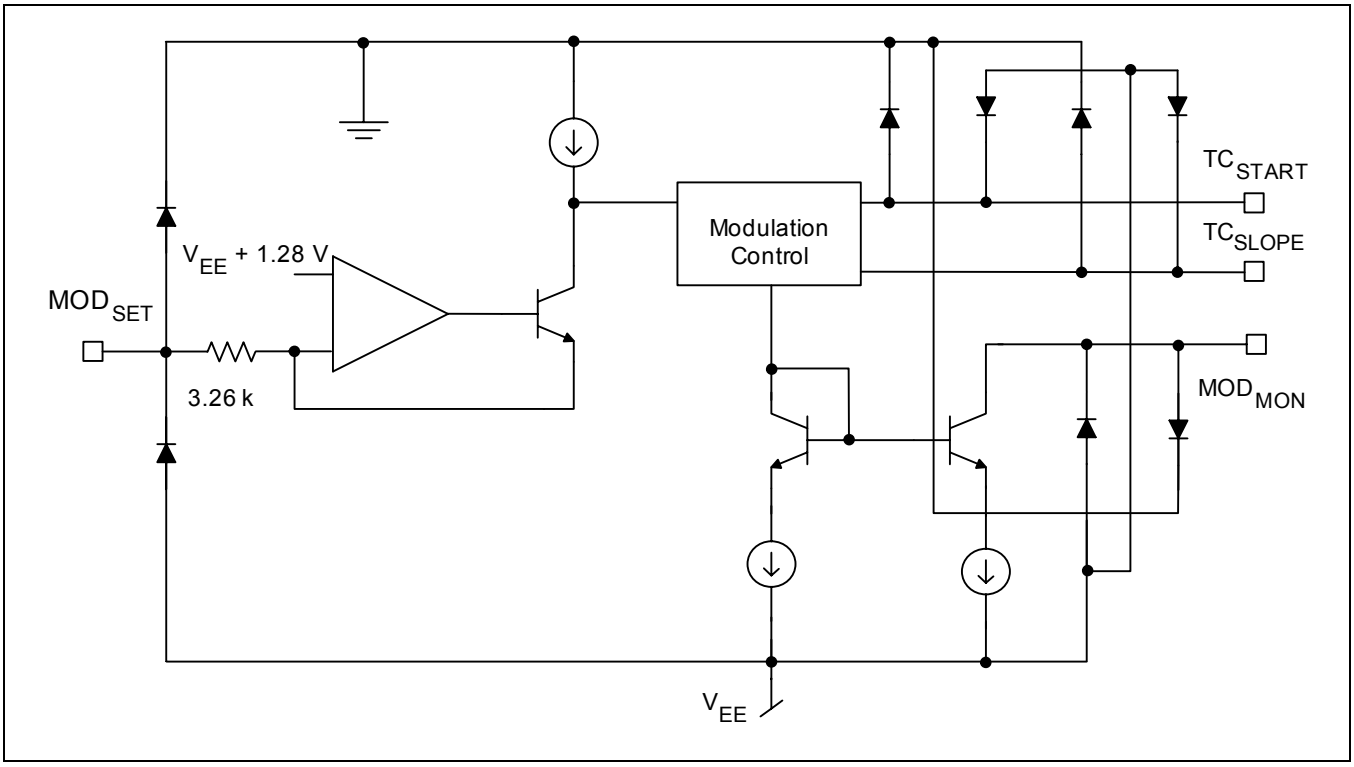


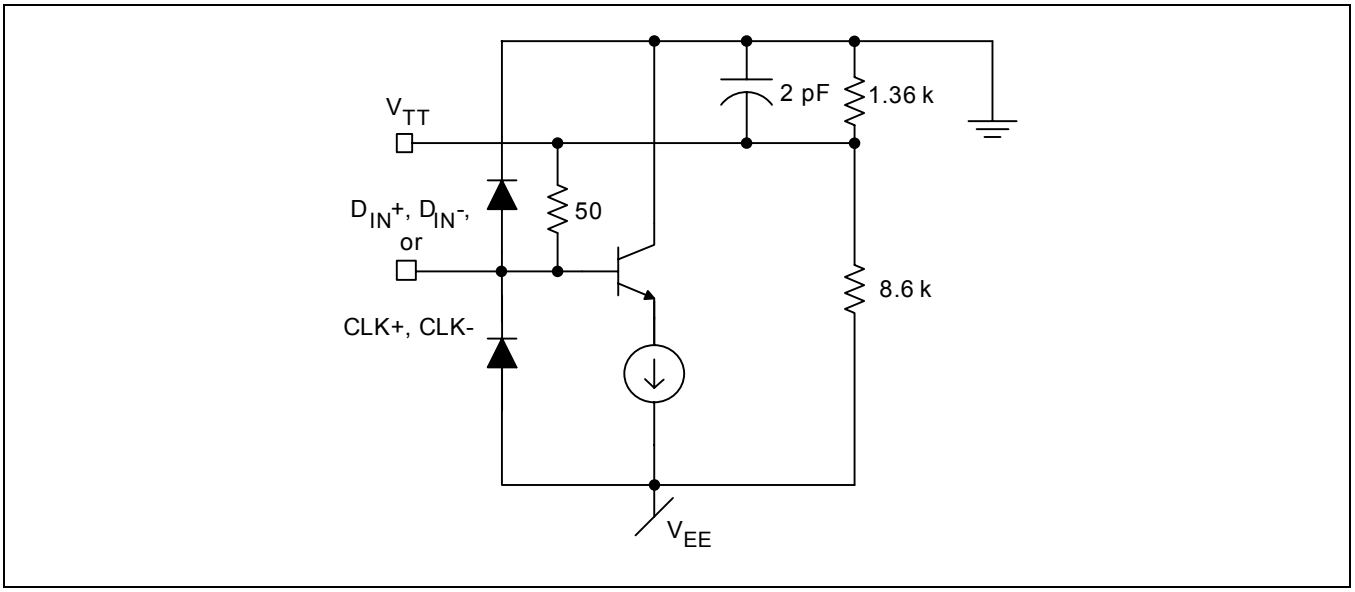
Figure 1-6. Modulator Control and Monitoring



1.3.5 Data and Clock Inputs

An input buffer with a D flip-flop allows the clock signal to re-time the data when the CEN input is tied high (GND). Data is re-timed on the rising edge of the clock signal. Both the clock and data inputs are CML levels, but can be AC-coupled PECL. The V_{TT} Pin allows the input termination network to be level-shifted for DC-coupling to a variety of signal levels and types. With V_{TT} tied high to ground, the clock and data inputs accept CML signals, while leaving V_{TT} floating allows the inputs to accept AC-coupled PECL signals. The relationship between clock, data and V(OUTP) is shown in Figure 2-1.

Figure 1-7. Data and Clock Inputs



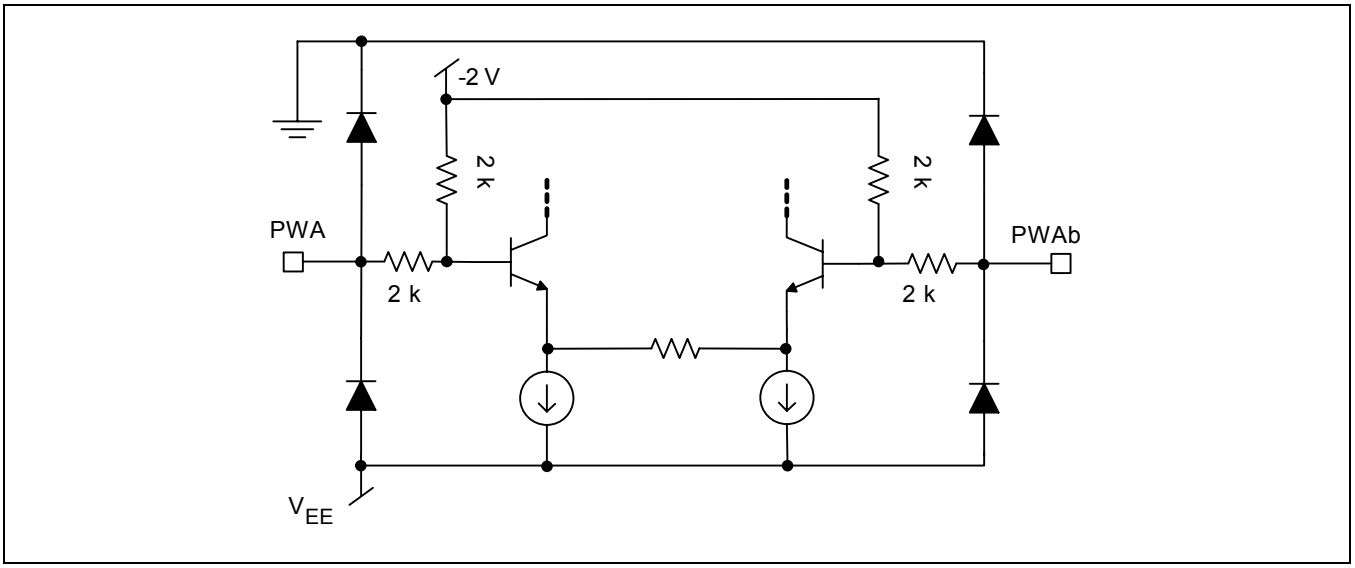
1.3.6 V_{TT} Input Termination

As mentioned in the data and clock description, the V_{TT} pin allows the input termination network to be level-shifted for DC-coupling to a variety of signal levels and types. With V_{TT} tied high to GND, the clock and data inputs accept CML signals, while leaving V_{TT} floating allows the inputs to accept AC-coupled PECL signals.

1.3.7 Pulse Width Adjust

Pulse Width adjustment is accomplished by connecting a 2 kΩ potentiometer to the PWA and PWAb pins with the center tap of the potentiometer going to V_{EE}. Connecting PWA and PWAb to the most negative potential disables this function. The pulse width adjust functions over a range of ±20 ps (when the duration of the positive going pulse is increased by up to 20 ps, the duration of the negative going pulse is correspondingly reduced by up to 20 ps).

Figure 1-8. Pulse Width Adjust



1.3.8 Clock Enable

This TTL/CMOS compatible input is referenced to V_{EE}. When the CEN input is tied high (GND), data re-timing is enabled which allows the clock signal to re-time the data. When CEN is tied low or left floating, the clock buffer is disabled, also resulting in a power savings. When the clock buffer is disabled the clock inputs may be left floating.

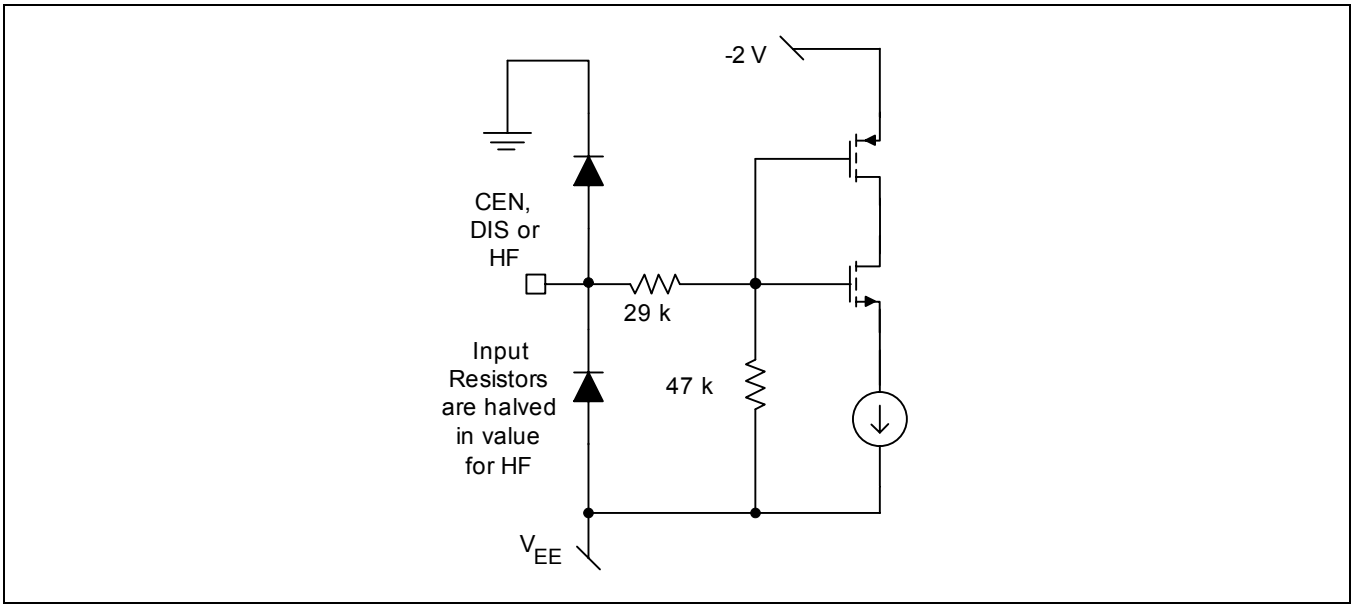
1.3.9 TX Disable

A TTL/CMOS compatible low referenced to V_{EE} on DIS (or leave floating) enables the modulation and bias current outputs while a high disables them. When high, will disable the bias and modulation outputs.

1.3.10 HF

A TTL/CMOS compatible low referenced to V_{EE} on HF (or leave floating) enables output damping which reduces overshoot and slightly increases rise and fall times. This compensation is typically selected through evaluation depending on laser/EAM characteristics.

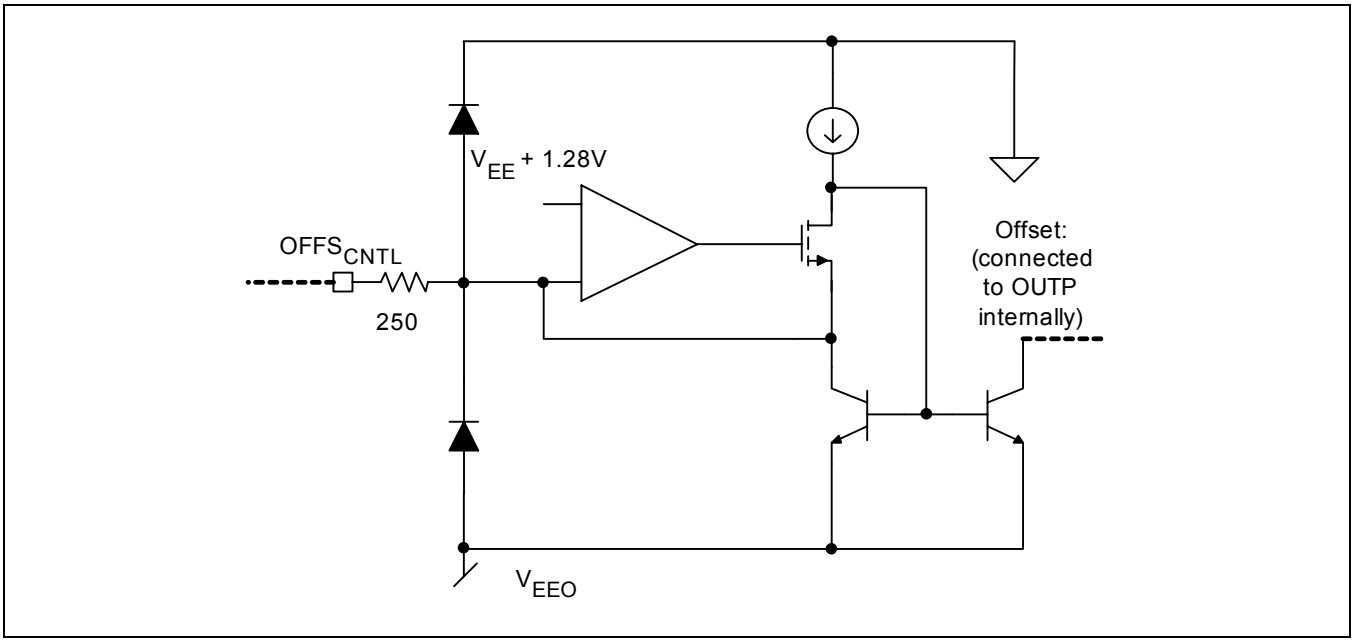
Figure 1-9. Clock Enable, Tx Disable and HF Input



1.3.11 Output Offset Control

Shown in Figure 1-10, the output offset control is used to provide the needed reverse DC bias for an EAM. The $OFFS_{CNTL}$ adjustment provides enough output current into 50 Ω to deliver a 0 to -1V offset. Connecting a 2k ohm potentiometer from $OFFS_{CNTL}$ to V_{EE} adjusts the output offset voltage. Alternatively, the $OFFS_{CNTL}$ input can be connected to a DAC which is capable of sinking up to 2 mA of current to the most negative supply.

Figure 1-10. Offset Control



1.4 Laser Eye Safety

Using this laser driver in the manner described herein does not ensure that the resulting laser transmitter complies with established standards such as IEC 825. Users must take the necessary precautions to ensure that eye safety and other applicable standards are met. Note that determining and implementing the level of fault tolerance required by the applications that this part is going into is the responsibility of the transmitter designer and manufacturer since the application of this device cannot be controlled by MindSpeed.

1.5 Design Brief

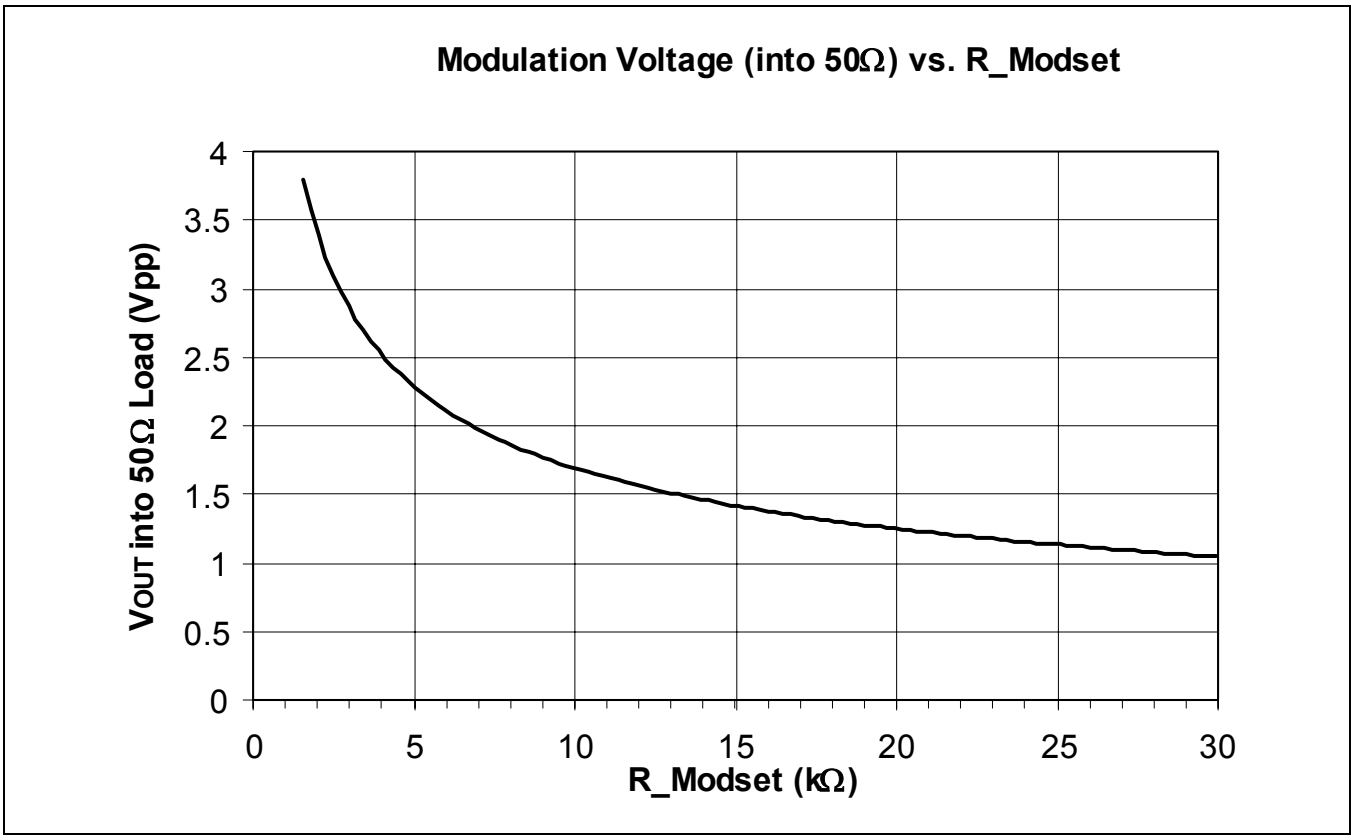
1.5.1 Step 1: Choosing R_{MOD}

Chose the value of R_{MOD} from Figure 1-11 depending on the value of peak-to-peak output voltage required. The approximate relationship is:

$$R_{MODSET} = [(27.3 * 450 * 1.28) / (V_{MOD})] - 3.26\ k\Omega$$

This value should be the nominal cold temperature value. Steps 3 and 4 show how to increase the modulation current with temperature to compensate for laser diode characteristics.

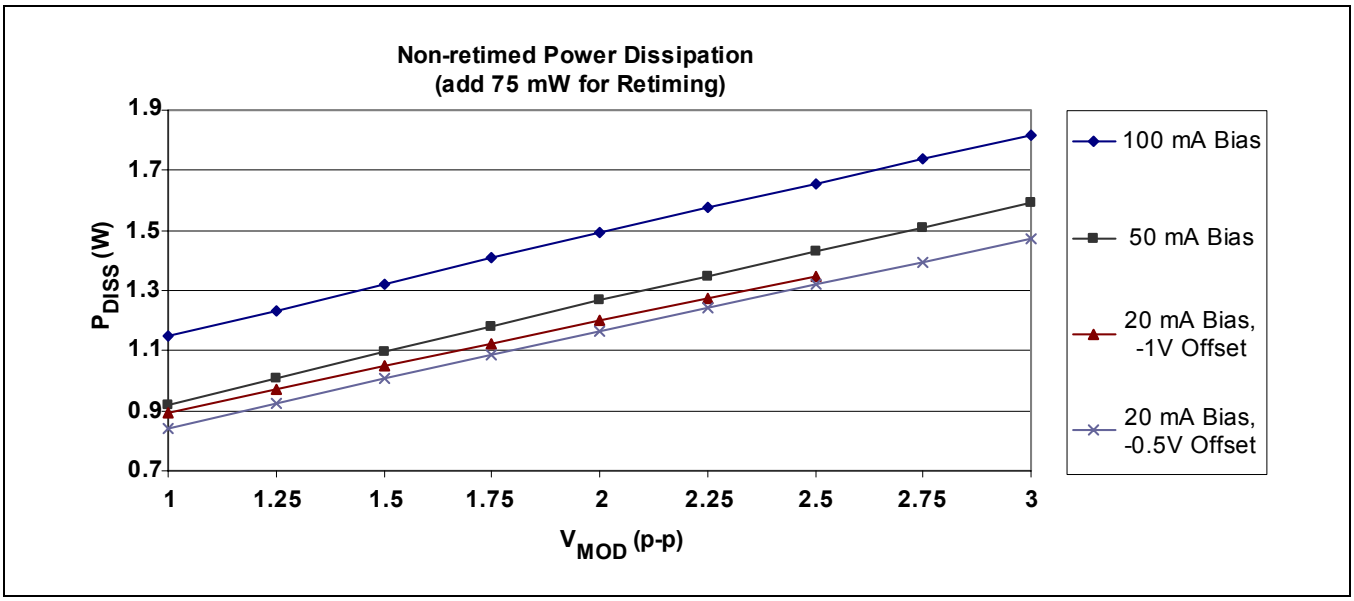
Figure 1-11. Modulation Voltage (into 50 ohm) vs. R_Modset



1.5.2 Step 2: Calculate Power Dissipation

Using Figure 1-12 below, determine the power dissipation for your application.

Figure 1-12. Non-retimed Power Dissipation



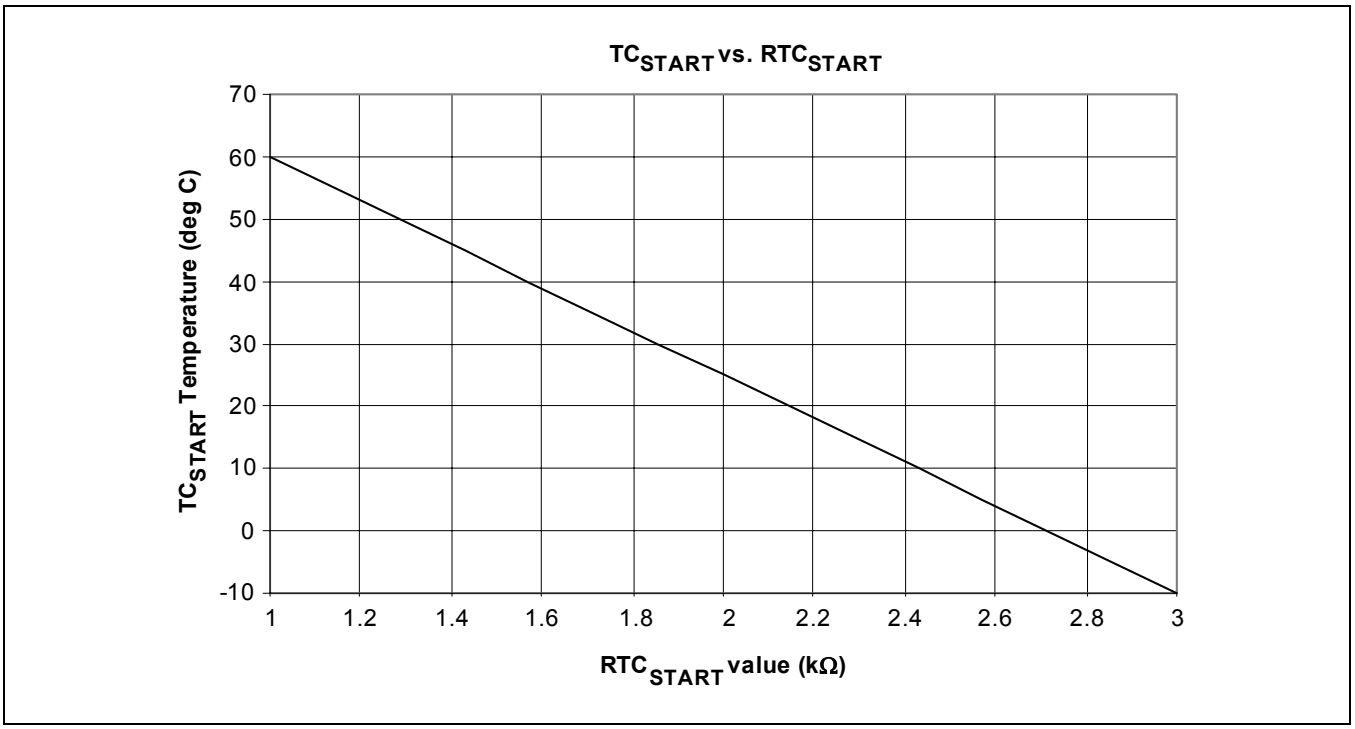
1.5.3 Step 3: Thermal Resistance

The thermal resistance of the package is 32°C/watt. Use this number to calculate the die temperature rise.

1.5.4 Step 4: Determine the value of RTC_{START}

The first step to calculating RTC_{START} is to determine the temperature rise of the die. Refer to Figure 1-13. This is the value at which the temperature compensation begins to increase the output modulation voltage. Along with RTC_{SLOPE}, it sets the value of modulation current increase at a given temperature.

Figure 1-13. TC_{START} vs. RTC_{START}



1.5.5 Step 5: Select RTC_{SLOPE}

The M02169 allows the user to compensate for the decrease in laser output power as temperature increases. Select the resistor value from the graphs below. Note that actual slope number is approximately linearly proportional to the RTC_{SLOPE} value. For example, using Figure 1-15 which has a TC_{START} value of 25°C, if it is desired to have the 85°C value for modulation current equal 1.5x the cold temperature value established with R_{MOD} as in step 1 of this procedure (nominal modulation current), then RTC_{SLOPE} = (25 kΩ + 50 kΩ)/2 = ~37.5 kΩ should be used. Also notice that Figure 1-14 uses a start value of approximately -10°C and Figure 1-15 uses a start value of ~25°C. The actual start value is established in Step 4.

Figure 1-14. RTC_{START} = 3.0 k ohm

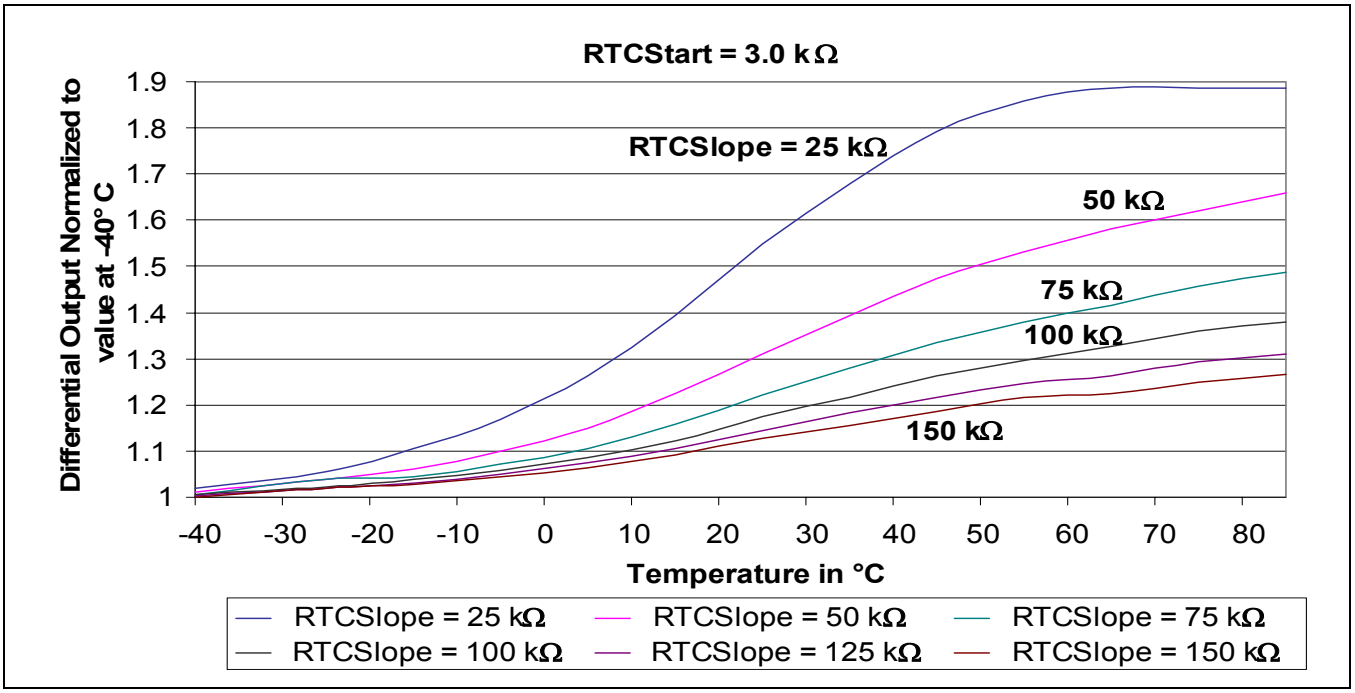
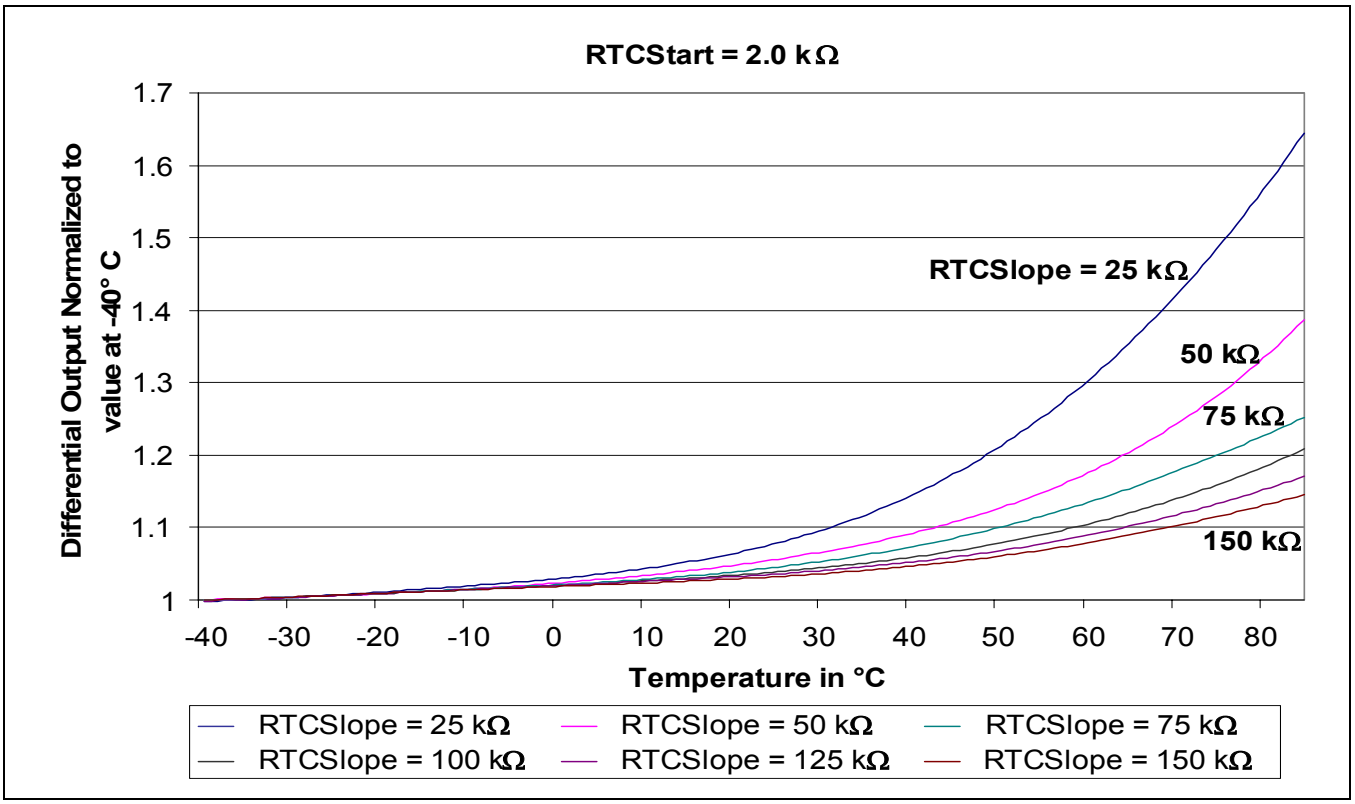


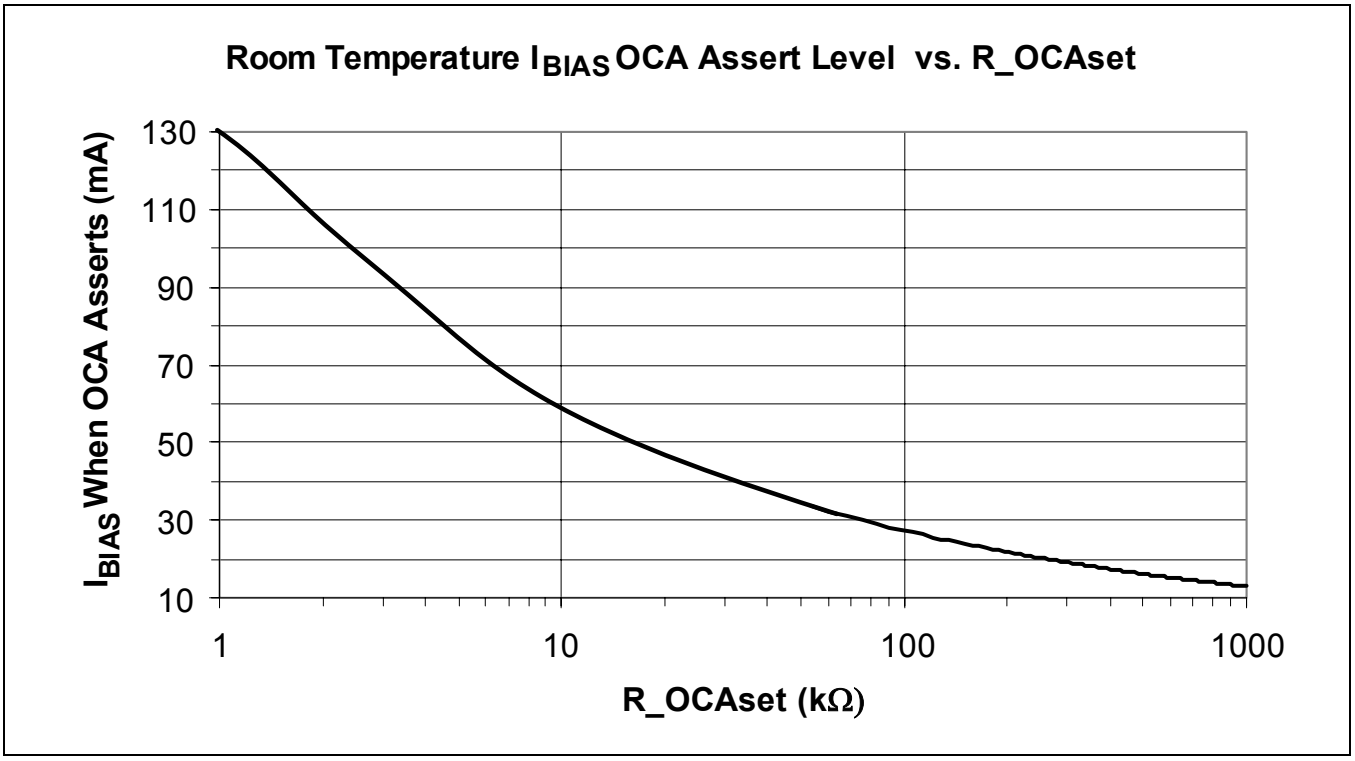
Figure 1-15. RTC_{START} = 2.0 k ohm



1.5.6 Step 6: Select ROCA$_{SET}$

The M02169 allows the user to limit the maximum I_{BIAS} current to roughly 10% above the OCA$_{SET}$ level. This relationship is shown below in Figure 1-16. When the Bias current exceeds the OCA$_{SET}$ level, the OCA flag is asserted, but not latched.

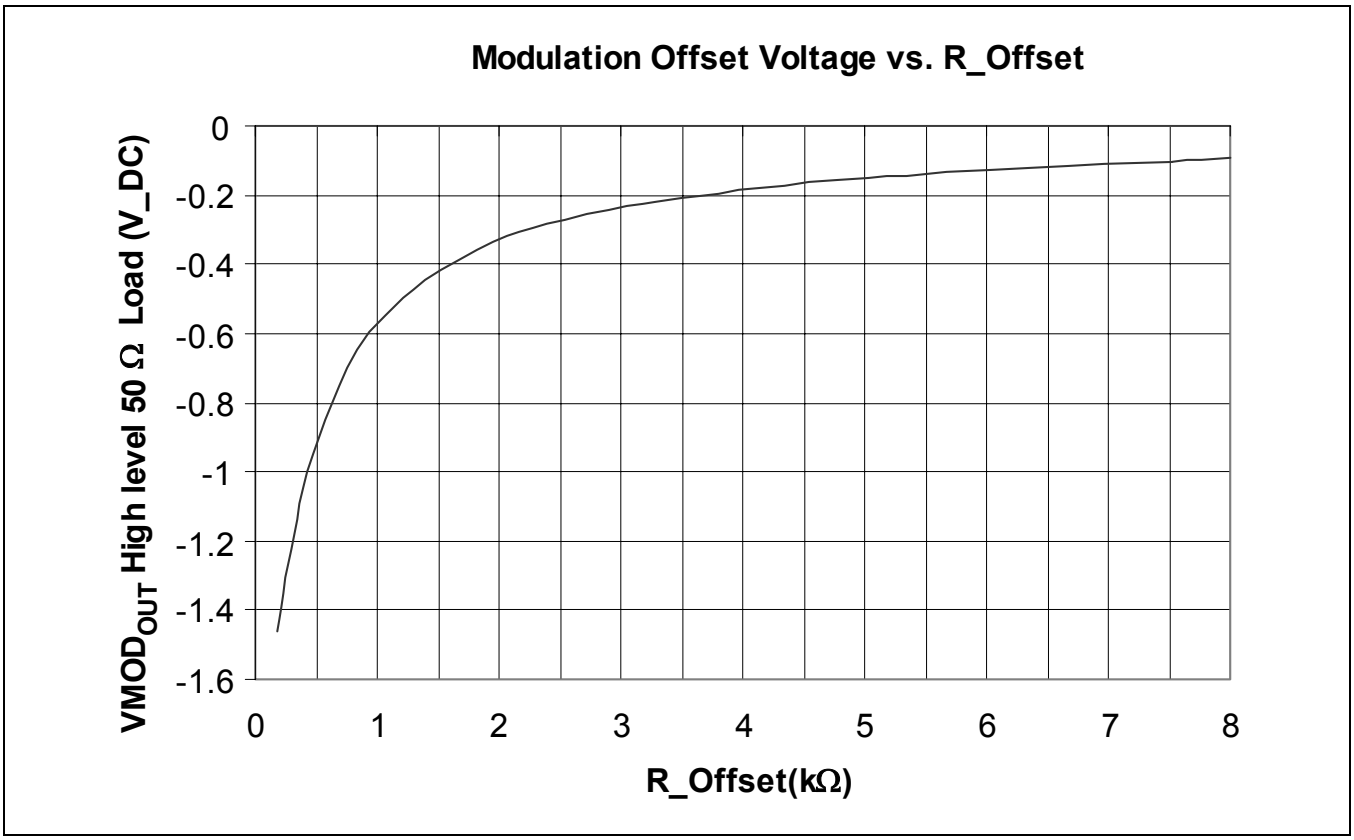
Figure 1-16. Room Temperature I_{BIAS} OCA Assert Level vs. R_OCAset



1.5.7 Step 7: Integrated Output Offset Control (EAM)

The M02169 contains an integral output offset control for reverse biasing an EAM. The relationship of R_Offset and the output voltage is given below in Figure 1-17.

Figure 1-17. Modulation Offset Voltage vs. R_Offset



1.5.8 Step 8: Automatic Power Control (EAM)

The M02169 APC and bias outputs may be used for providing the bias on direct modulated lasers, or as the bias controller for the laser portion of an integrated EAM. When used to bias an integrated EAM, an external current mirror is used. Figure 1-19 in this data sheet shows such an example with the mirror ratio set to 5.

Realistic mirror ratios may be as high as 20, and the external current mirror also serves to reduce the overall power dissipation in the M02169. R_{OCASET} should be set to limit the bias current to the minimum level necessary taking into account the gain of the current mirror. Using Figure 1-19 as an example, the bias current mirror gain is 5 and R_{OCASET} should be set to allow a maximum bias current of no more than 25 mA.

1.6 Applications

Figure 1-18. Application Block Diagram (1) Direct Modulated Laser (DML)

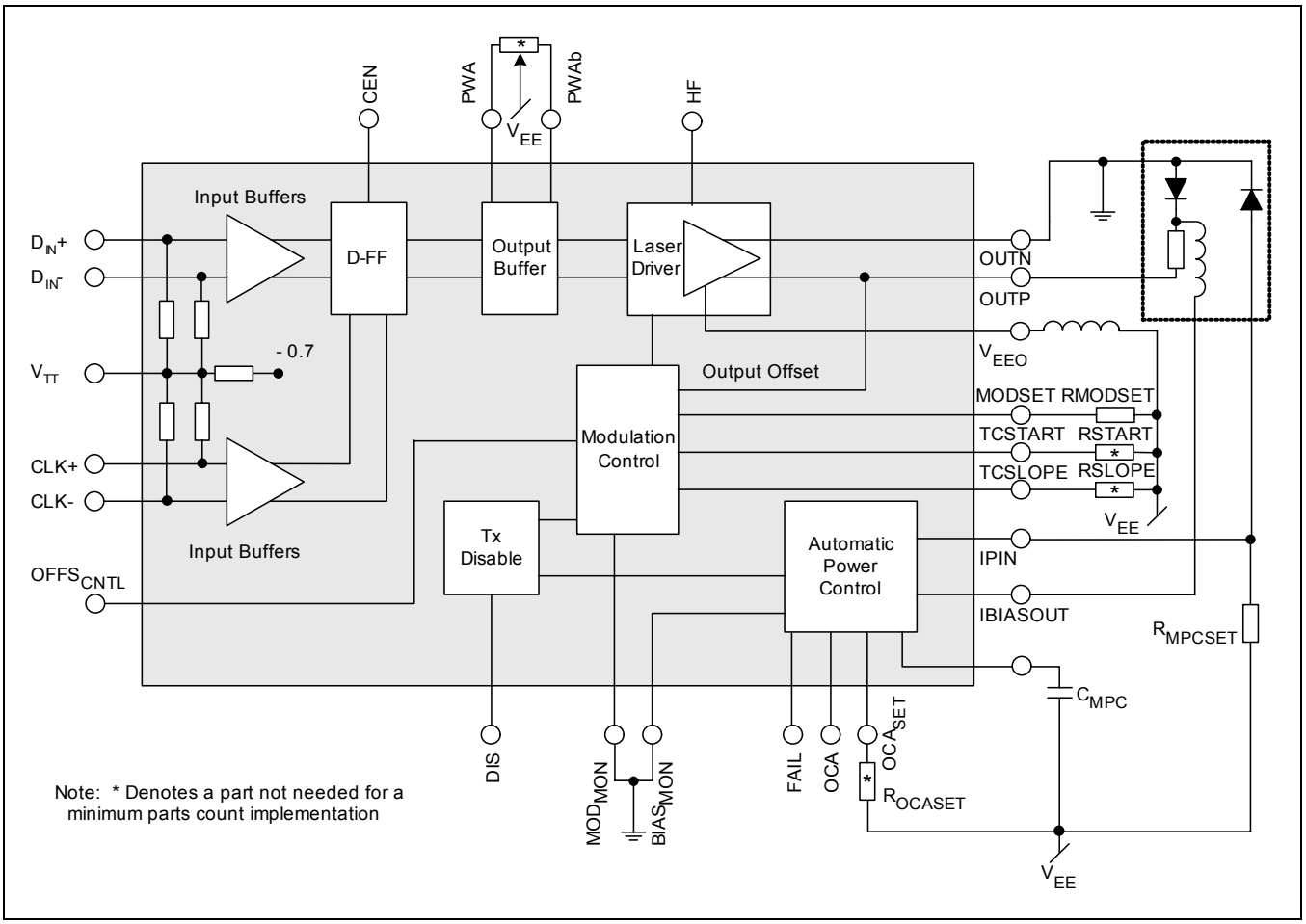
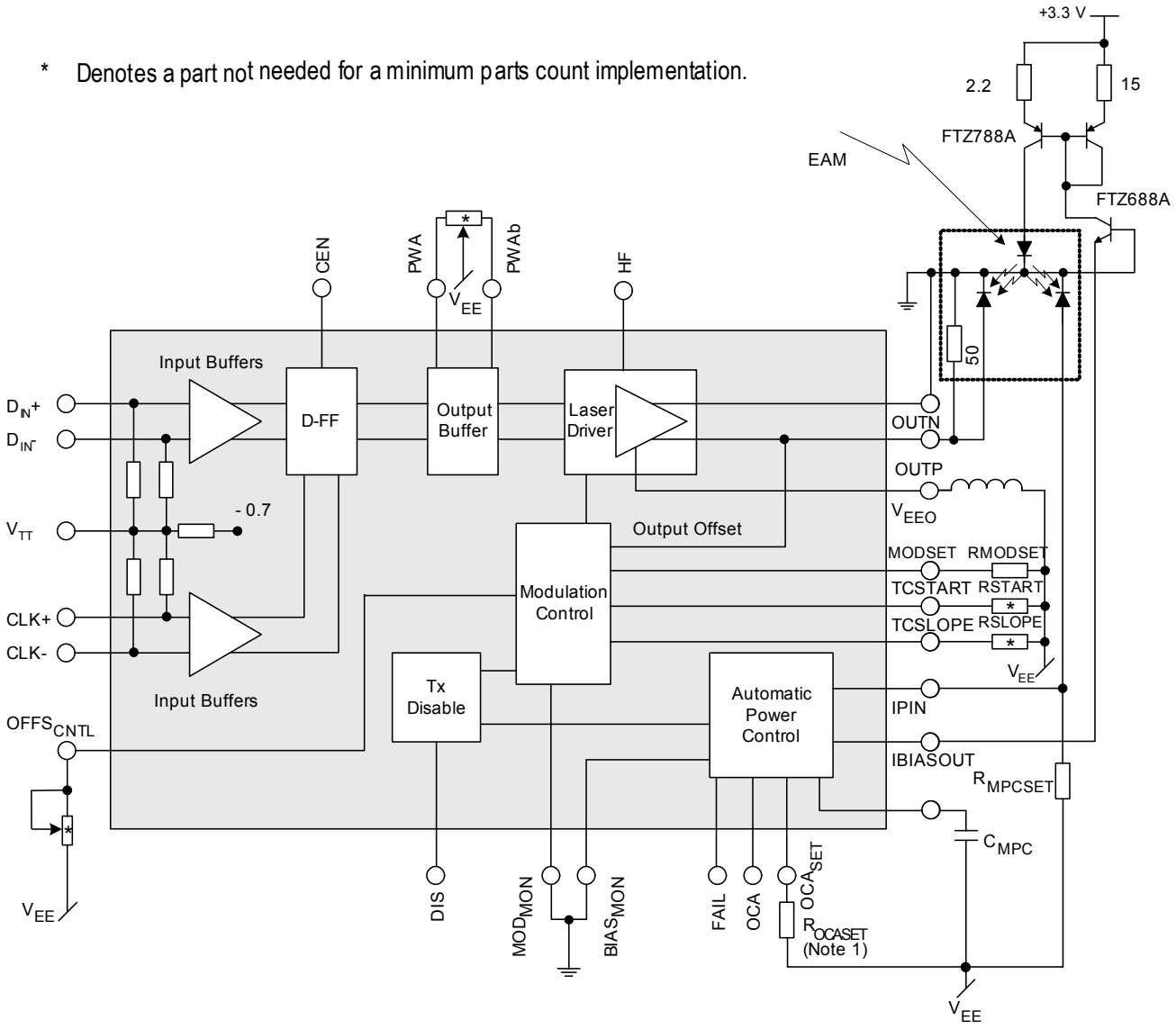


Figure 1-19. Application Block Diagram (2) Electro-Absorbtive (EA) Laser



Note:
1. R_{OCASET} should be set to limit the bias current to the minimum level necessary. Using the above components, the bias current mirror gain is 5 and R_{OCASET} should be set to allow a maximum bias current of no more than 25 mA.

1.7 Pin Definitions

Table 1-1. Pin Description

QFN Pin Number	Name	Function
1	PWAb	Negative pulse width adjust input. A potentiometer between this pin and PWA adjusts output pulse width. Connect PWA and PWAb to V_{EE} to disable this function (3)
2	GND	Ground (4)
3	D_{IN}+	Positive data input (CML or AC coupled PECL) - Self biased if V_{TT} left floating
4	D_{IN}-	Negative data input (CML or AC coupled PECL) - Self biased if V_{TT} left floating
5	V_{TT}	Termination for 50 Ω CML inputs; connect to ground for DC coupled clock and data inputs, leave floating to AC couple clock and data inputs
-	V_{EE}	Power supply (4)
6	CLK+	Positive clock input (CML or AC coupled PECL). Self Biased if V_{TT} left floating. Can leave disconnected if not used. Data re-timed on rising edge
7	CLK-	Negative clock input (CML or AC coupled PECL). Self Biased if V_{TT} left floating. Can leave disconnected if not used. Data re-timed on falling edge
8	GND	Ground
9	CEN	Clock enable input. Set high to use CLK inputs, Low or floating when not using CLK Inputs (direct data). 80 kΩ internal pull-down to V_{EE}
10	DIS	Bias (1) and Modulation Output Disable (TTL/CMOS). Set low or leave floating for normal operation. 80 kΩ internal pull-down to V_{EE}. When high, will disable the bias and modulation outputs.
11	GND	Ground
12	$BIAS_{MON}$	Bias output current monitor. See functional description for detailed information. Connect directly to GND if not used
13	MOD_{MON}	Modulation output current monitor. See functional description for detailed information. Connect directly to GND if not used
14	FAIL	Automatic Power Control Failure indicator. Goes high when automatic power control loop is not able to maintain constant power (1)
15	OCA	Laser over-current alarm. Goes high when laser bias current exceeds level set at OCA_{SET} (1)
16	HF	Output compensation control. Set high (GND) for normal operation. When low or floating, output overshoot is decreased and edge speed is slightly slower
17	I_{PIN}	Monitor photodiode input. Connect this input to the monitor photodiode anode for automatic power control. A resistor connected from this pin to V_{EE} sets laser output power. Leave floating if not using automatic power control (3)
18	$I_{BIASOUT}$	Laser bias current output. Connect to laser cathode for DML applications using automatic power control(1). Connect to V_{EE} when not using automatic power control
19	OUTN	Negative modulation output. Draws current when D_{IN}+ is high. Internally terminated with 50Ω. Connect directly to ground (2)
20	OUTP	Positive modulation output. Draws current when D_{IN}+ is low. Offset adjustment is integrated into this output and controlled by $OFFS_{CNTL}$
21	OUTN	Negative modulation output. Draws current when D_{IN}+ is high. Internally terminated with 50Ω. Connect directly to ground (2)
22	NC	Not used; can connect to V_{EE}, ground or leave floating

Table 1-1. Pin Description

QFN Pin Number	Name	Function
23	V_{EEO}	Power supply for modulation output stage (4)
24	V_{REG}	Internal regulator voltage. Leave floating
25	C_{MPC}	A capacitor from this pin to V_{EE} sets the dominant pole for automatic power control. Capacitor not required if APC loop is not used (3)
26	$OFFS_{CNTL}$	Offset control input. A resistor between this pin and V_{EE} sets the offset level at OUTP. Leave floating if not used
27	TC_{SLOPE}	Connecting a resistor between this pin and V_{EE} sets the temperature coefficient of modulation current. Leave floating if not used (3)
28	TC_{START}	A resistor from this pin to V_{EE} sets the temperature at which the temperature coefficient of modulation current (set by TC_{SLOPE}) is activated. Leave floating if not used (3)
29	GND	Ground (4)
30	MOD_{SET}	Modulation current adjust. Connect a resistor between this pin and V_{EE} to set laser modulation current(3)
31	OCA_{SET}	Temperature-dependent bias current limit. OCA is asserted when this limit is exceeded. Connect a resistor between this pin and V_{EE} to set limit. Defaults to maximum (100 mA) if connected to V_{EE}. Leave floating if not using automatic power control circuitry (3)
32	PWA	Positive pulse width adjust input. A potentiometer between this pin and PWAb adjusts output pulse width. Connect PWA and PWAb to V_{EE} to disable this function. (3)
Center pad	V_{EE}	Power supply (must be connected to lowest potential) (4)

Notes:
(1)When using the internal bias current source in DML applications or with an external current mirror as shown in Figure 1-19 for EAM applications.
(2)Both sets of OUTN pads or terminals, when connected, result in a 25 Ω load.
(3) See additional information in the detailed description.
(4) For +5 V operation, the M02169 V_{EE} pins are connected to system ground and the M0269 GND pin is connected to system V_{CC} (+5.0). All connections in the applications diagrams referenced to V_{EE} are now referenced to system ground and all M02169 connections referenced to ground are now referenced to system V_{CC}.

2.0 Product Specification

2.1 Absolute Maximum Ratings

Table 2-1. Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{EE}	Power supply voltage	-6.0 to +0.4	V
T_A	Operating ambient temperature	-40 to +85	°C
T_{STG}	Storage temperature	-65 to +150	°C
$I_{BIASOUT\ (MAX)}$	Maximum bias output current	120	mA
$V_{OFFS\ (MAX)}$	Maximum output offset voltage (1)	1.5 (into 50 Ω load at OUTP)	V
$V_{MOD\ (MAX)}$	Maximum modulation voltage (1)	3.6 (into 50 Ω load at OUTP)	V
$I_{MOD\ (MAX)}$	Maximum modulation current	80	mA
PWA, PWAb	Pulse width adjust	-2 to V_{EE}	V
D_{IN}+/-, CLK+/-	Data and clock inputs	-2 to +0.4	V
HF, CEN, DIS	Mode control inputs	V_{EE} to +0.4	V
$BIAS_{MON}$, MOD_{MON}	Bias and modulation output current mirror compliance voltage	V_{EE} to +0.4	V
I_{PIN}	I_{PIN} voltage	V_{EE} to V_{EE} + 3.6	V
V_{TT}	Termination voltage	-2 to +0.4	V
FAIL, OCA, OCA_{SET}, MOD_{SET}, $OFFS_{CNTL}$	Status flags and set inputs	V_{EE} to V_{EE} + 3.6	V
TC_{START}	Temperature compensation start	V_{EE} to V_{EE} + 1	V
TC_{SLOPE}	Temperature compensation slope	V_{EE} to V_{EE} + 3.6	V
OUTP	Modulator output	V_{EE} to +0.4	V

Note:
(1) EAM applications.

These are the absolute maximum ratings at or beyond which the IC can be expected to fail or be damaged. Reliable operation at these extremes for any length of time is not implied.

2.2 Recommended Operating Conditions

Table 2-2. Recommended Operating Conditions

Parameter	Rating	Units
Power Supply	5.0 +/- 5%, -5.2 +/- 5%	V
Operating Ambient	-40 to +85	°C

2.3 DC Characteristics

(V_{EE} = -4.75 to -5.46 V, T_A = -40 to +85 °C, HF = high, V_{OUTP} = 2.5Vpp, V_{OFFS} = 0.5V, unless otherwise noted)

Table 2-3. DC Electrical Characteristics

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
I_{EE}	Supply current	No retiming (CEN low)(1) With retiming and max. modulation(1)		155 190	180 215	mA
I_{BIAS}	Bias current adjust range	Limited by OCA_{SET} across temperature range; $V(I_{BIASOUT}) > V_{EE}$ + 1 V	1		100	mA
$I_{BIAS(OFF)}$	Bias current with output disabled	DIS = high		30	300	µA
	Ratio of I_{BIAS} current to $BIAS_{MON}$ current	$V(BIAS_{MON}) > V_{EE}$ + 1 V		60		A/A
I_{OCA}	Bias current limit adjustment range	Point at which OCA asserts	15 (2)		100 (3)	mA
V_{OFFS}	Offset voltage adjust range	Below GND; OUTP terminated into 50 Ω load, V_{MOD} = 0 V	0		1	V
	Ratio of offset voltage to current at $OFFS_{CNTL}$	OUTP terminated into 50 Ω load		0.52		V/mA
V_{MD}	Monitor diode reverse bias voltage	= -V(I_{PIN})		3.8		V
I_{MD}	Monitor diode current adjustment range	Guaranteed by design	10		1500	µA
CEN, DIS	Logic input high voltage		V_{EE}+3.0		0	V
CEN, DIS	Logic input low voltage		V_{EE}		V_{EE}+0.8	V
FAIL, OCA	Logic output high voltage		V_{EE}+3.0		V_{EE}+3.6	V
FAIL, OCA	Logic output low voltage		V_{EE}		V_{EE}+0.4	V

Table 2-3. DC Electrical Characteristics

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
R_{IN}	Single-ended input impedance	Data and clock inputs (inputs terminated to V_{TT})	40	55	60	W
R_{OUT}	Single-ended output termination resistance	OUTP to GND	48	60	72	W
V_{SELF}	Self-biased common mode input voltage	V_{TT} left floating		-0.75		V
V_{INCM}	Common-mode input compliance voltage	Data and clock inputs (4)	-0.8		$-V_{IN(DIFF)}/4$	V
$V_{IN(DIFF)}$	Differential input voltage	$=2*(DIN+_{HIGH}-DIN+_{LOW})$ (4) (clock inputs follow same relationship)	300		1600	mV

Notes:
(1). Excludes output modulation, bias, and/or offset current
(2). Minimum set point at T_A = +25 °C
(3). Default value at T_A = +85 °C with OCA_{SET} connected to V_{EE}
(4).See Figure 2-1

2.4 AC Characteristics

(V_{EE} = -4.75 to -5.46 V, T_A = -40 to +85 °C, HF = high, V_{OUTP} = 2.5Vpp, V_{OFFS} = 0.5V, unless otherwise noted)

Table 2-4. AC Electrical Characteristics

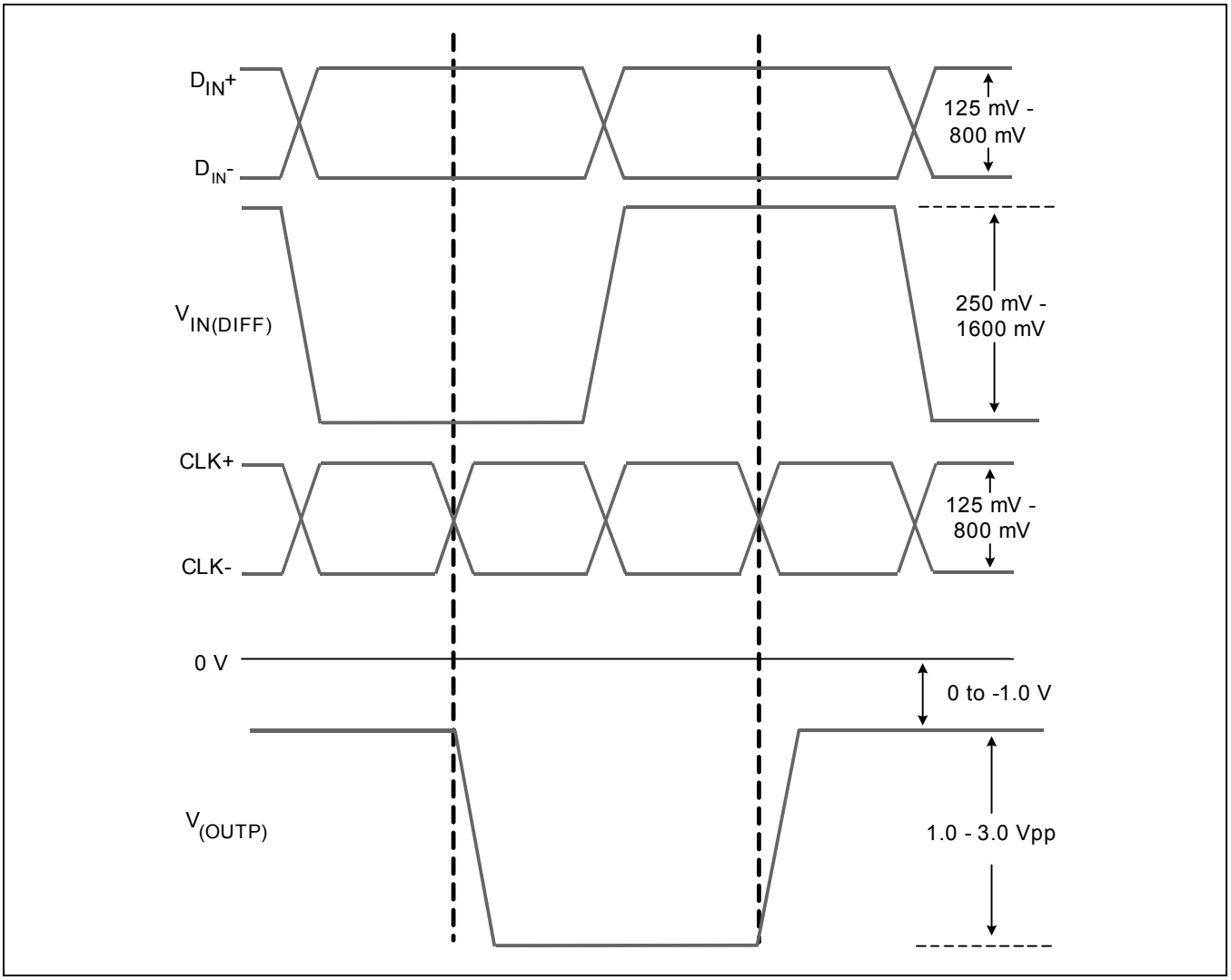
Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{MOD}	Modulation voltage adjust range	OUTP terminated into 50 Ω load	1		3 (1)	V_{PP}
$V_{MOD(OFF)}$	Modulation voltage with output disabled	OUTP terminated into 50 Ω load; DIS = high			15	mV_{PP}
$V_{MOD(PP)}/I_{MODMON}$	Ratio of peak to peak modulation voltage to MOD_{MON} current	OUTP terminated into 50 Ω load; $V(MOD_{MON}) > V_{EE}$ + 2 V		830		mV/mA
I_{MOD-TC}	Programmable range for modulation current temperature coefficient	Adjustable using TC_{SLOPE} (2)	500		10^4	ppm/°C
$T_{TCSTART}$	Programmable temperature at which modulation current TC compensation enables	Dependent upon TC_{START} value (2)	0		60	°C
tr	Modulation output rise time	20% to 80% into 50 Ω load. Measured using alternating 1-0 pattern at 2.5 Gbps		26	34	ps
tf	Modulation output fall time	20% to 80% into 50 Ω load. Measured using alternating 1-0 pattern at 2.5 Gbps		23	31	ps
OS	Overshoot of modulation output	OUTP terminated into 50 Ω load		2		%
T_S	Setup time	Referenced to 50% transition point of non-inverting clock input going high (CLK+)		15		ps

Table 2-4. AC Electrical Characteristics

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
T_H	Hold time	Referenced to 50% transition point of non-inverting clock input going high (CLK+)		15		ps
PWA	Pulse width adjust range	Measured using 1-0 pattern at 10 Gbps		± 20		ps
RJ	Random jitter, rms			0.3		ps
DJ	Modulation output deterministic jitter	Peak-to-peak. Measured into 50 Ω load using 2^{23}-1 PRBS at 10 Gbps; using clock inputs (includes PWD)		8	15	ps
S11	Input return loss	Data and clock inputs; 50 MHz to 10 GHz		-15		dB
S22	Output return loss	50 MHz to 10 GHz		-10		dB

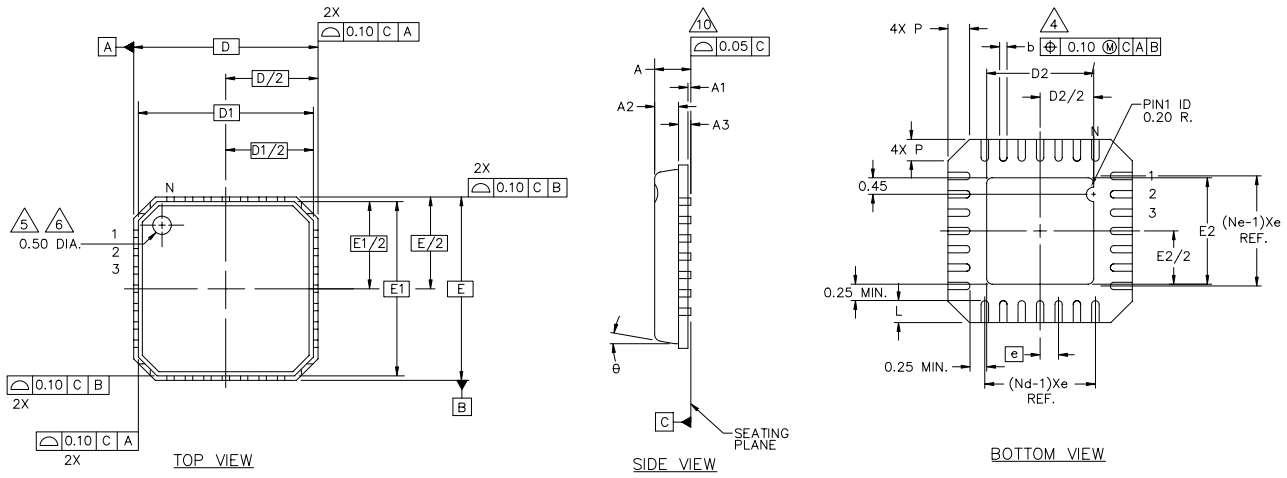
Notes:
(1) $|V_{EE}| - V_{MOD} - V_{OFFS} > 1.7$ V. Output swing can extend beyond this range but AC specifications may not be met.
(2) Guaranteed by design and characterization.

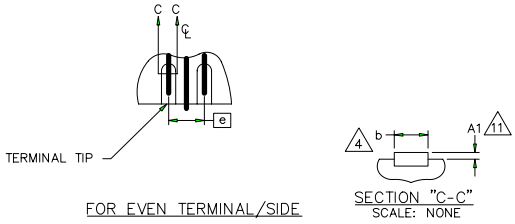
Figure 2-1. Data and Clock Input Requirements, Output Description



2.5 Package Specification

Figure 2-2. QFN32 Package Information





Note: View is for a 28 pin package. All dimensions in the tables apply for the 32 pin package

SYMBOL	PITCH VARIATION D			NOTE
	MIN.	NOM.	MAX.	
e		0.50 BSC		
N		32		3
Nd		8		3
Ne		8		3
L	0.30	0.40	0.50	
b	0.18	0.23	0.30	4
Q	0.00	0.20	0.45	
D2	3.15	3.30	3.45	
E2	3.15	3.30	3.45	

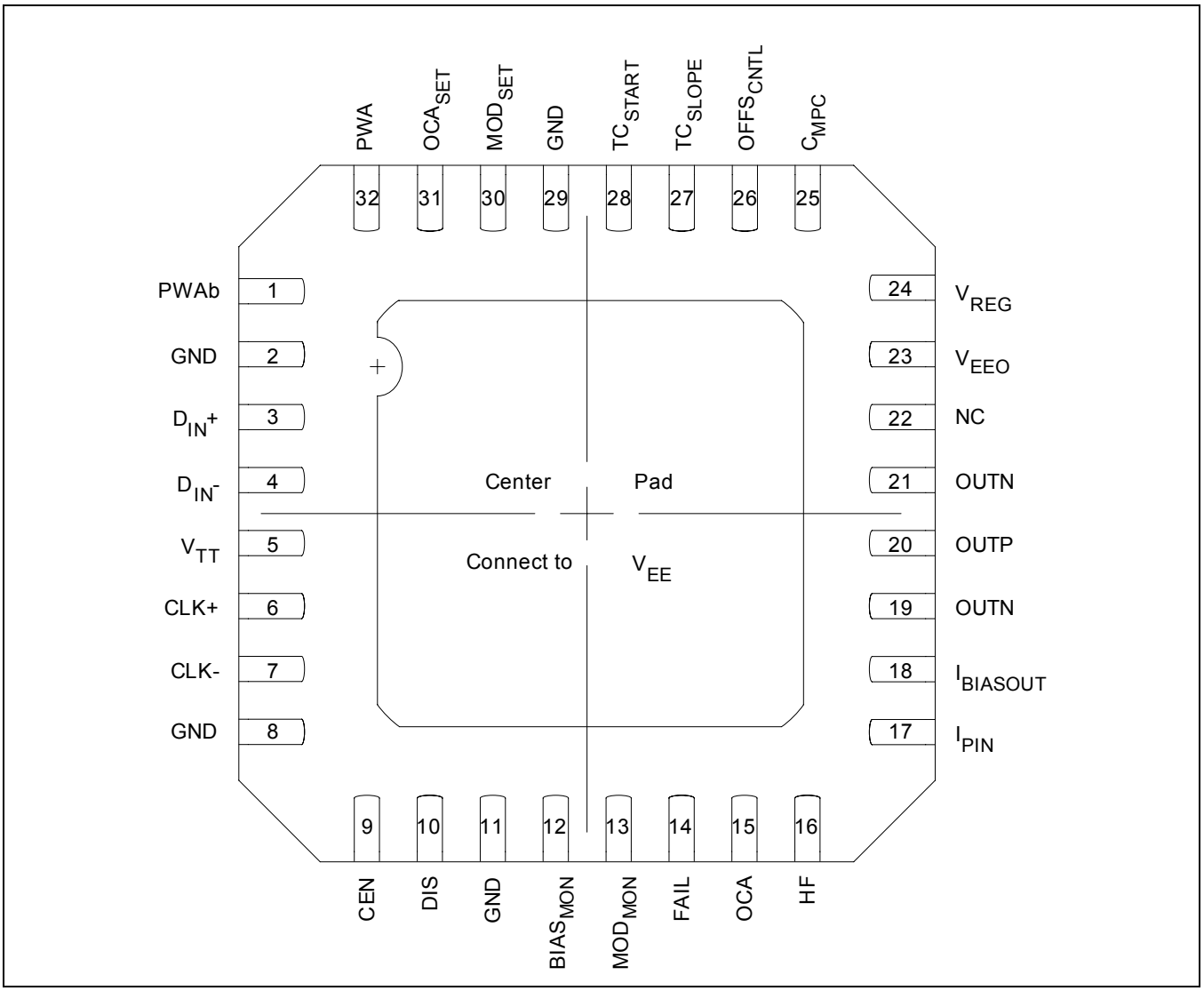
SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	-	0.85	0.90	
A1	0.00	0.01	0.05	11
A2	-	0.65	0.70	
A3		0.20 REF.		
D		5.00 BSC		
D1		4.75 BSC		
E		5.00 BSC		
E1		4.75 BSC		
θ			12°	
P	0.24	0.42	0.60	
R	0.13	0.17	0.23	

NOTES:

2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. - 1994.
3. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X-DIRECTION &
   Ne IS THE NUMBER OF TERMINALS IN Y-DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. THE SHAPE SHOWN ON FOUR CORNERS ARE NOT ACTUAL I/O.
9. PACKAGE WARPAGE MAX 0.05mm.
10. APPLIED FOR EXPOSED PAD AND TERMINALS.
    EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
11. APPLIED ONLY FOR TERMINALS.

2.6 Pinout Information

Figure 2-3. QFN32 Pinout Information



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