EM78P5840/41/42

8-BIT MICRO-CONTROLLER

Version 2.6

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Version History

Specification Revision History	
Version	Content
eFHP5830B	
1.0	Initial version
eFHP5840	
2.0	1. Change counter1 external input pin from PC2 to P94 2. Modify P60, P61 to INPUT/OUTPUT IO 3. Remove P71 internal pull high function 4. Modify control register initial value 5. Remove 256 byte Data RAM 6. Remove SPI function 7. Add IRC and ERIC oscillator function 8. Decrease Stack from 16 to 8 9. Add Counter1 external source (from IO pad) 10. Remove Counter2
2.1	1. Add the relative of ERIC oscillating frequency and external R
2.2	1. Add IRC mode CLK trimming control in code option. 2. Modify PORT9 sink/driver current.
2.3	1. Rename “ERC mode” to “ERIC mode” 2. Modify the relative between ERIC mode’s oscillating CLK and the value of external resister.
2.4	1. Change pin name from “ERCI” to “ERIC” 2. Change the descript about CONT reg bit7
2.5	1. Remove Crystal mode’s Idle application 2. Modify operating temperature
2.6	1. Rename eFH78P5840/41/42 →EM78P5840/41/42 2. Change IRC frequency deviation from +/- 5% to +/- 10%

Relative to EM785840’s ROM-less, OTP and mask:

ROM-less	OTP	Mask
ICE5830	EM78P5840 EM78P5841 EM78P 5842	EM785840 EM785841 EM785842

Table1: the relation between EM78P5830 and EM78P5840 series:

EM78P5830 series	EM78P5840 series	PACKAGE
EM78P5830CP EM78P5830ACP	EM78P5840P	18 pin PDIP
EM78P5830CM EM78P5830ACM	EM78P5840M	18 pin SOP
EM78P5830BP EM78P5830ABP	EM78P5841P	20 pin PDIP
EM78P5830BM EM78P5830ABM	EM78P5841M	20 pin SOP
EM78P5830FP EM78P5830AFP	EM78P5842P	24 pin PDIP
EM78P5830FM EM78P5830AFM	EM78P5842M	24 pin SOP

Table2: the major differences between EM78P5830 and EM78P5840 series:

	EM78P5830 series	EM78P5840 series
CID RAM	256 byte	NA
ERIC mode	NA	Under 6M Hz
IRC mode	NA	2M / 4M Hz
WDT source	Crystal or PLL	IRC1
External CNT1 input	NA	Shared with P94
P71 pull high	Internal pull high	External pull high
/RESET pin	/RESET only	Shared with P71
PLLC pin	PLLC only	Shared with P70 and ERCI
XIN, XOUT	Crystal input	Shared with P60 and P61

Table3: the major differences between ICE5840, EM78P5840 and EM785840:

	ICE5840	EM78P5840 series	EM785840 series
CID RAM	1024 byte	NA	NA
CID RAM address auto +1	V	NA	NA
CNT1 (**)	8 bit counter	8 bit counter	8 or 16 (shared with CNT2) bit counter
CNT2 (**)	V	X	V
STACK	12	8	8

** CNT2 is only exist on EM78P5840/41/42 and EM785840/41/42, CNT2 is un-support on ICE5840.

Table4: Differences between EM78P5840, EM78P5841 and EM78P5842:

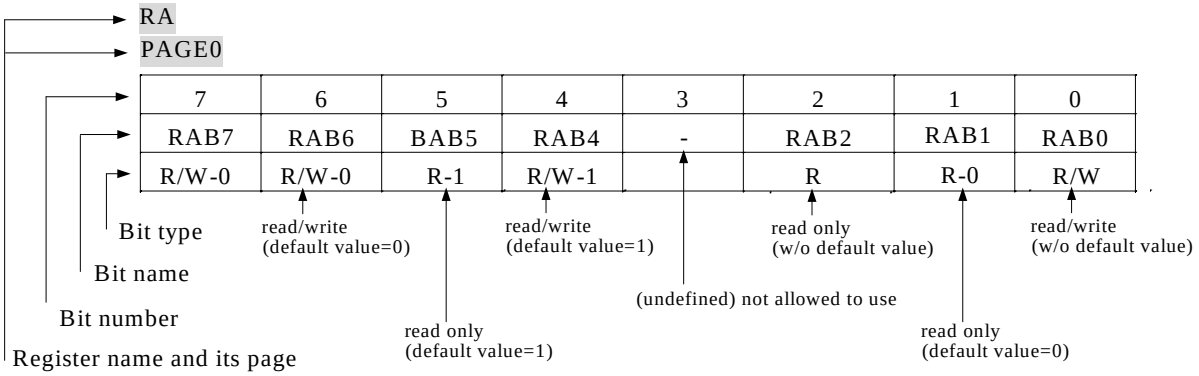
	EM78P5840	EM78P5841	EM78P5842
Pin count	18	20	24
PWM	X	2 channel	2 channel
IO (MAX)	16	18	22

User Application Note

(Before using this chip, take a look at the following description note, it includes important messages.)

1. There are some undefined bits in the registers. The values in these bits are unpredicted. These bits are not allowed to use. We use the symbol "-" in the spec to recognize them. ***A fixed value must be write in some specific unused bits by software or some unpredicted wrong will occur.***

2. You will see some names for the register bits definitions. Some name will be appear very frequently in the whole spec. The following describes the meaning for the register's definitions such as bit type, bit name, bit number and so on.



3. Always set IOCC PAGE1 bit 0 = 1 otherwise partial ADC function cannot be used (in ICE5830).

4. Please do not switch MCU operation mode from normal mode to sleep mode directly. Before into sleep mode, please switch MCU to green mode.

5. While switching main clock (regardless of high freq to low freq or on the other hand), adding 6 instructions delay (NOP) is required.

6. Offset voltage will effect ADC's result, please refer to figure 19 to detail.

7. Please do not connect unnecessary circuit on OTP burner pins during burning the OTP ROM.

I. General Description

The EM78P5840 series are 8-bit RISC type microprocessor with low power, high speed CMOS technology. There are 4Kx13 bits Electrical One Time Programmable Read Only Memory (OTP-ROM) within it. It provides security bits and some One time programmable Option bits to protect the OTP memory code from any external access as well as to meet user's options.

This integrated single chip has an on_chip watchdog timer (WDT), program OTP-ROM, RAM, programmable real time clock/counter, internal interrupt, power down mode, dual PWM (Pulse Width Modulation), 8-channel 10-bit A/D converter and tri-state I/O.

II. Feature

CPU

・Operating voltage : 2.2V~5.5V at main CLK less then 3.58MHz.

Main CLK(Hz)	Under 3.58M	14.3M
Operating Voltage(min)	2.2V	3.6V

・ 4k x 13 on chip Electrical One Time Programmable Read Only Memory (OTP-ROM)
・ 144 x 8 on chip general propose RAM
・ Up to 19 bi-directional and 3 input only general purpose I/O
・ 8 level stack for subroutine nesting
・ 8-bit real time clock/counter (TCC)
・ One 8-bit counter interrupt
・ On-chip watchdog timer (WDT)
・ 99.9% single instruction cycle commands
・ Three action modes in Crystal mode (Main clock can be programmed to 3.58M or 14.3M Hz)

Mode	CPU status	Main clock	32.768kHz clock status
Sleep mode	Turn off	Turn off	Turn off
Green mode	Turn on	Turn off	Turn on
Normal mode	Turn on	Turn on	Turn on

・ 2 level Normal mode frequency: 3.58M and 14.3MHz.
・ Input port interrupt function
・ Dual clocks operation (Internal PLL main clock , External 32.768KHz)

Operating frequency mode

・ Crystal mode (XIN,XOUT pin connect external crystal and capacitance)
・ ERIC mode (ERCI pin connect resister to VDD)
・ IRC mode

PWM

・ Dual PWM (Pulse Width Modulation) with 10-bit resolution
・ Programmable period (or baud rate)
・ Programmable duty cycle

ADC

・Operating : 2.5V 5.5V

Converter Rate	74.6K	37.4K	18.7K	9.3K
Operating Voltage(min)	3.5V	3.0V	2.5V	2.5V

・8 channel 10-bit successive approximation A/D converter
・Internal (VDD) reference voltage

POR

・Power-on reset

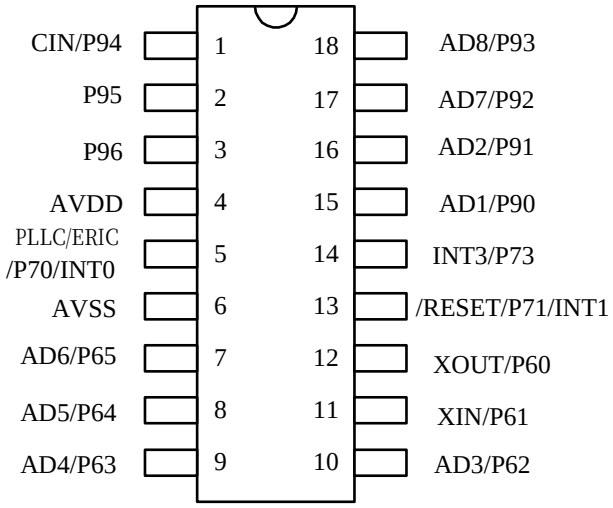
PACKAGE

EM78P5840M → 18 pin SOP, EM78P5841M → 20 pin SOP, EM78P5842M → 24 pin SOP
EM78P5840P → 18 pin PDIP, EM78P5841P → 20 pin PDIP, EM78P5842P → 24 pin PDIP

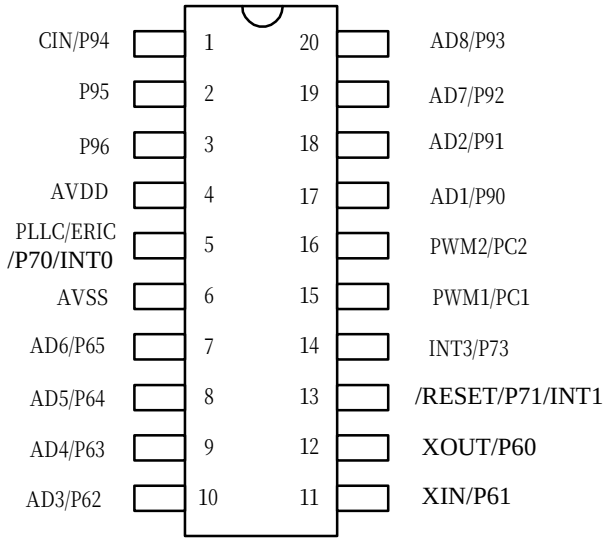
III. Application

General products application.

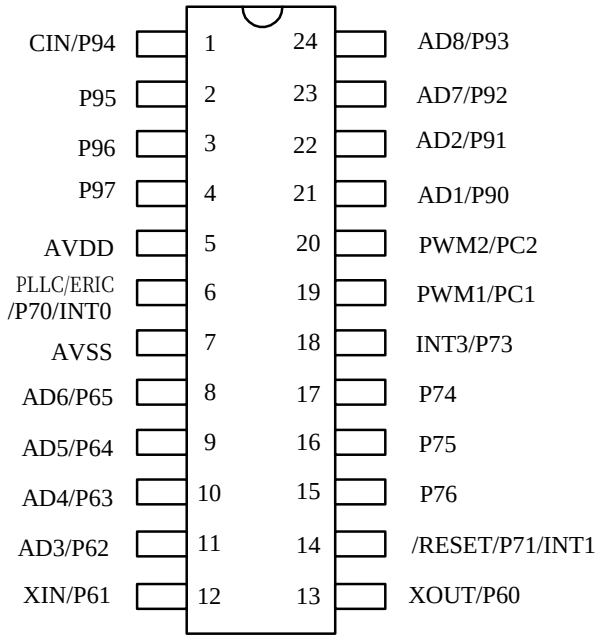
IV. Pin Configuration



(a)



(b)



(c)

Fig.1: EM78P5840 series pin assignment.
(a): EM78P5840M, EM78P5840P
(b): EM78P5841M, EM78P5841P
(c): EM78P5842M, EM78P5842P

V. Functional Block Diagram

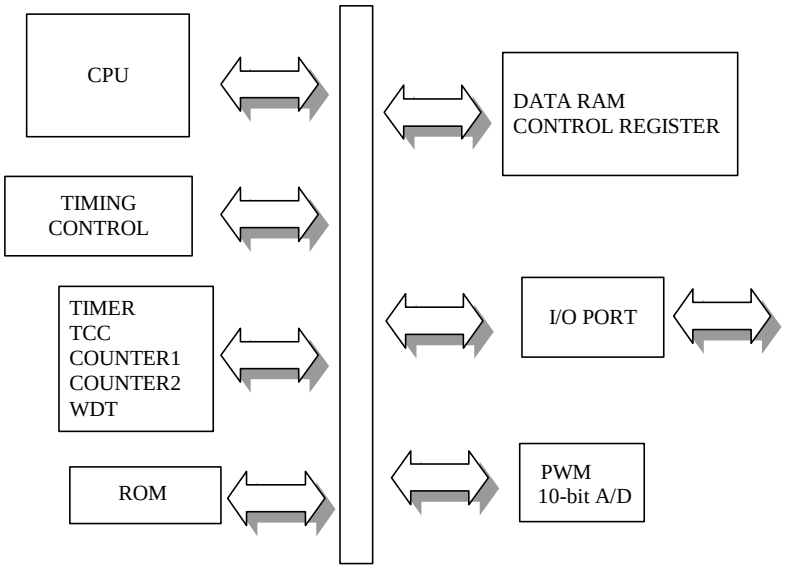


Fig.2a Block diagram

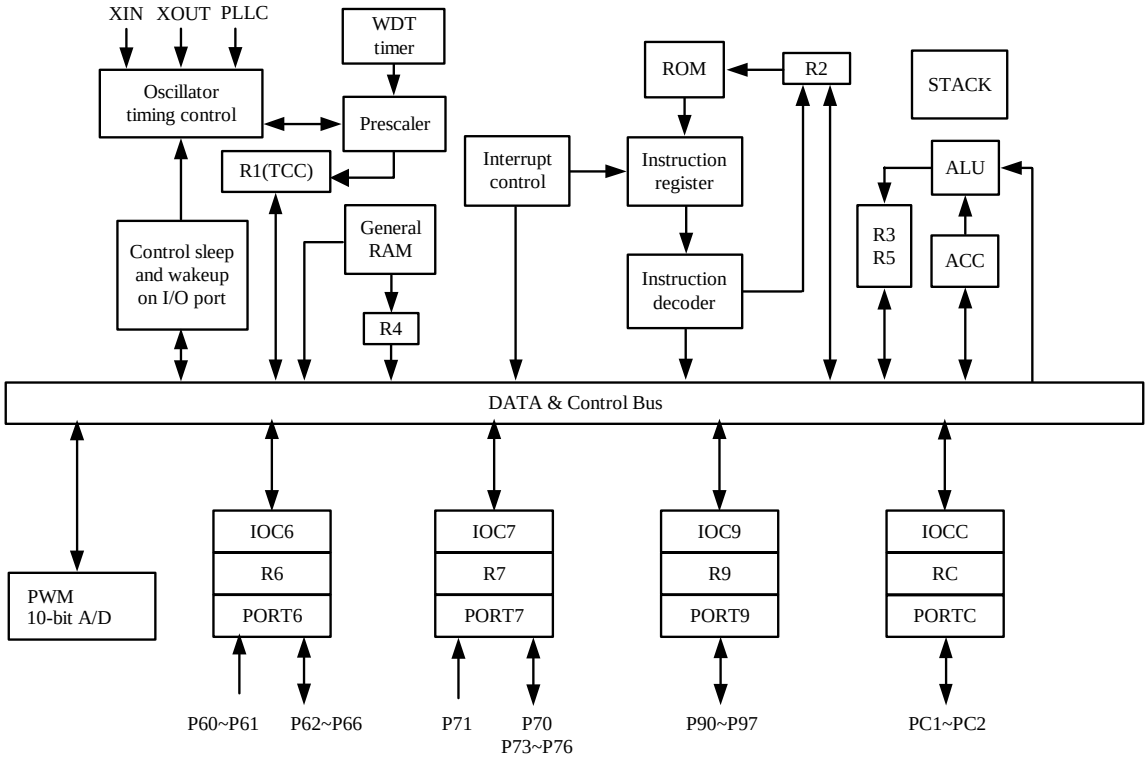


Fig.2b Block diagram

VI. Pin Descriptions

PIN	I/O	DESCRIPTION
POWER		
AVDD	POWER	Power
AVSS	POWER	Ground
CLOCK		
XIN	I	Input pin for 32.768 kHz oscillator
XOUT	O	Output pin for 32.768 kHz oscillator
PLLC	I	Phase loop lock capacitor, connect a capacitor 0.047u to 0.1u to the ground.
OSC	I	ERIC mode clock signal input. This pin is shared with PLLC.
CIN	I	Counter1 external CLK input. This pin is shared with P94. Note the frequency of the input CLK must less than 1M Hz.
10-bit 8 channel A/D		
AD1	I (P90)	ADC input channel 1. Shared with PORT90
AD2	I (P91)	ADC input channel 2. Shared with PORT91
AD3	I (P62)	ADC input channel 3. Shared with PORT62
AD4	I (P63)	ADC input channel 4. Shared with PORT63
AD5	I (P64)	ADC input channel 5. Shared with PORT64
AD6	I (P65)	ADC input channel 6. Shared with PORT65
AD7	I (P92)	ADC input channel 7. Shared with PORT92
AD8	I (P93)	ADC input channel 8. Shared with PORT93
PWM		
PWM1	O	Pulse width modulation output This pin shared with PORTC1
PWM2	O	Pulse width modulation output This pin shared with PORTC2
IO		
P60 ~ P61	I/O	PORT60,1 can be INPUT or OUTPUT port each bit.. These two pins can be used on ERIC and IRC modes.
P62 ~P65	I/O	PORT6 can be INPUT or OUTPUT port each bit.
P70	I/O	PORT70 can be INPUT or OUTPUT port each bit.
P71	I	PORT71 is INPUT only.
P73~P76	I/O	PORT7 can be INPUT or OUTPUT port each bit.
P90 ~ P97	I/O	PORT9 can be INPUT or OUTPUT port each bit.
PC1 ~ PC2	I/O	PORTC can be INPUT or OUTPUT port each bit.
INT0	(PORT70)	Interrupt sources. Once PORT70 has a falling edge or rising edge signal (controlled by CONT register), it will generate a interruption.
INT1	(PORT71)	Interrupt sources which has the same interrupt flag. Any pin from PORT71 has a falling edge signal, it will generate a interruption.
INT3	PORT73	Interrupt sources which has the same interrupt flag. Any pin from PORT73 has a falling edge signal, it will generate a interruption.
/RESET	I	Low reset

VII. Functional Descriptions

VII.1 Operational Registers

Register configuration

	R PAGE registers			
Addr	R PAGE0	R PAGE1	R PAGE2	R PAGE3
00	Indirect addressing			
01	TCC			
02	PC			
03	Page, Status			
04	RAM bank, RSR			
05	Program ROM page			PWM control
06	Port6 I/O data			Duty of PWM1
07	Port7 I/O data	ADC MSB output data		PWM1 control Duty of PWM1
08				Period of PWM1
09	Port9 I/O data			Duty of PWM2
0A	PLL, Main clock, WDTE			PWM2 control Duty of PWM2
0B		ADC output data buffer		Period of PWM2
0C	PortC I/O data	Counter1 data		
0D				
0E	Interrupt flag			
0F	Interrupt flag			
10 : 1F	16 bytes Common registers			
20	Bank0	Bank1	Bank2	Bank3
:	Common registers			
3F	(32x8 for each bank)			

*Address 00~0F with page0~page3 are special registers. Address 10~1F are global with general purpose memory. By setting MOV instruction, MCU can read or write these register directly and RAM bank select bits (RB1, RB0 in R4 page0) will be ignored. Address 20~ 3F are general purpose RAM too, but user must indicate the bank number before access data.

	IOC PAGE registers	
Addr	IOC PAGE0	IOC PAGE1
00		
01		
02		
03		
04		
05		
06	Port6 I/O control	Port6 switches
07	Port7 I/O control	Port7 pull high
08		
09	Port9 I/O control	
0A		
0B		ADC control
0C		
0D		Clock source (CN1) Prescaler(CN1)
0E	Interrupt mask	
0F	Interrupt mask	
10		
:		
1F		
20		
:		
3F		

* IOC register are special registers. User can use instruction "IOW" to write data or "IOR" to read data.

VII.2 Operational Register Detail Description

R0 (Indirect Addressing Register)

R0 is not a physically implemented register. It is used as indirect addressing pointer. Any instruction using R0 as register actually accesses data pointed by the RAM Select Register (R4).

Example:

```
Mov    A, @0x20        ;store a address at R4 for indirect addressing
Mov    0x04, A
Mov    A, @0xAA        ;write data 0xAA to R20 at bank0 through R0
Mov    0x00, A
```

R1 (TCC)

TCC data buffer. Increased by 16.384KHz or by the instruction cycle clock (controlled by CONT register). Written and read by the program as any other register.

R2 (Program Counter)

The structure is depicted in Fig.3.

Generates 4k × 13 external ROM addresses to the relative programming instruction codes.

"JMP" instruction allows the direct loading of the low 10 program counter bits.

"CALL" instruction loads the low 10 bits of the PC, PC+1, and then push into the stack.

"RET" ("RETL k", "RETI") instruction loads the program counter with the contents at the top of stack.

"MOV R2, A" allows the loading of an address from the A register to the PC, and the ninth and tenth bits are cleared to "0".

"ADD R2,A" allows a relative address be added to the current PC, and contents of the ninth and tenth bits are cleared to "0".

"TBL" allows a relative address added to the current PC, and contents of the ninth and tenth bits don't change.

The most significant bit (A10~A11) will be loaded with the contents of bit PS0~PS1 in the status register (R5 PAGE0) upon the execution of a "JMP", "CALL", "ADD R2, A", or "MOV R2, A" instruction.

If an interrupt is triggered, PROGRAM ROM will jump to address 0x08 at page0. The CPU will store ACC, R3 status and R5 PAGE automatically, and they will be restored after instruction RETI.

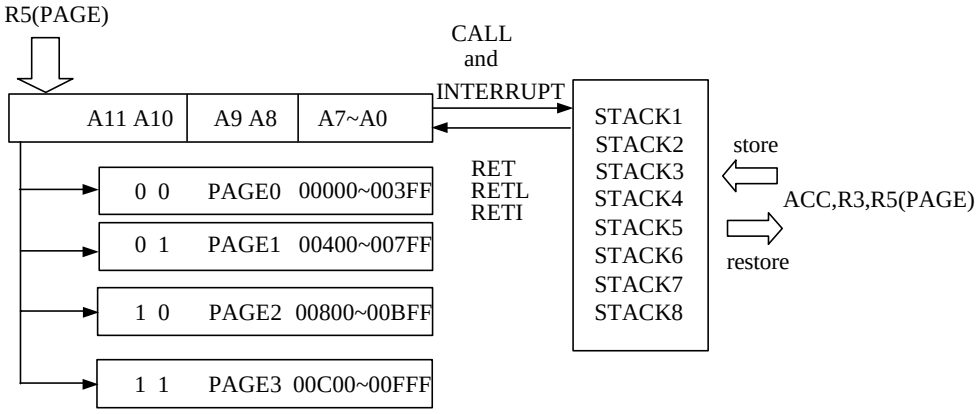


Fig.3 Program counter organization

R3 (Status, Page selection)

(Status flag, Page selection bits)

7	6	5	4	3	2	1	0
RPAGE1	RPAGE0	IOCPAGE	T	P	Z	DC	C
R/W-0	R/W-0	R/W-0	R	R	R/W	R/W	R/W

Bit 0(C) : Carry flag

Bit 1(DC) : Auxiliary carry flag

Bit 2(Z) : Zero flag

Bit 3(P) : Power down bit

Set to 1 during power on or by a "WDTC" command and reset to 0 by a "SLEP" command.

Bit 4(T) : Time-out bit

Set to 1 by the "SLEP" and "WDTC" command, or during power up and reset to 0 by WDT timeout.

EVENT	T	P	REMARK
WDT wake up from sleep mode	0	0	
WDT time out (not sleep mode)	0	1	
/RESET wake up from sleep	1	0	
Power up	1	1	
Low pulse on /RESET	x	X	x : don't care

Bit 5(IOCPAGE) : change IOC5 ~ IOCE to another page

Please refer to Fig.4 control register configuration for details.

0/1 ➔ IOC page0 / IOC page1

Bit 6(RPAGE0 ~ RPAGE1) : change R5 ~ RE to another page

Please refer to VII.1 Operational registers for detail register configuration.

(RPAGE1,RPAGE0)	R page # selected
(0,0)	R page 0
(0,1)	R page 1
(1,0)	R page 2
(1,1)	R page 3

R4 (RAM selection for common registers R20 ~ R3F)

(RAM selection register)

7	6	5	4	3	2	1	0
RB1	RB0	RSR5	RSR4	RSR3	RSR2	RSR1	RSR0
R/W-0	R/W-0	R/W	R/W	R/W	R/W	R/W	R/W

Bit 0 ~ Bit 5 (RSR0 ~ RSR5) : Indirect addressing for common registers R20 ~ R3F

RSR bits are used to select up to 32 registers (R20 to R3F) in the indirect addressing mode.

Bit 6 ~ Bit 7 (RB0 ~ RB1) : Bank selection bits for common registers R20 ~ R3F

These selection bits are used to determine which bank is activated among the 4 banks for 32 register (R20 to R3F)..

Please refer to VII.1 Operational registers for details.

R5 (Program page selection, PWM control)

PAGE0 (PORT5 I/O data register, Program page register)

7	6	5	4	3	2	1	0
X	X	X	X	0	0	PS1	PS0
-	-	-	-	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 1 (PS0 ~ PS1) : Program page selection bits

PS1	PS0	Program memory page (Address)
0	0	Page 0
0	1	Page 1
1	0	Page 2
1	1	Page 3

User can use PAGE instruction to change page to maintain program page by user.

Bit2~Bit3 : (undefined) These 2 bits must clear to 0 or MCU will access wronging program code.

Bit4~Bit7: (undefined) not allowed to use

PAGE1, PAGE2 (Unused registers)

These two registers are not allowed to used.

PAGE3 (PWMCON)

7	6	5	4	3	2	1	0
PWM2E	PWM1E	T2EN	T1EN	T2P1	T2P0	T1P1	T1P0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 1 (T1P0 ~ T1P1): TMR1 clock prescale option bits.

T1P1	T1P0	Prescale
0	0	1:2(Default)
0	1	1:8
1	0	1:32
1	1	1:64

Bit 2 ~ Bit 3 (T2P0 ~ T2P1): TMR2 clock prescale option bits.

T2P1	T2P0	Prescale
0	0	1:2(Default)
0	1	1:8

1	0	1:32
1	1	1:64

Bit 4 (T1EN): TMR1 enable bit
0 ➔ TMR1 is off (default value).
1 ➔ TMR1 is on.
Bit 5 (T2EN): TMR2 enable bit
0 ➔ TMR2 is off (default value).
1 ➔ TMR2 is on.
Bit 6 (PWM1E): PWM1 enable bit
0 ➔ PWM1 is off (default value), and its related pin carries out the PC1 function;
1 ➔ PWM1 is on, and its related pin will be set to output automatically.
Bit 7 (PWM2E): PWM2 enable bit
0 ➔ PWM2 is off (default value), and its related pin carries out the PC2 function.
1 ➔ PWM2 is on, and its related pin will be set to output automatically.

R6 (PORT6 I/O data, PWM control)

PAGE0 (PORT6 I/O data register)

7	6	5	4	3	2	1	0
X	X	P65	P64	P63	P62	P61	P60
-	-	R/W	R/W	R/W	R/W	R/W	R/W

Bit0 ~ Bit1 (P60 ~ P61): PORT60 and PORT61 can be used on IRC and ERIC mode. In these two mode, PORT60 and PORT61 will defined to general purpose IO. In crystal mode, PORT60 and PORT61 are defined to crystal input (XIN and XOUT) pins and these two bits are undefined.

Bit2 ~ Bit6 (P62 ~ P65): 4-bit PORT6(2~5) I/O data register

User can use IOC register to define input or output each bit.

Bit6 ~ Bit7 : Unused register. These bits are not allowed to use.

PAGE1, PAGE2 : (undefined) not allowed to use

These two registers are not allowed to use.

PAGE3 (DT1L: the Least Significant Byte (Bit 7 ~ Bit 0) of Duty Cycle of PWM1)

7	6	5	4	3	2	1	0
PWM1[7]	PWM1[6]	PWM1[5]	PWM1[4]	PWM1[3]	PWM1[2]	PWM1[1]	PWM1[0]
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

A specified value keeps the output of PWM1 to stay at high until the value matches with TMR1.

R7 (PORT7 I/O data, ADC, Duty cycle of PWM)

PAGE0 (PORT7 I/O data register)

7	6	5	4	3	2	1	0
X	P76	P75	P74	P73	X	P71	P70
-	R/W	R/W	R/W	R/W	-	R	R/W

Bit0 (P70): PORT70 is a multi-function pin. In Crystal mode, by setting P70S in code option, PORT70 will be general purpose IO or PLLC. Please do not enable PLL function if PORT70 defined to IO. In IRC or ERIC mode, this pin will defined to PORT70 and P70S will be ignored. P70 is PORT70 I/O data register and user can use IOC register to define input or output each bit.

Bit1 (P71): PORT71 is shared with /RESET pin. By setting P71S in code option, PORT71 will defined to INPUT pin or /RESET pin. This register is a read only bit. P71 dose not support internal pull high function. If user want to use P71 interrupt, external pull high is necessary.

Bit3 ~ Bit6 (P73 ~ P76): 4 - bit PORT7 I/O data register

User can use IOC register to define input or output each bit.

PAGE1 (ADC resolution selection bit and ADC MSB output data)

7	6	5	4	3	2	1	0
X	X	AD9	AD8	X	ADRES	0	0
-	-	R	R	-	R/W-0	R-0	R-0

Bit 0~Bit 1: *Undefined register. These two bits are not allowed to use. These bits must clear to 0.*

Bit 2(ADRES) : Resolution selection for ADC

0 ➔ ADC is 8-bit resolution

When 8-bit resolution is selected, the most significant(MSB) 8-bit data output of the internal 10-bit ADC will be mapping to RB PAGE1 so R7 PAGE1 bit 4 ~5 will be of no use.

1 ➔ ADC is 10-bit resolution

When 10-bit resolution is selected, 10-bit data output of the internal 10-bit ADC will be exactly mapping to RB PAGE1 and R7 PAGE1 bit 4 ~5.

Bit 3 : *(undefined) not allowed to use*

Bit 4 ~ Bit 5(AD8 ~ AD9) : The most significant 2 bit of 10-bit ADC conversion output data

Combine there two bits and RB PAGE1 as complete 10-bit ADC conversion output data.

Bit 6 ~ Bit 7 : *(undefined) not allowed to use*

PAGE2 : (undefined) not allowed to use

PAGE3 (DT1H: the Most Significant Byte (Bit 1 ~ Bit 0) of Duty Cycle of PWM)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	PWM1[9]	PWM1[8]
R-0	R-0	R-0	R-0	R-0	R-0	R/W-0	R/W-0

Bit 0 ~ Bit 1 (PWM1[8] ~ PWM1[9]): The Most Significant two bits of PWM1 Duty Cycle

Bit 2 ~ Bit 7 : Unused.

R8 (Data RAM address, PWM1 period)

PAGE0: *(undefined) not allowed to use*

PAGE1: *(undefined) not allowed to use*

PAGE2: *(undefined) not allowed to use*

PAGE3 (PRD1: Period of PWM)

7	6	5	4	3	2	1	0
PRD1[7]	PRD1[6]	PRD1[5]	PRD1[4]	PRD1[3]	PRD1[2]	PRD1[1]	PRD1[0]
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

The content of this register is a period (time base) of PWM1. The frequency of PWM1 is the reverse of the period.

R9 (PORT9 I/O data)

PAGE0 (PORT9 I/O data register)

7	6	5	4	3	2	1	0
P97	P96	P95	P94	P93	P92	P91	P90
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 0 ~ Bit 7 (P90 ~ P97) : 8-bit PORT9(0~7) I/O data register

User can use IOC register to define input or output each bit.

PAGE1: *(undefined) not allowed to use*

PAGE2: *(undefined) not allowed to us*

PAGE3 (DT2L: the Least Significant Byte (Bit 7 ~ Bit 0) of Duty Cycle of PWM2)

7	6	5	4	3	2	1	0
PWM2[7]	PWM2[6]	PWM2[5]	PWM2[4]	PWM2[3]	PWM2[2]	PWM2[1]	PWM2[0]
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

A specified value keeps the output of PWM2 to stay at high until the value matches with TMR2.

RA (PLL, Main clock selection, Watchdog timer)

PAGE0 (PLL enable bit, Main clock selection bits, Watchdog timer enable bit)

7	6	5	4	3	2	1	0
0	PLLEN	CLK2	CLK1	CLK0	X	X	WDTEN
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	-	-	R/W-0

Bit 0(WDTEN) : Watch dog control bit.

0/1 ➔ disable/enable

User can use WDTC instruction to clear watch dog counter. The watchdog timer is a free running on-chip RC oscillator. The WDT will keep on running even after the oscillator driver has been turned off (i.e. in sleep mode). During normal operation or sleep mode, a WDT time-out (if enabled) will cause the device to reset. The WDT can be enabled or disabled at any time during the green mode or normal mode by software programming. Without presacler, the WDT time-out period is approximately 18 ms.

Bit 1~Bit 2 : Unused

Bit 3 ~ Bit 5 (CLK0 ~ CLK2) : MAIN clock selection bits on Crystal mode. These three bits are unused on IRC and ERIC mode.

In Crystal mode:

User can choose different frequency of main clock by CLK1 and CLK2. All the clock selection is list below.

PLLEN	CLK2	CLK1	CLK0	Sub clock	MAIN clock	CPU clock
1	0	0	0	32.768kHz	3.582MHz	3.582MHz (Normal mode)
1	0	0	1	32.768kHz	3.582MHz	3.582MHz (Normal mode)
1	0	1	0	32.768kHz	3.582MHz	3.582MHz (Normal mode)
1	0	1	1	32.768kHz	3.582MHz	3.582MHz (Normal mode)
1	1	0	0	32.768kHz	14.3MHz	14.3MHz (Normal mode)
1	1	0	1	32.768kHz	14.3MHz	14.3MHz (Normal mode)
1	1	1	0	32.768kHz	14.3MHz	14.3MHz (Normal mode)
1	1	1	1	32.768kHz	14.3MHz	14.3MHz (Normal mode)
0	don't care	don't care	don't care	32.768kHz	don't care	32.768kHz (Green mode)

Bit 6(PLLEN) : PLL's power control bit which is CPU mode control register. This bit is only used in crystal mode. In RC mode, this bit will be ignored.

0/1 ➔ disable PLL/enable PLL

If enable PLL, CPU will operate at normal mode (high frequency). Otherwise, it will run at green mode (low frequency, 32768 Hz).

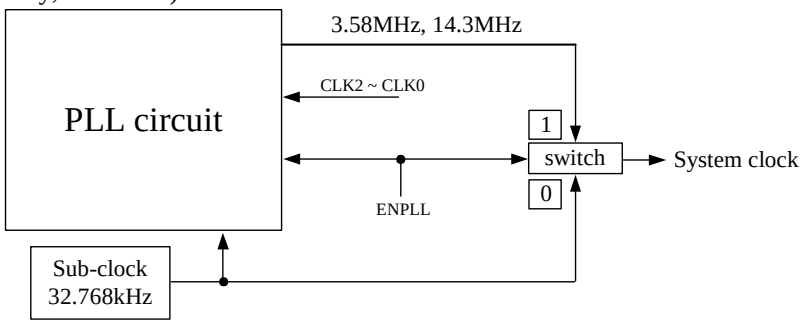


Fig.4 The relation between 32.768kHz and PLL

Bit 7: Unused register. Always keep this bit to 0 or some un-expect error will happen!

Next table show the status after wake-up and the wake-up sources list

Wakeup signal	SLEEP mode
	RA(7,6)=(0,0) + SLEP
TCC time out IOCF bit0=1	No function
COUNTER1 time out IOCF bit1=1	No function
WDT time out	Reset and jump to address 0
PORT7 (0,1,3)	Reset and Jump to address 0

PORT70 's wakeup function is controlled by IOCF bit 3. It's falling edge or rising edge trigger (controlled by CONT register bit7).

PORT71 's wakeup function is controlled by IOCF bit 4. It's falling edge trigger.

PORT73 's wakeup function is controlled by IOCF bit 5. It is falling edge trigger.

PAGE1,2 : *(undefined) not allowed to use*

PAGE3 (DT2H: the Most Significant Byte (Bit 1 ~ Bit 0) of Duty Cycle of PWM2)

7	6	5	4	3	2	1	0
X	X	X	X	X	X	PWM2[9]	PWM2[8]
-	-	-	-	-	-	R/W-0	R/W-0

Bit 0 ~ Bit 1 (PWM2[8] ~ PWM2[9]): The Most Significant Byte of PWM1 Duty Cycle
A specified value keeps the PWM1 output to stay at high until the value matches with TMR1.
Bit 2 ~ Bit 7 : (undefined) not allowed to use

RB (ADC input data buffer)

PAGE0 : *(undefined) not allowed to use*

PAGE1 (ADC output data register)

7	6	5	4	3	2	1	0
AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
R	R	R	R	R	R	R	R

Bit 0 ~ Bit 7 (AD0 ~ AD7) : The last significant 8 bit of 10-bit or whole of 8 bit resolution ADC conversion output data. Combine there 8 bits and R7 PAGE1 bit4~5 as complete 10-bit ADC conversion output data in 10 bit resolution mode.

PAGE 2 *(undefined) not allowed to use*

PAGE3 (PRD2: Period of PWM2)

7	6	5	4	3	2	1	0
PRD2[7]	PRD2[6]	PRD2[5]	PRD2[4]	PRD2[3]	PRD2[2]	PRD2[1]	PRD2[0]
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

The content of this register is a period (time base) of PWM2. The frequency of PWM2 is the reverse of the period.

RC (PORTC I/O data, Counter1 data)

PAGE0 (PORT9 I/O data register)

7	6	5	4	3	2	1	0
X	X	X	X	X	PC2	PC1	X
-	-	-	-	-	R/W	R/W	-

Bit 1 ~ Bit 2 (PC1 ~ PC2) : PORTC1,PORTC2 I/O data register

User can use IOC register to define input or output each bit.

Bit 0; Bit 3~Bit 7: (undefined) not allowed to use.(These bits are not sure to 0 or 1)

PAGE1 (Counter1 data register)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CN17	CN16	CN15	CN14	CN13	CN12	CN11	CN10
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 7 (CN10 ~ CN17) : Counter1's buffer that user can read and write.

Counter1 is a 8-bit up-counter with 8-bit prescaler that user can use RC PAGE1 to preset and read the counter.(write ➔ preset) After a interruption , it will reload the preset value.

Example for writing :

```
MOV    0x0C, A    ; write the data at accumulator to counter1 (preset)
```

Example for reading :

```
MOV    A, 0x0C    ; read the data at counter1 to accumulator
```

PAGE2,3 *(undefined) not allowed to use.*

RD (Undefined register)

PAGE0 (Unused)

7	6	5	4	3	2	1	0
X	***0***	***0***	0	X	***0***	***0***	***0***
-	R/W-0	R/W-0	R/W-0	-	R/W	R/W	R/W

Bit 0 ~Bit 2 : These three bits must clear to 0 or MCU power consumption will increase.

Bit 3 , Bit 7 : *(undefined) not allowed to use*

Bit4 ~ Bit6 : These 3 bits are unused in mask/OTP EM785840, but they are used for ICE5830. About the definition of these 3 bits, please refer to appendix II. In ICE5830, please clear bit4, bit5 and bit6 to 0.

PAGE1,2,3 *(undefined) not allowed to use.*

RE (Interrupt flag)

PAGE0 (Interrupt flag)

7	6	5	4	3	2	1	0
PWM2	0	ADI	PWM1	0	0	0	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit0 ~ Bit3, Bit6: These four bits must clear to 0 or unable to expect error will occur .

Bit 4(PWM1) : PWM1 one period reach interrupt flag.

Bit 5 (ADI) : ADC interrupt flag after a sampling

Bit 7 (PWM2) : PWM2 (Pulse Width Modulation channel 2) interrupt flag

Set when a selected period is reached, reset by software.

PAGE2,3 *(undefined) not allowed to use.*

RF (Interrupt status)

(Interrupt status register)

7	6	5	4	3	2	1	0
INT3	0	0	INT1	INT0	0	CNT1	TCIF
R/W-0	R/W-X	R/W-X	R/W-0	R/W-0	R/W-X	R/W-0	R/W-0

"1" means interrupt request, "0" means non-interrupt

Bit 0(TCIF) : TCC timer overflow interrupt flag

Set when TCC timer overflows.

Bit 1(CNT1) : counter1 timer overflow interrupt flag

Set when counter1 timer overflows.

Bit 2,5,6: Unused (These bits are not sure to 0 or 1. When programmer determine what interrupt occur in subroutine, be care to note these bits)

Bit 3(INT0): By setting PORT70 to general IO, INT0 will define to PORT70 pin's interrupt flag. If PORT70 has a falling edge/rising edge (controlled by CONT register) trigger signal, CPU will set this bit. If setting the pin to PLLC or OSCI, PORT70 interrupt will un-exist and INT0 register will be ignored.

Bit 4(INT1): By setting PORT71 to general IO, INT1 will define to PORT71 pin's interrupt flag. External pull high circuit is needed for PORT71 interrupt operation. If PORT71 has a falling edge trigger signal, CPU will set this bit. If setting the pin to /RESET, PORT71 interrupt will un-exist and INT1 register will be ignored.

Bit 7(INT3): External PORT73 pin interrupt flag. If PORT73 has a falling edge trigger signal, CPU will set this bit.

<Note> IOCF is the interrupt mask register. User can read and clear.

Trigger edge as the table

Signal	Trigger
TCC	Time out
COUNTER1	Time out
INT0	Falling Rising edge
INT1	Falling edge
INT3	Falling edge

R10~R3F (General Purpose Register)

R10~R3F (Banks 0 ~ 3) : all are general purpose registers.

VII.3 Special Purpose Registers

A (Accumulator)

Internal data transfer, or instruction operand holding

It's not an addressable register.

CONT (Control Register)

7	6	5	4	3	2	1	0
P70EG	INT	TS	RETBK	PAB	PSR2	PSR1	PSR0
R/W-1	R/W-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

Bit 0 ~ Bit 2 (PSR0 ~ PSR2) : TCC/WDT prescaler bits

PSR2	PSR1	PSR0	TCC rate	WDT rate
0	0	0	1:2	1:1
0	0	1	1:4	1:2
0	1	0	1:8	1:4
0	1	1	1:16	1:8
1	0	0	1:32	1:16
1	0	1	1:64	1:32
1	1	0	1:128	1:64
1	1	1	1:256	1:128

Bit 3(PAB) : Prescaler assignment bit

0/1 ➔ TCC/WDT

Bit 4(RETBK) : Return value backup control for interrupt routine

0/1 ➔ disable/enable

When this bit is set to 1, the CPU will store ACC,R3 status and R5 PAGE automatically after an interrupt is triggered. And it will be restored after instruction RETI. When this bit is set to 0, the user need to store ACC, R3 and R5 PAGE in user program.

Bit 5(TS) : TCC signal source

0 ➔ Internal instruction cycle clock

1 ➔ IRC output

Bit 6 (INT) : INT enable flag

0 ➔ interrupt masked by DISI or hardware interrupt

1 ➔ interrupt enabled by ENI/RETI instructions

Bit 7 (P70EG): If switch port70 to INT0 input, P70EG can select the interrupt toggle type.

0 ➔ P70 's interruption source is a rising edge signal and falling edge signal.

1 ➔ P70 's interruption source is a falling edge signal.

CONT register is readable (CONTR) and writable (CONTW).

TCC and WDT :

There is an 8-bit counter available as prescaler for the TCC or WDT. The prescaler is available for the TCC only or WDT only at the same time.

An 8 bit counter is available for TCC or WDT determined by the status of the bit 3 (PAB) of the CONT register.

See the prescaler ratio in CONT register.

Fig.5 depicts the circuit diagram of TCC/WDT.

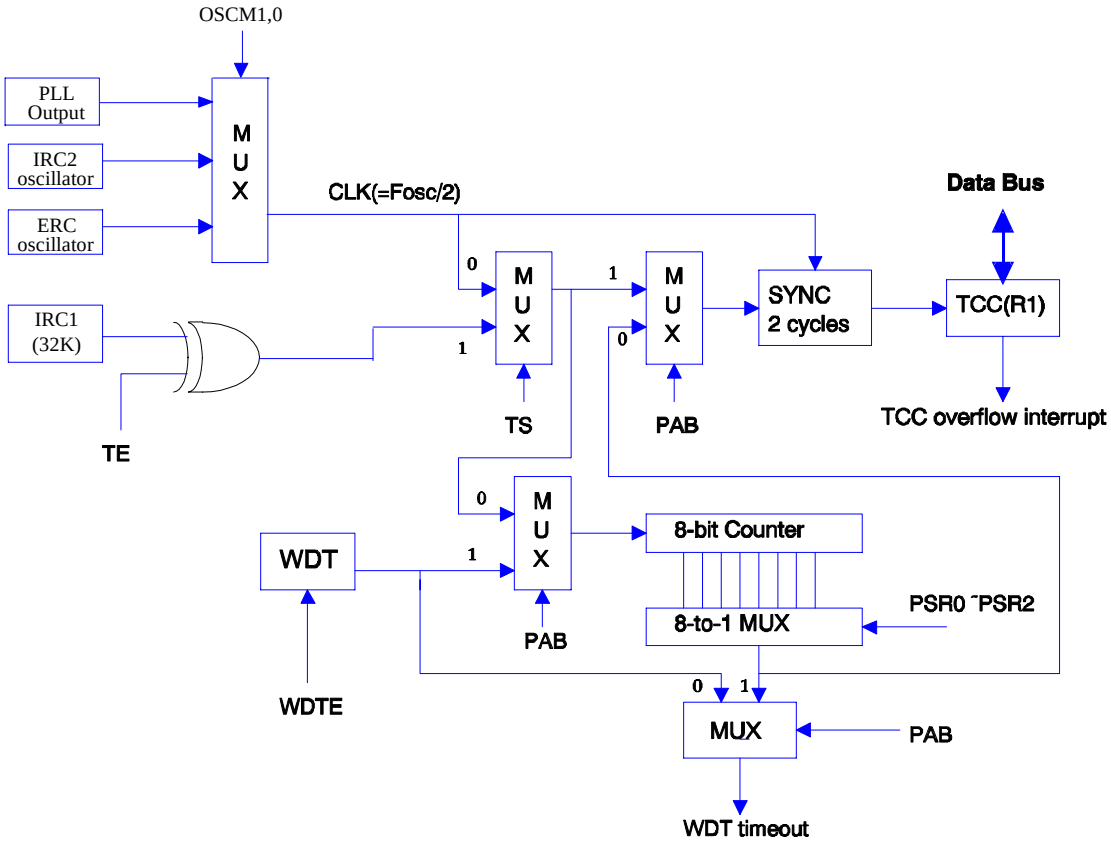


Fig.5 Block diagram of TCC WDT

IOC5 (Unused)

PAGE0 (Unused)

7	6	5	4	3	2	1	0
0	***0***	***0***	-	-	-	-	-
R/W	R/W	R/W					

Bit0~4 : *(undefined) not allowed to use*

Bit5~Bit7(Unused) : These three bits must clear to 0 or MCU power consumption will increase.
The default value in these 3 bits are "1". Please clear them to "0" when init MCU.

PAGE1 *(undefined) not allowed to use.****(This page is not sure to 0 or 1)***

IOC6 (PORT6 I/O control, P6* pins switch control)

PAGE0 (PORT6 I/O control register)

7	6	5	4	3	2	1	0
0	0	IOC65	IOC64	IOC63	IOC62	IOC61	IOC60
-	-	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

Bit0~Bit1: In crystal mode, these two bits are unused registers. In IRC or ERIC mode, PORT60 and PORT61 are I/O direction control register.

Bit 2 ~ Bit 5 (IOC62 ~ IOC65) : PORT6(2~5) I/O direction control register

0 ➔ put the relative I/O pin as output

1 ➔ put the relative I/O pin into high impedance

Bit6~Bit7 (Unused): These2 bits must clear to 0 or MCU power consumption will increase.
The default value in these 2 bits are "1". Please clear them to "0" when init MCU.

PAGE1 (P6* pins switch control register)

7	6	5	4	3	2	1	0
X	0	P65S	P64S	P63S	P62S	P91S	P90S
-	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

ADC channel 1 and channel 2 are shared with PORT90 and PORT91.

Bit 0(P90S) : Select normal I/O PORT90 pin or channel 1 input AD1 pin of ADC
0 ➔ P90 (I/O PORT90) pin is selected
1 ➔ AD1 (Channel 1 input of ADC) pin is selected

Bit 1(P91S) : Select normal I/O PORT91 pin or channel 2 input AD2 pin of ADC
0 ➔ P91 (I/O PORT91) pin is selected
1 ➔ AD2 (Channel 2 input of ADC) pin is selected

Bit 2(P62S) : Select normal I/O PORT62 pin or channel 3 input AD3 pin of ADC
0 ➔ P62 (I/O PORT62) pin is selected
1 ➔ AD3 (Channel 3 input of ADC) pin is selected

Bit 3(P63S) : Select normal I/O PORT63 pin or channel 4 input AD4 pin of ADC
0 ➔ P63 (I/O PORT63) pin is selected
1 ➔ AD4 (Channel 4 input of ADC) pin is selected

Bit 4(P64S) : Select normal I/O PORT64 pin or channel 5 input AD5 pin of ADC
0 ➔ P64 (I/O PORT64) pin is selected
1 ➔ AD5 (Channel 5 input of ADC) pin is selected

Bit 5(P65S) : Select normal I/O PORT65 pin or channel 6 input AD6 pin of ADC
0 ➔ P65 (I/O PORT65) pin is selected
1 ➔ AD5 (Channel 6 input of ADC) pin is selected

Bit 6: Unused register. Please clear this bit to 0 or ADC result will wronging.

Bit 7: Unused register. This bit is nor allowed to use.

IOC7 (PORT7 I/O control, PORT7 pull high control)

PAGE0 (PORT7 I/O control register)

7	6	5	4	3	2	1	0
X	IOC76	IOC75	IOC74	IOC73	X	X	IOC70
-	R/W-1	R/W-1	R/W-1	R/W-1	-	-	R/W-1

Bit0(IOC70): PORT70 pin will defined to general purpose IO, PLLC or OSC by setting code option. In IRC mode or crystal mode(only at code option P70S =0), PORT70 pin will be a general purpose IO. IOC70 is PORT70 pin's I/O direction control register.

0 ➔ put the relative I/O pin as output
1 ➔ put the relative I/O pin into high impedance

Bit1 (Unused) : This bit is unused registers. By setting P71S = 1 in code option, PORT71 pin will be a INPUT only pin.

Bit2; Bit7 (Unused) : These 2 bits must clear to 0 or MCU power consumption will increase. The default value in these 3 bits are "1". Please clear them to "0" when init MCU.

Bit3~Bit6 (IOC73~IOC76) : PORT7 I/O direction control register
0 ➔ put the relative I/O pin as output
1 ➔ put the relative I/O pin into high impedance

PAGE1 (PORT7 pull high control register)

7	6	5	4	3	2	1	0
X	PH76	PH75	PH74	PH73	X	X	PH70
-	R/W-0	R/W-0	R/W-0	R/W-0	-	-	R/W-0

Bit0: PORT70 pull high control register. This bit only exist on setting PORT70 general purpose IO.
0 ➔ disable pull high function.
1 ➔ enable pull high function

Bit1, Bit7 (Unused): These2 bits must clear to 0 or MCU power consumption will increase.

Bit3~Bit6 : PORT7 pull high control register

0 ➔ disable pull high function.
1 ➔ enable pull high function

IOC8 (Unused), *not allowed to use*

IOC9 (PORT9 I/O control, PORT9 switches)

PAGE0 (PORT9 I/O control register)

7	6	5	4	3	2	1	0
IOC97	IOC96	IOC95	IOC94	IOC93	IOC92	IOC91	IOC90
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

Bit 0 ~ Bit 7 (IOC90 ~ IOC97) : PORT9(0~7) I/O direction control register
0 ➔ put the relative I/O pin as output
1 ➔ put the relative I/O pin into high impedance

PAGE1 (Unused)

7	6	5	4	3	2	1	0
0	***0***	***0***	***0***	***0***	***0***	***0***	***0***
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

*****These 8 bits must clear to 0 or Port9 input or output function will wronging***

IOCA (Unused)

PAGE0*(undefined) not allowed to use*

PAGE1 Unused

7	6	5	4	3	2	1	0
X	***0***	X	X	***0***	X	AD8S	AD7S
-	R/W	-	-	R/W	-	R/W-0	R/W-0

Bit 0(AD7S) : Select normal I/O PORT92 pin or channel 7 input AD7 pin of ADC
0 ➔ P92 (I/O PORT92) pin is selected
1 ➔ AD7 (Channel 7 input of ADC) pin is selected
Bit 1(AD8S) : Select normal I/O PORT93 pin or channel 8 input AD8 pin of ADC
0 ➔ P93 (I/O PORT93) pin is selected
1 ➔ AD8 (Channel 8 input of ADC) pin is selected

Bit3 , Bit6 (Unused) : These 2 bits must clear to 0 or MCU power consumption will increase.
Bit2 ~ Bit7 are undefined register, they are not allowed to use.

IOCB (ADC control)

PAGE0 (Unused)

7	6	5	4	3	2	1	0
0	***0***	***0***	***0***	***0***	***0***	***0***	***0***
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

***** This page must clear to 0 or MCU power consumption will increase.***

The default value in these 8 bits are "1". Please clear them to "0" when init MCU.

PAGE1 (ADC control bits)

7	6	5	4	3	2	1	0
IN2	IN1	IN0	ADCLK1	ADCLK0	ADPWR	0	ADST
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		R/W-0

Bit 0(ADST) : AD converter start to sample

By setting to "1", the AD will start to sample data. This bit will be cleared by hardware automatically after a sampling.

Bit 1 : *(undefined) not allowed to use. This bit must clear to 0.*

Bit 2(ADPWR) : AD converter power control, 1/0 ➔ enable/disable.

Bit 3 ~ Bit 4 (ADCLK0 ~ ADCLK1) : AD circuit 's sampling clock source.

For Crystal mode:

ADCLK1	ADCLK0	Sampling rate	Operation voltage
0	0	74.6K	>=3.5V
0	1	37.4K	>=3.0V
1	0	18.7K	>=2.5V
1	1	9.3K	>=2.5V

For IRC or ERIC mode, AD converter rate will change by oscillator. The formula for input frequency and AD converter rate is: ***AD converter rate = oscillator / 4 / (2^ADCLK)/12***

For example, if input CLK = 4M Hz:

ADCLK1	ADCLK0	Sampling rate	Operation voltage
0	0	83.3K	>=3.5V
0	1	41.7K	>=3.0V
1	0	20.8K	>=2.5V
1	1	10.4K	>=2.5V

* Please avoid AD converter rate over 50K Hz, it maybe decrease ADC's resolution.

This is a CMOS multi-channel 10-bit successive approximation A/D converter.

Features

74.6kHz maximum conversion speed (Crystal mode) at 5V.
Adjusted full scale input
Internal (VDD) reference voltage
8 analog inputs multiplexed into one A/D converter
Power down mode for power saving
A/D conversion complete interrupt
Interrupt register, A/D control and status register, and A/D data register

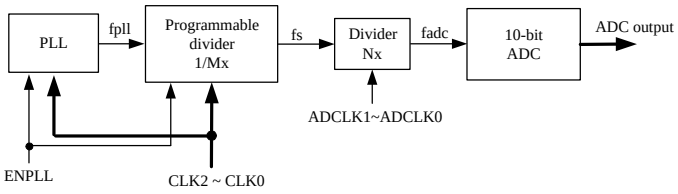


Fig.6 ADC voltage control logic

Bit 5 ~ Bit 7(IN0~ IN2) : Input channel selection of AD converter

These two bits can choose one of three AD input.

IN2	IN1	IN0	Input	Pin
0	0	0	AD1	P90
0	0	1	AD2	P91
0	1	0	AD3	P62
0	1	1	AD4	P63
1	0	0	AD5	P64
1	0	1	AD6	P65
1	1	0	AD7	P92
1	1	1	AD8	P93

*Before switch to the AD channel, please set the corresponding pin as AD input.

IOCC (PORTC I/O control, ADC control)

PAGE0 (PORTC I/O control)

7	6	5	4	3	2	1	0
0	***0***	***0***	***0***	***0***	IOCC2	IOCC1	***0***
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

Bit 1 ~ Bit 2 (IOCC1 ~ IOCC2) : PORTC(1~2) I/O direction control register

0 ➔ put the relative I/O pin as output

1 ➔ put the relative I/O pin into high impedance

***** Bit0 , Bit3 ~ Bit7 must clear to 0 or MCU power consumption will increase.***

The default value in these 6 un-define bits are "1". Please clear them to "0" when init MCU.

PAGE1 (PORT switch)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	***1***
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W/0

Bit 0: Always set this bit to "1" otherwise partial ADC function cannot be used)

Bit 1 ~ Bit 7: *(undefined) not allowed to use*

IOCD (TONE1 control, Clock source, Prescaler of CN1)

PAGE0 (Reserved)

PAGE1 (Clock source and prescaler for COUNTER1)

7	6	5	4	3	2	1	0
CNTI/ES	X	X	X	CNT1S	C1_PSC2	C1_PSC1	C1_PSC0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 2 (C1_PSC0 ~ C1_PSC2) : COUNTER1 prescaler ratio

C1_PSC2	C1_PSC1	C1_PSC0	COUNTER1
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

Bit 3(CNT1S) : COUNTER1 clock source. This bit will un-effect on RC mode (RC mode's CLK is always equal to oscillator frequency).

0/1 ➔ 16.384kHz / system clock.

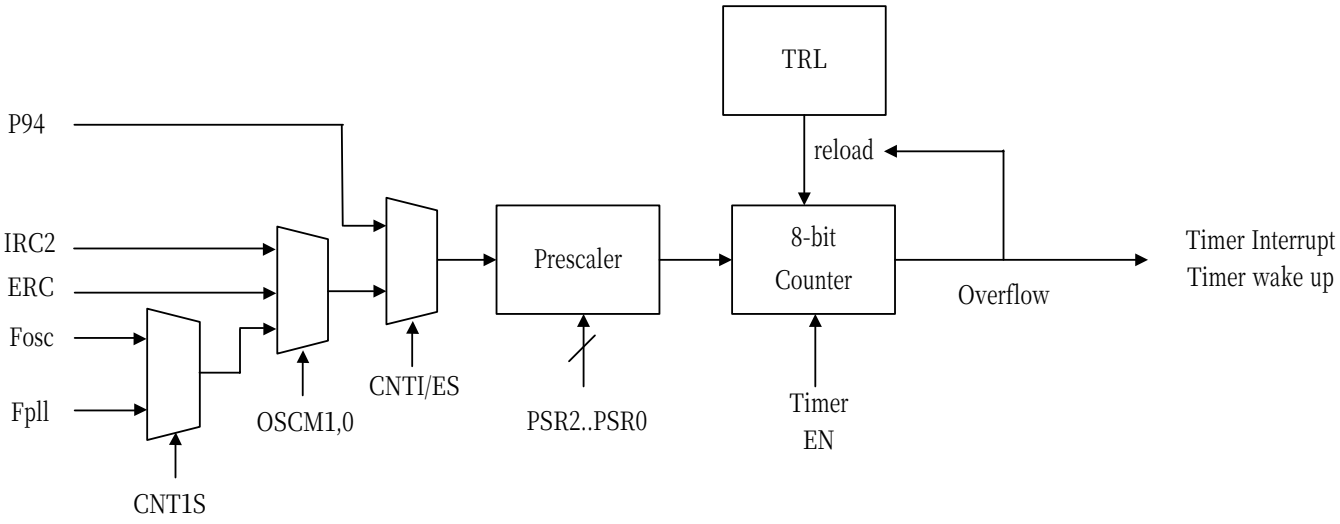


Fig 7: Timer CLK source diagram

Bit4 ~ Bit6: Unused register. These three bits are not allowed to use.

Bit7 (CNTI/ES):Counter source select.

CNTI/ES = 0 ➔ Timer counter CLK come from system CLK or Crystal output and P94 is defined to general propose IO.

CHTI/ES = 1 ➔ P94 is defined to input and Timer counter's CLK will come from P94's falling edge.

IOCE (Interrupt mask,)

PAGE0 (Interrupt mask)

7	6	5	4	3	2	1	0
PWM2	0	ADI	PWM1	X	X	X	X
R/W-0	R/W-0	R/W-0	R/W-0	-	-	-	-

Bit 0 ~ Bit 3 : unused

Bit 4(PWM1) : PWM1 one period reach interrupt mask.

Bit 5 (ADI) : ADC conversion complete interrupt mask

0/1 ➔ disable/enable interrupt

There are four registers for A/D converter. Use one bit of interrupt control register (IOCE PAGE0 Bit5) for

A/D conversion complete interrupt. The status and control register of A/D (IOCB PAGE1 and RE PAGE0 Bit5) responses the A/D conversion status or takes control on A/D. The A/D data register (RB PAGE1) stores A/D conversion result.

ADI bit in IOCE PAGE0 register is end of A/D conversion complete interrupt enable/disable. It enables/disables ADI flag in RE register when A/D conversion is complete. ADI flag indicates the end of an A/D conversion. The A/D converter sets the interrupt flag, ADI in RE PAGE0 register when a conversion is complete. The interrupt can be disabled by setting ADI bit in IOCE PAGE0 Bit5 to '0'.

The A/D converter has eight analog input channels AD1~AD8 multiplexed into one sample and hold to A/D module. Reference voltage can be driven from internal power. The A/D converter itself is of an 10-bit successive approximation type and produces lost significant 8-bit result in the RB PAGE1 and most significant 2 bit to R7 PAGE1 bit4, bit5. A conversion is initiated by setting a control bit ADST in IOCB PAGE1 Bit0. Prior to conversion, the appropriate channel must be selected by setting IN0~IN2 bits in RE register and allowed for enough time to sample data. Every conversion data of A/D need 12-clock cycle time. The minimum conversion time required is 13 us (73K sample rate). ADST Bit in IOCB PAGE1 Bit0 must be set to begin a conversion.

It will be automatically reset in hardware when conversion is complete. At the end of conversion, the START bit is cleared and the A/D interrupt is activated if ADI in IOCE PAGE0 Bit5 = 1. ADI will be set when conversion is complete. It can be reset in software.

If ADI = 0 in IOCE PAGE0 Bit5, when A/D start conversion by setting ADST(IOCB PAGE1 Bit0) = 1 then A/D will continue conversion without stop and hardware won't reset ADST bit. In this condition, ADI is deactived. After ADI in IOCE PAGE0 bit5 is set, ADI in RE PAGE0 bit5 will activate again.

To minimum operating current , all biasing circuits in the A/D module that consume DC current are power down when ADPWR bit in IOCB PAGE1 Bit2 register is a '0'. When ADPWR bit is a '1', A/D converter module is operating.

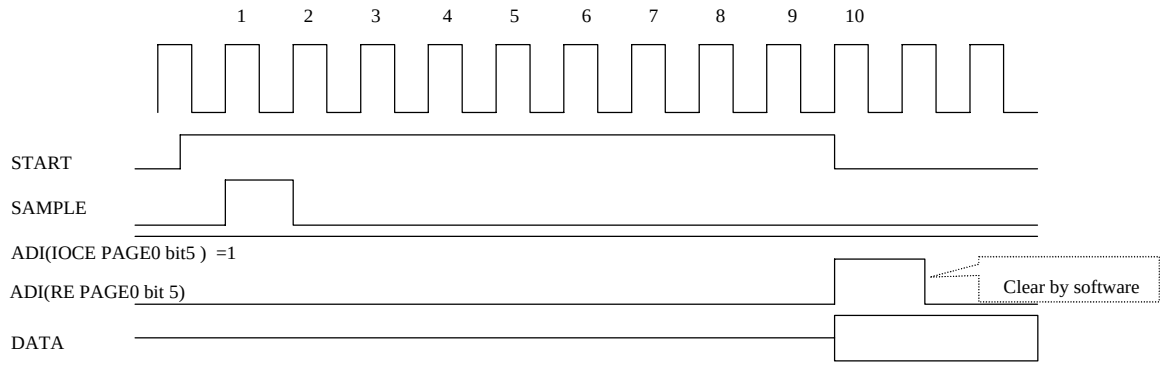


Fig.8 A/D converter timing

Bit 6: Undefined register. Please clear this bit to 0.

Bit 7 (PWM2) : PWM2 interrupt enable bit

0/1 ➔ disable/enable interrupt

IOCF (Interrupt mask)

(Interrupt mask register)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
INT3	X	X	INT1	INT0	X	CNT1	TCIF
R/W-0	-	-	R/W-0	R/W-0	-	R/W-0	R/W-0

Bit 0~1; 3~4 ; Bit 7 : interrupt enable bit

0 ➔ disable interrupt

1 ➔ enable interrupt

Bit 2, 5~6 : (remain these values to "0"othwise it will generate unpredicted interrupts)

The status after interrupt and the interrupt sources list as the table below.

Interrupt signal		SLEEP mode	GREEN mode	NORMAL mode
TCC time out IOCF bit0=1 And "ENI"	ENI	RESET and Jump to address 0	Interrupt (jump to address 8 at page0)	Interrupt (jump to address 8 at page0)
	DISI	No function	No function	No function
COUNTER1 time out IOCF bit1=1 And "ENI"		No function	Interrupt (jump to address 8 at page0)	Interrupt (jump to address 8 at page0)
PORT70 Only at IRC mode or crystal mode (at P70S = 0)		RESET and Jump to address 0	Interrupt (jump to address 8 at page0)	Interrupt (jump to address 8 at page0)
PORT71 Only at P71S = 0		RESET and Jump to address 0	Interrupt (jump to address 8 at page0)	Interrupt (jump to address 8 at page0)
PORT73 IOCF bit3 bit7 =1 And "ENI"		RESET and Jump to address 0	Interrupt (jump to address 8 at page0)	Interrupt (jump to address 8 at page0)
ADI IOCE bit5 = 1 And "ENI		No function	No function	Interrupt (jump to address 8 at page0)
PWM1 IOCE bit4 = 1 And "ENI		No function	Interrupt (jump to address 8 at page0)	Interrupt (jump to address 8 at page0)

PORT70 's interrupt function is controlled by IOCF bit 3. It's falling edge or rising edge trigger (controlled by CONT register bit7).

PORT71 's interrupt function is controlled by IOCF bit 4. It's falling edge trigger.

PORT73 's interrupt function is controlled by IOCF bit 7. They are falling edge trigger.

ADI interrupt source function is controlled by RE PAGE0 bit 5. It is rising edge trigger after ADC sample complete.

VII.4 I/O Port

The I/O registers are bi-directional tri-state I/O ports. The I/O ports can be defined as "input" or "output" pins by the I/O control registers under program control. The I/O data registers and I/O control registers are both readable and writable. The I/O interface circuit is shown in Fig.9.

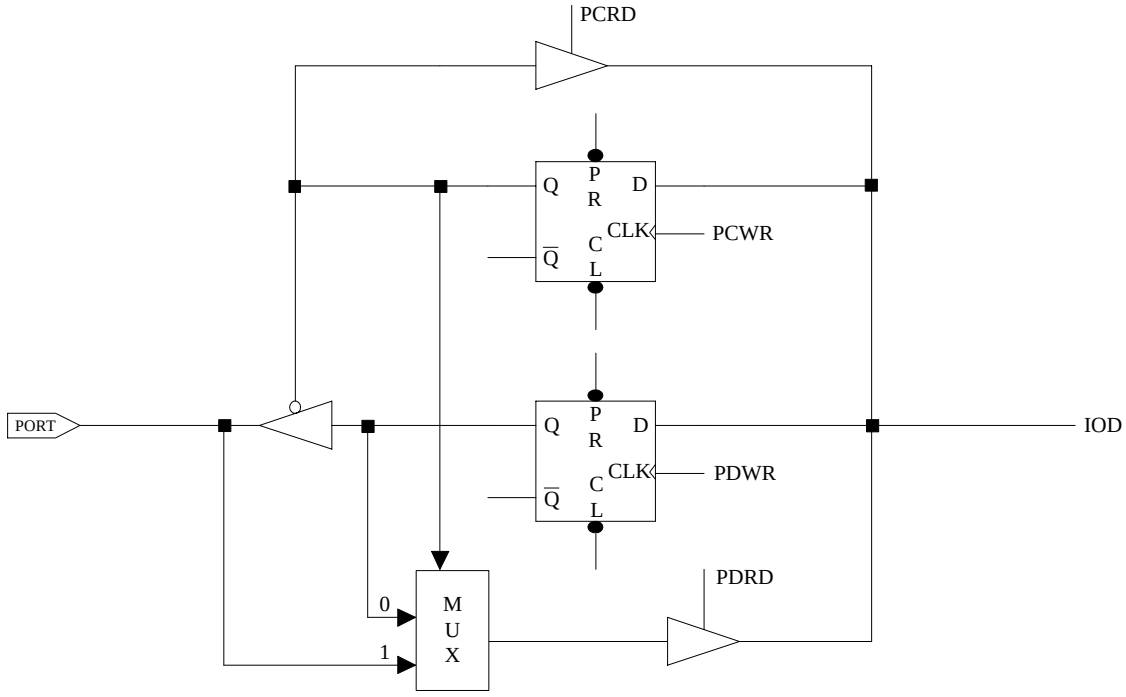


Fig.9_1 The circuit of I/O port and I/O control register

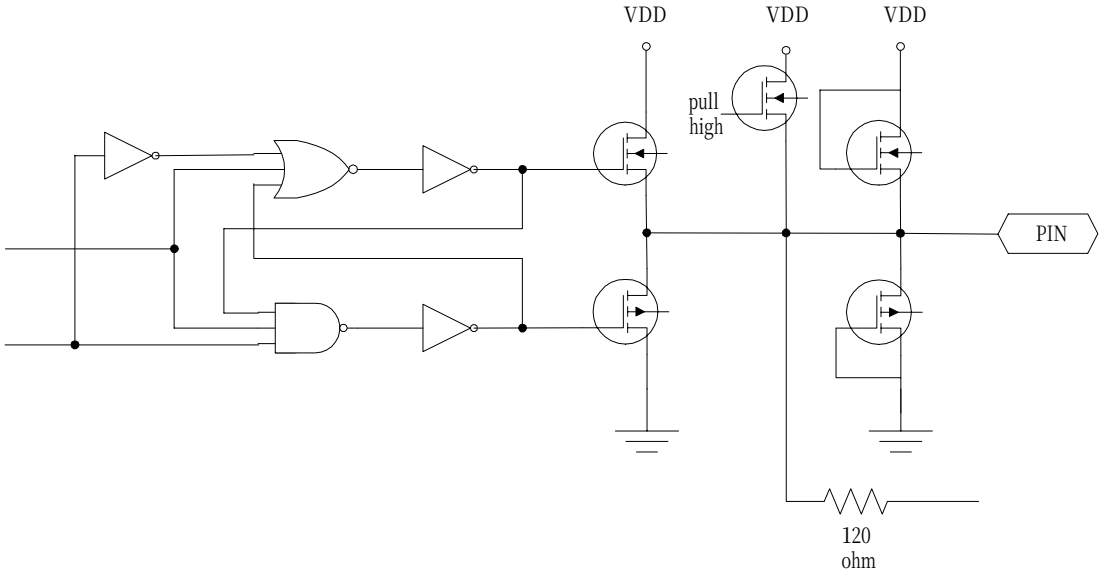


Fig.9_2 The input/output circuit of EM785840 input/output ports

VII.5 RESET

The RESET can be caused by

(1) Power on reset

(2) WDT timeout. (if enabled and in GREEN or NORMAL mode)

(3) /RESET pin pull low (At P71S = 1).

Once the RESET occurs, the following functions are performed.

- The oscillator is running, or will be started.
- The Program Counter (R2) is set to all "0".
- When power on, the upper 3 bits of R3 and the upper 2 bits of R4 are cleared.
- The Watchdog timer and prescaler counter are cleared.
- The Watchdog timer is disabled.

VII.6 Wake-up

The controller provided sleep mode for power saving :

SLEEP mode, RA(7) = 0 + "SLEP" instruction

The controller will turn off all the CPU and crystal. Other circuit with power control like key tone control or PLL control (which has enable register), user has to turn it off by software.

Wake-up from SLEEP mode

(1) WDT time out

(2) External interrupt

(3) /RESET pull low

All these cases will reset controller , and run the program at address zero. The status just like the power on reset.

VII.7 Interrupt

RF is the interrupt status register which records the interrupt request in flag bit. IOCF is the interrupt mask register. Global interrupt is enabled by ENI instruction and is disabled by DISI instruction. When one of the interrupts (when enabled) generated, will cause the next instruction to be fetched from address 008H. Once in the interrupt service routine, the source of the interrupt can be determined by polling the flag bits in the RF register. The interrupt flag bit must be cleared in software before leaving the interrupt service routine and enabling interrupts to avoid recursive interrupts.

VII.8 Instruction Set

Instruction set has the following features:

(1) Every bit of any register can be set, cleared, or tested directly.

(2) The I/O register can be regarded as general register. That is, the same instruction can operates on I/O register.

The symbol "R" represents a register designator which specifies which one of the 64 registers (including operational registers and general purpose registers) is to be utilized by the instruction. Bits 6 and 7 in R4 determine the selected register bank. "b" represents a bit field designator which selects the number of the bit, located in the register "R", affected by the operation. "k" represents an 8 or 10-bit constant or literal value.

INSTRUCTION BINARY	HEX	MNEMONIC	OPERATION	STATUS AFFECTED	Instruction cycle
0 0000 0000 0000	0000	NOP	No Operation	None	1
0 0000 0000 0001	0001	DAA	Decimal Adjust A	C	1
0 0000 0000 0010	0002	CONTW	A → CONT	None	1
0 0000 0000 0011	0003	SLEP	0 → WDT, Stop oscillator	T,P	1
0 0000 0000 0100	0004	WDTC	0 → WDT	T,P	1
0 0000 0000 rrrr	000r	IOW R	A → IOCR	None	1
0 0000 0001 0000	0010	ENI	Enable Interrupt	None	1
0 0000 0001 0001	0011	DISI	Disable Interrupt	None	1
0 0000 0001 0010	0012	RET	[Top of Stack] → PC	None	2
0 0000 0001 0011	0013	RETI	[Top of Stack] → PC Enable Interrupt	None	2
0 0000 0001 0100	0014	CONTR	CONT → A	None	1
0 0000 0001 rrrr	001r	IOR R	IOCR → A	None	1
0 0000 0010 0000	0020	TBL	R2+A → R2 bits 9,10 do not clear	Z,C,DC	2
0 0000 01rr rrrr	00rr	MOV R,A	A → R	None	1
0 0000 1000 0000	0080	CLRA	0 → A	Z	1
0 0000 11rr rrrr	00rr	CLR R	0 → R	Z	1
0 0001 00rr rrrr	01rr	SUB A,R	R-A → A	Z,C,DC	1
0 0001 01rr rrrr	01rr	SUB R,A	R-A → R	Z,C,DC	1
0 0001 10rr rrrr	01rr	DECA R	R-1 → A	Z	1
0 0001 11rr rrrr	01rr	DEC R	R-1 → R	Z	1
0 0010 00rr rrrr	02rr	OR A,R	A ∨ R → A	Z	1
0 0010 01rr rrrr	02rr	OR R,A	A ∨ R → R	Z	1
0 0010 10rr rrrr	02rr	AND A,R	A & R → A	Z	1
0 0010 11rr rrrr	02rr	AND R,A	A & R → R	Z	1
0 0011 00rr rrrr	03rr	XOR A,R	A ⊕ R → A	Z	1
0 0011 01rr rrrr	03rr	XOR R,A	A ⊕ R → R	Z	1
0 0011 10rr rrrr	03rr	ADD A,R	A + R → A	Z,C,DC	1
0 0011 11rr rrrr	03rr	ADD R,A	A + R → R	Z,C,DC	1
0 0100 00rr rrrr	04rr	MOV A,R	R → A	Z	1
0 0100 01rr rrrr	04rr	MOV R,R	R → R	Z	1
0 0100 10rr rrrr	04rr	COMA R	/R → A	Z	1
0 0100 11rr rrrr	04rr	COM R	/R → R	Z	1

0	0101	00rr	rrrr	05rr	INCA R	R+1 → A	Z	1
0	0101	01rr	rrrr	05rr	INC R	R+1 → R	Z	1
0	0101	10rr	rrrr	05rr	DJZA R	R-1 → A, skip if zero	None	2 if skip
0	0101	11rr	rrrr	05rr	DJZ R	R-1 → R, skip if zero	None	2 if skip
0	0110	00rr	rrrr	06rr	RRCA R	R(n) → A(n-1) R(0) → C, C → A(7)	C	1
0	0110	01rr	rrrr	06rr	RRC R	R(n) → R(n-1) R(0) → C, C → R(7)	C	1
0	0110	10rr	rrrr	06rr	RLCA R	R(n) → A(n+1) R(7) → C, C → A(0)	C	1
0	0110	11rr	rrrr	06rr	RLC R	R(n) → R(n+1) R(7) → C, C → R(0)	C	1
0	0111	00rr	rrrr	07rr	SWAPA R	R(0-3) → A(4-7) R(4-7) → A(0-3)	None	1
0	0111	01rr	rrrr	07rr	SWAP R	R(0-3) ↔ R(4-7)	None	1
0	0111	10rr	rrrr	07rr	JZA R	R+1 → A, skip if zero	None	2 if skip
0	0111	11rr	rrrr	07rr	JZ R	R+1 → R, skip if zero	None	2 if skip
0	100b	bbrr	rrrr	0xxx	BC R,b	0 → R(b)	None	1
0	101b	bbrr	rrrr	0xxx	BS R,b	1 → R(b)	None	1
0	110b	bbrr	rrrr	0xxx	JBC R,b	if R(b)=0, skip	None	2 if skip
0	111b	bbrr	rrrr	0xxx	JBS R,b	if R(b)=1, skip	None	2 if skip
1	00kk	kkkk	kkkk	1kkk	CALL k	PC+1 → [SP] (Page, k) → PC	None	2
1	01kk	kkkk	kkkk	1kkk	JMP k	(Page, k) → PC	None	2
1	1000	kkkk	kkkk	18kk	MOV A,k	k → A	None	1
1	1001	kkkk	kkkk	19kk	OR A,k	A ∨ k → A	Z	1
1	1010	kkkk	kkkk	1Akk	AND A,k	A & k → A	Z	1
1	1011	kkkk	kkkk	1Bkk	XOR A,k	A ⊕ k → A	Z	1
1	1100	kkkk	kkkk	1Ckk	RETL k	k → A, [Top of Stack] → PC	None	2
1	1101	kkkk	kkkk	1Dkk	SUB A,k	k-A → A	Z,C,DC	1
1	1110	0000	0001	1E01	INT	PC+1 → [SP] 001H → PC	None	1
1	1110	100k	kkkk	1E8k	PAGE k	K->R5(4:0)	None	1
1	1111	kkkk	kkkk	1Fkk	ADD A,k	k+A → A	Z,C,DC	1

***** 1 Instruction cycle = 2 main CLK***

VII.9_1 Code Option

EM78P5840 CODE Option Register

12	11	10	9	8	7	6	5	4	3	2	1	0
IR3	IR2	IR1	IR0	P71S	P70S	OSCM1	OSCM0	IRC2S	MER	1	1	/POT0

Bit 0 (/POT0): program ROM protect option.

If set 1 to the bit, program memory can be access; else if clear this bit , program memory can not be access.

Bit 3(MER) : Memory error recover function

0 ➔ disable memory error recover function

1 ➔ enable memory error recovery function

If user enable memory error recovery function, MCU will improve effect from environment noise**.**

Bit 4 (IRC2S): Internal RC oscillating frequency (for system CLK) select.

0 ➔ 2M Hz

1 ➔ 4M Hz

Bit5~Bit6 (OSCM0~OSCM1): EM78P5840 oscillating mode select.

OSCM1	OSCM0	Oscillating mode
0	0	IRC mode
0	1	ERIC mode
1	X	Crystal mode

Bit 7 (P70S): PORT70 function select bit:

OSCM1	OSCM0	P70S	PORT70 status
0	0	X	General Purpose IO
0	1	X	OSC input, please cascade resister to AVDD
1	X	1	PLLC output, please cascade capacitor to AVSS
1	X	0	General Purpose IO, PLL function will disable

Bit 8 (P71S): PORT71 function select bit:

0 ➔ /RESET pin selected..

1 ➔ General purpose INPUT port “PORT71” selected

Bit 9~ Bit12 (IR0~IR3): By setting IR0~IR3, IRC mode’s oscillating frequency can be adjust. Next table show the trimming code table of IRC frequency.

IR3~IR0	Frequency
0000	1.05*F
0001	1.10*F
0010	1.15*F
0011	1.20*F
0100	1.25*F
0101	1.30*F
0110	1.35*F
0111	1.40*F
1000	0.65*F
1001	0.70*F
1010	0.75*F
1011	0.80*F
1100	0.85*F
1101	0.90*F
1110	0.95*F
1111	1.0*F

* ”F” means the frequency of IRC output.

VII.10 PWM (Pulse Width Modulation)

(1) Overview

In PWM mode, both PWM1 and PWM2 pins produce up to a 10-bit resolution PWM output (see. Fig.10 for the functional block diagram). A PWM output has a period and a duty cycle, and it keeps the output in high. The baud rate of the PWM is the inverse of the period. Fig.11 depicts the relationships between a period and a duty cycle.

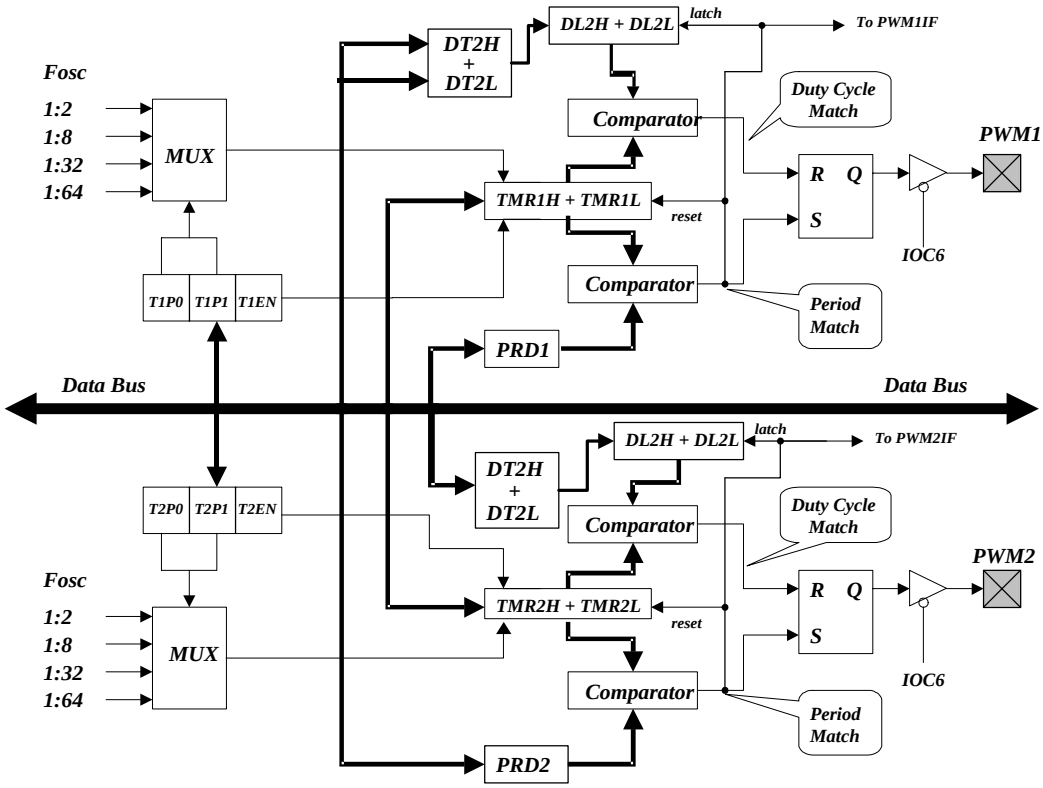


Fig.10 The Functional Block Diagram of the Dual PWMs

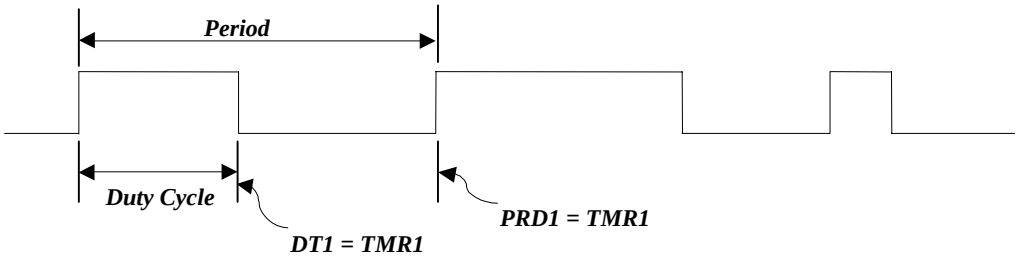


Fig.11 The Output Timing of the PWM

(2) Increment Timer Counter (TMRX: TMR1H/TWR1L or TMR2H/TWR2L)

TMRX are ten-bit clock counters with programmable prescalers. They are designed for the PWM module as baud rate clock generators. TMRX can be read, written, and cleared at any reset conditions. If employed, they can be turned down for power saving by setting T1EN bit to 0.

(3) PWM Period (PRDX : PRD1 or PRD2)

The PWM period is defined by writing to the PRDX register. When TMRX is equal to PRDX, the following events occur on the next increment cycle:

- TMRX is cleared.
- The PWMX pin is set to 1.

• The PWM duty cycle is latched from DT1/DT2 to DTL1/DTL2.
< Note > The PWM output will not be set, if the duty cycle is 0;
• The PWMXIF pin is set to 1.

The following formula describes how to calculate the PWM period:

PERIOD = (PRDX + 1) * 4 * (1/Fosc) * (TMRX prescale value)

Where Fosc is system clock

(4) PWM Duty Cycle (DTX: DT1H/ DT1L; DTL: DL1H/DL1L)

The PWM duty cycle is defined by writing to the DTX register, and is latched from DTX to DLX while TMRX is cleared. When DLX is equal to TMRX, the PWMX pin is cleared. DTX can be loaded at any time. However, it cannot be latched into DTL until the current value of DLX is equal to TMRX.

The following formula describes how to calculate the PWM duty cycle:

Duty Cycle = (DTX) * (1/Fosc) * (TMRX prescale value)

(5) PWM Programming Procedures/Steps

Load PRDX with the PWM period.
(1) Load DTX with the PWM Duty Cycle.
(2) Enable interrupt function by writing IOCF PAFE0, if required.
(3) Set PWMX pin to be output by writing a desired value to IOCC PAGE0.
Load a desired value to R5 PAGE3 with TMRX prescaler value and enable both PWMX and TMRX.

(6) Timer

Timer1 (TMR1) and Timer2 (TMR2) (TMRX) are 10-bit clock counters with programmable prescalers, respectively. This is designed for the PWM module as baud rate clock generators. TMRX can be read, written, and cleared at any reset conditions.

The figure in the next page shows TMRX block diagram. Each signal and block are described as follows:

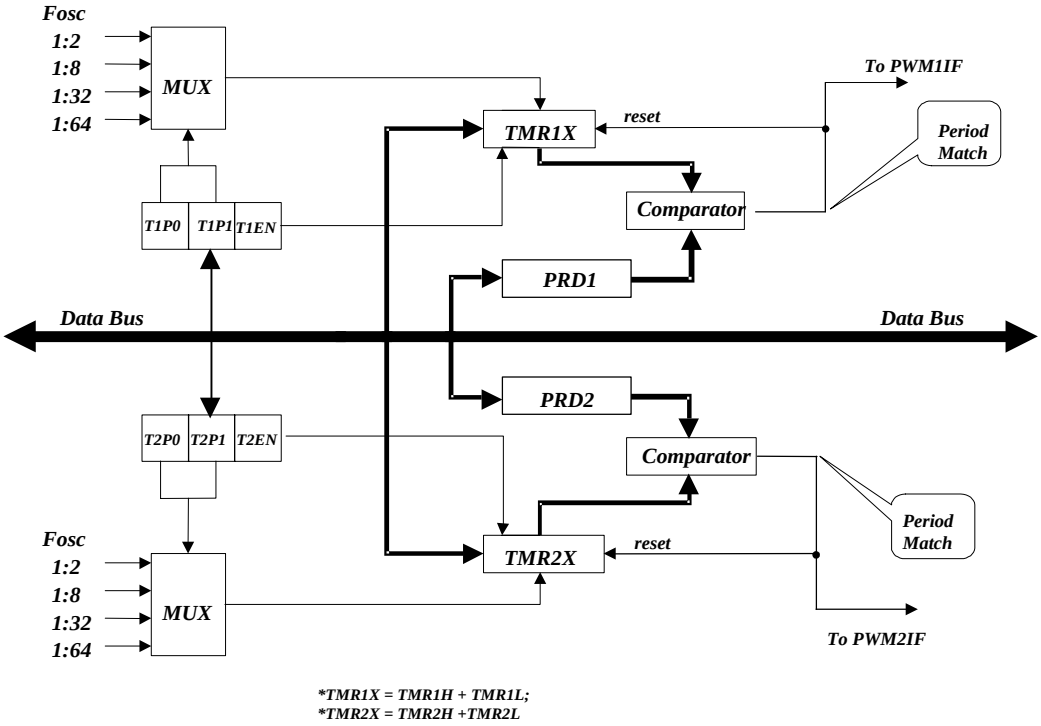


Fig.12 TMRX Block Diagram

- Fosc: Input clock.
- Prescaler (T1P0 and T1P1): Options of 1:2, 1:8, 1:32, and 1:64 are defined by TMRX. It is cleared when any type of reset occurs.
- TMR1X (TMR1H/TWR1L):Timer X register; TMRX is increased until it matches with PRDX, and then is reset to 0. TMRX cannot be read.
- PRDX (PRD1): PWM period register.

When defining TMRX, refer to the related registers of its operation as shown in prescale register. It must be noted that the PWMX bits must be disabled if their related TMRXs are employed. That is, bit 6 of the PWMCON register must be set to '0'.

Related Control Registers(R5 PAGE3) of TMR1 and TMR2

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM2E	PWM1E	T2EN	T1EN	T2P1	T2P0	T1P1	T1P0

Timer programming procedures/steps

Load PRDX with the TIMER period.
Enable interrupt function by writing IOCF PAGE0, if required
Load a desired value to PWMCON with the TMRX prescaler value and enable both TMRX and disable PWMX.

VII.11 Oscillator

The EM78P5840 can be operated in two different oscillator modes, each of them are crystal mode and RC mode. Users can select one of them by setting code option. The descript of these two oscillator mode are as below:

(1) Crystal mode:

For crystal mode operation, one crystal and tow capacitances is needed for external circuit. In this mode, eFTP5840 can be run in three active mode include normal mode, green mode and sleep mode. The advantages of this mode are low power consumption (in green mode) and with more precise main CLK. Next figure show the application circuit of crystal mode. Pin XIN and pin XOUT can be connected with a crystal directly to generate oscillation. By clear code option"P70S" to 0, PORT70 can switch to general IO (disable PLL function and EM78P5840 can not active on normal mode); /RESET pin can switch to PORT71 if clear "P71S" to 0.

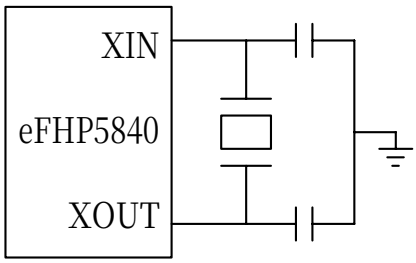


Fig 13: Application circuit of Crystal mode

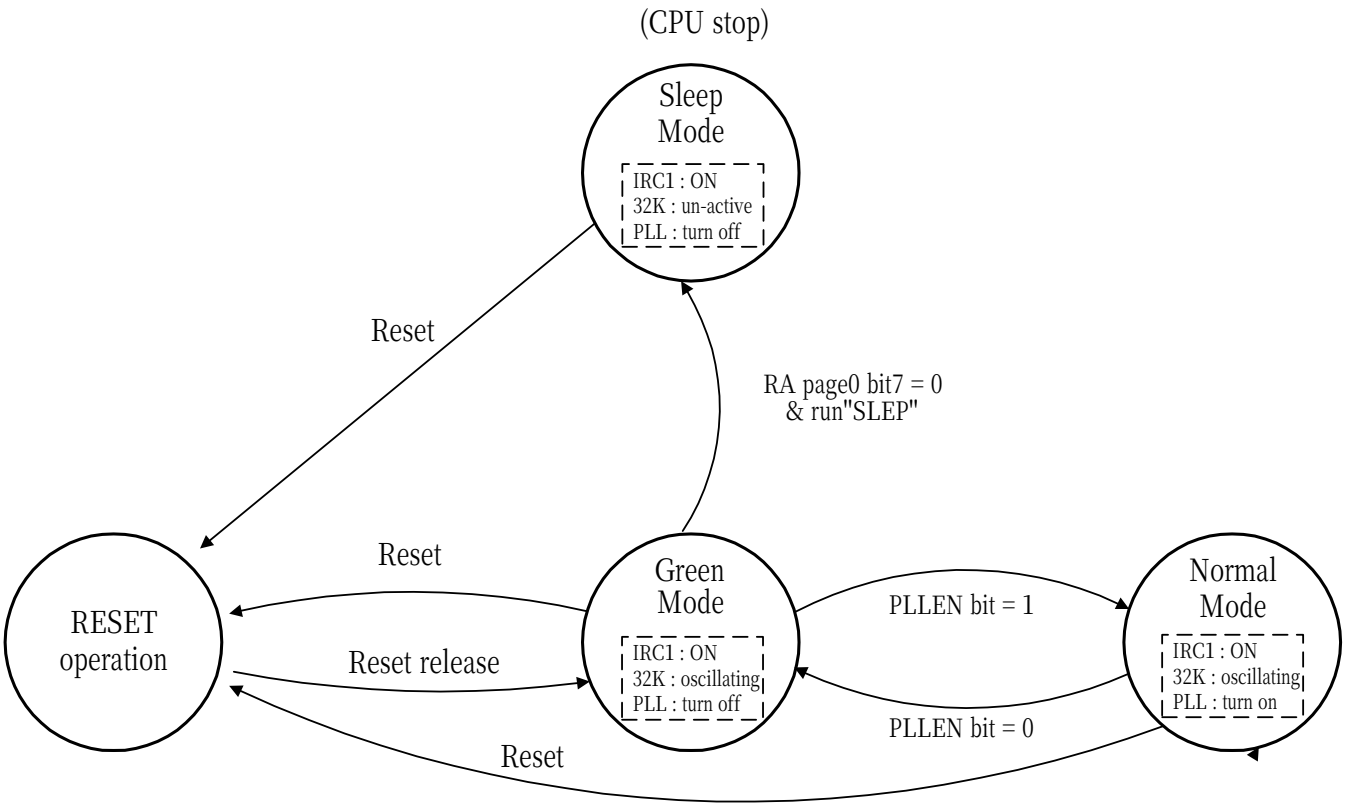


Fig 14: The relative of Crystal mode's normal, green and sleep mode

(2) IRC mode:

For some applications that do not require precise timing calculation, the RC oscillator could offer users with an effective cost savings. eFTP5840 offer a versatile internal RC mode with default frequency value of 4M and 2MHz. In this mode, PLLC, XIN, XOUT and /RESET pins can defined to general purpose IO. The IRC frequency will drift with the variation of voltage, temperature and process:

The frequency deviation of IRC mode:

Internal RC	Freq range (before adjust IR0~IR3) (IR0~IR3 = 1111)	Freq range (after adjust IR0~IR3)
4M Hz	2.8M ~ 5.2M	3.6M ~ 4.4M
2M Hz	1.4M ~ 2.6M	1.8 M ~ 2.2M

**The frequency of IRC output can be adjust by setting IR0~IR3 in code option. By setting IR0~IR3, the frequency deviation can be compensation. Please refer to code option to detail.*

In IRC mode, PORT60, PORT61 and PORT70 are defined to bi-direction IO. By clearing P71S in code option to 0, /RESET pin can also switch to INPUT pin (PORT71). In IRC mode, only two active modes can be achieved, please refer to next figure to detail.

(3) ERIC mode:

ERIC mode is equipped with an internal capacitor and an external resistor (connected to VDD). The internal capacitor functions as temperature compensator. In order to obtain more accurate frequency, a precise resistor is recommended.

Nevertheless, it should be noted that the frequency of the RC oscillator is influenced by the supply voltage, the values of the even by the operation temperature. Moreover, the frequency also changes slightly from one chip to another due to the manufacturing process variation. Besides, the package types, and the way the PCB is layout, have certain effect on the system frequency. About the application is as below:

The frequency deviation of ERIC mode:

Internal C, external R	Freq range
4M Hz (R=51K)	3.5M ~ 4.4M
2M Hz(R=100K)	1.8M ~ 2.2M

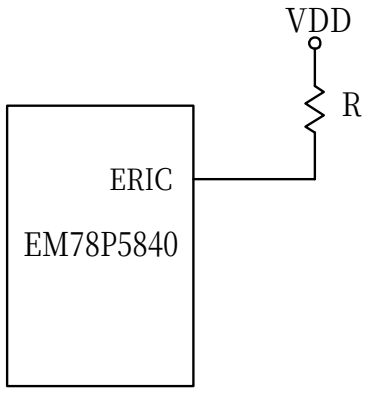


Fig 15: Application circuit of ERIC mode

ERIC's oscillating frequency will base on IRC2's CLK (determined on code option "IRC2S"). For example, if IRC2S = 0, IRC2's oscillating frequency is 2M Hz. At this time, by adjusting R, system CLK will be changed. But the system CLK will always greater than 2M. That is to say, system CLK can only be adjusted between 2M to 6M. Next two table show the corresponding between system oscillating CLK and the value of external resister.

The corresponding between system oscillating CLK and the value of external resister

Frequency (Hz)	External resister (ohm)	Operating Voltage (VDD)
6M	34K	3.0 ~5.5 V
5M	41K	2.8 ~5.5 V
4M	51K	2.5 ~5.5 V
3.58M	57K	2.2 ~5.5 V
2.1M	97K	2.2 ~5.5 V

*Only 2 types active mode (normal mode and sleep mode) are permitting in RC mode.

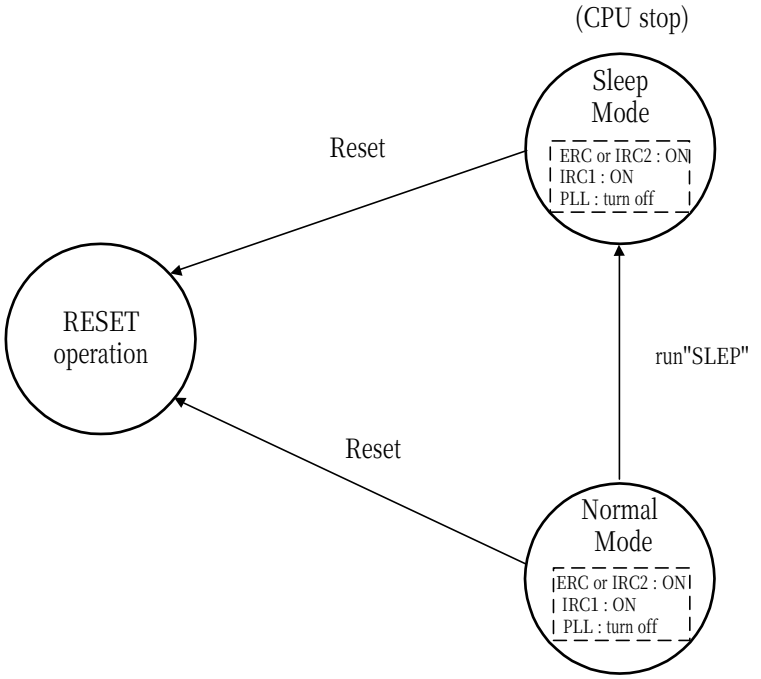


Fig 15: The relative of IRC and ERIC mode's normal and sleep mode

VII.12 Power on Considerations

Any micro-controller is not guaranteed to start to operate properly before the power supply stabilizes at its steady states. EM78P5840 power on reset voltage range is 1.6V ~ 2.0V. Under customer application, VDD must drop to below 1.6V and remains OFF for 10uS before power can be switched on again. This way, EM78P5840 will reset and work normally. The extra external reset circuit will work well if VDD can rise at very fast speed (50mS or less). However, under most cases where critical applications are involved, extra devices are required to assist in solving the power-up problems.

VII.13 External Power on Reset circuit

By Setting code option "P71S" to 1, /RESET pin is selected. Next figure is an external RC to produce the reset pulse. The pulse width should be kept long enough for VDD to reach minimum operation voltage. The diode D acts as a short circuit at the moment of power down. The capacitor C will discharged rapidly and fully.

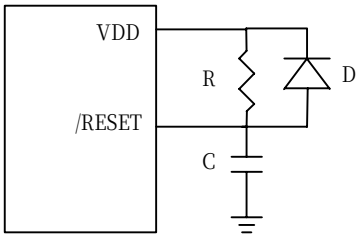


Fig 15: External power on reset circuit 1

POR reset voltage is influenced in process or temperature. For some application, a constant reset voltage is important. Next circuit will support a adjust reset voltage. By adjusting R41 and R46, POR reset voltage will be a constant (Vpor) and the potential on /RESET pin will drop to 0 when VDD drop to below Vpor. Next plot show the relative between VDD and Vpor. When R41 = 3.9M ohm and R46 = 910K ohm, /RESET will keep to 0 if VDD is below 2.24V and will active after VDD upper to 2.1V.

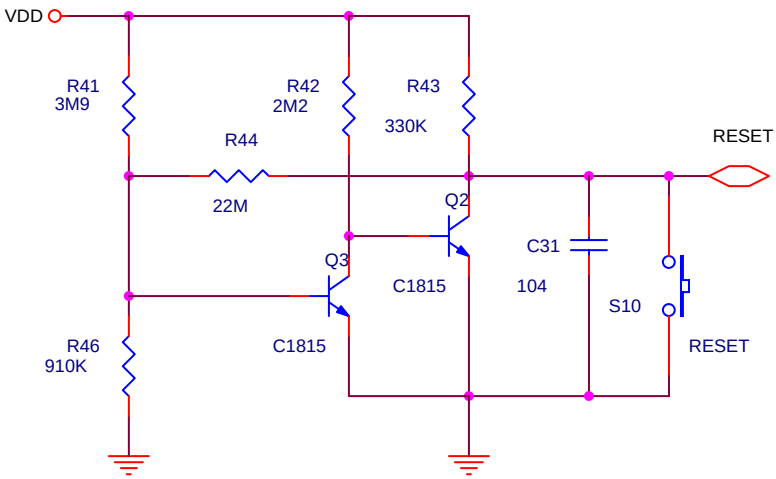


Fig 16: External power on reset circuit 2

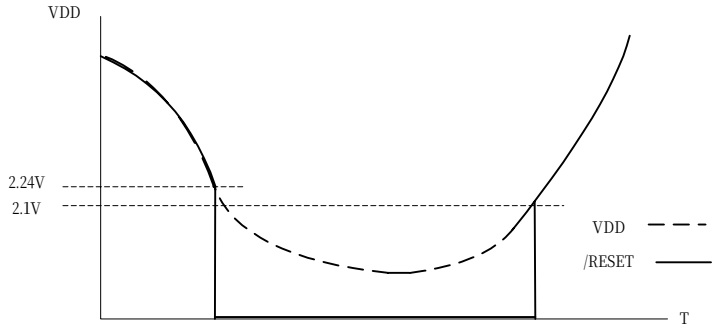


Fig 17: The relative between VDD and Vpor

VIII. Absolute Operation Maximum Ratings

RATING	SYMBOL	VALUE	UNIT
DC SUPPLY VOLTAGE	VDD	-0.3 To 6	V
INPUT VOLTAGE	Vin	-0.5 to VDD +0.5	V
OPERATING TEMPERATURE RANGE	Ta	0 to 70	℃

IX. DC Electrical Characteristic

(Ta = 25°C, AVDD=VDD=5V±5%, VSS=0V)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input leakage current for input pins	IIL1	VIN = VDD, VSS			±1	μA
Input leakage current for bi-directional pins	IIL2	VIN = VDD, VSS			±1	μA
Input high voltage (except P71)	VIH		2.5			V
Input low voltage (except P71)	VIL				0.8	V
P71 Input high voltage	VIH		2.0			V
P71 Input low voltage	VIL				0.8	V
Input high threshold voltage	VIHT	/RESET, TCC	2.0			V
Input low threshold voltage	VILT	/RESET, TCC			0.8	V
Clock input high voltage	VIHX	OSCI	3.5			V
Clock input low voltage	VILX	OSCI			1.5	V
Output high voltage for PORTC1~PORTC2	VOH1	IOH = -6mA	2.4			V
Output high voltage for PORT60~PORT67; PORT7	VOH2	IOH = -10mA	2.4			V
Output high voltage for PORT9	VOH3	IOH = -15mA	2.4			V
Output low voltage for PORTC1~PORTC2	VOL1	IOH = 6mA			0.4	V
Output low voltage for PORT60~PORT67; PORT7	VOL2	IOH = 10mA			0.4	V
Output low voltage for PORT9	VOL3	IOH = 15mA			0.4	V
Pull-high current	IPH	Pull-high active input pin at VSS		-10	-15	μA
Power down current (SLEEP mode)	ISB1	All input and I/O pin at VDD, output pin floating, WDT disabled		1	4	μA
Low clock current (GREEN mode)	ISB2	CLK=32.768KHz, All analog circuits disabled, All input and I/O pin at VDD, output pin floating, WDT disabled		25	35	μA
Operating supply current (Normal mode)	ICC1	/RESET=High, CLK=3.582MHz, All analog circuits disabled, output pin floating		1.5	2.5	mA

XI. AC Electrical Characteristic

CPU instruction timing (Ta = 25°C, AVDD=VDD=5V, VSS=0V)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input CLK duty cycle	Dclk		45	50	55	%
Instruction cycle time	Tins	32.768kHz		60		us
		3.582MHz		550		ns
Device delay hold time	Tdrh			16		ms
TCC input period	Ttcc	Note 1	(Tins+20)/N			ns
Watchdog timer period	Twdt	Ta = 25°C	16-30%	16	16+30%	ms

Note 1: N= selected prescaler ratio.

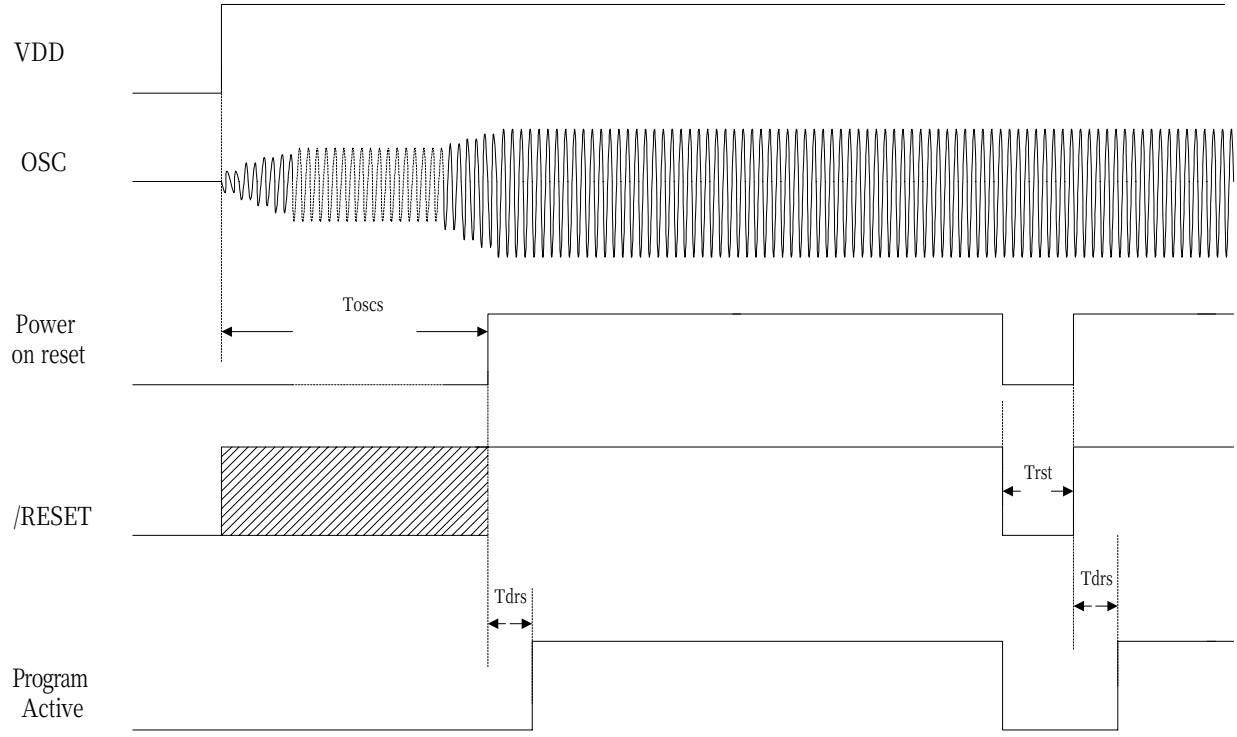
ADC characteristic (VDD = 5V, Ta = +25°C, for internal reference voltage)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Upper bound offset voltage	Vofh			44	52.8	mV
Lower bound offset voltage	Vofl			32	38.4	mV

*These parameters are characterized but not tested.
* About ADC characteristic, please refer to next page.

Timing characteristic (AVDD=VDD=5V,Ta=+25°C)

Description		Symbol	Min	Typ	Max	Unit
Oscillator timing characteristic						
Crystal start up	32.768kHz	Tosc	400		1500	ms
	3.579MHz PLL			5	10	us
Timing characteristic of reset						
The minimum width of reset low pulse		Trst	3			uS
The delay between reset and program start		Tdrs		18		mS



The relative between OSC stable time and power on reset

EM78P5840 operation voltage(X axis → min VDD ; Y axis → main CLK):

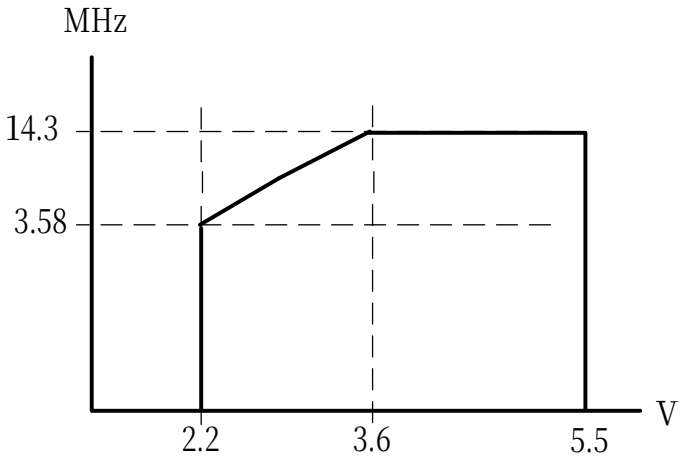


Fig.18 The relative between operating voltage and main CLK

EM785840's 10 bit ADC characteristic

EM785840 build in 10 bit resolution, multi channel ADC function. In ideal, if ADC's reference voltage is 5V, the ADC's LSB will be 5V/1024. But in practical, for some physics or circuit's character, some un-ideal will effect the converter result. As the next figure, offset voltage will reduce AD's converter range. If AD's input voltage less than VOFL, ADC will output 0; in opposition, if input voltage is larger than (VDD-VOFH), ADC will output 1023. That is to say the physics AD converter range will replace by (VDD-VOFH+LSB-VOFL+LSB). If we defined that VRB = VOFL – LSB and VRT = VDD-VOFH+LSB, the physics LSB is:

LSB = (VRT - VRB) / 1024
= ***(VDD – (VOFH+VOFL)) / 1022***

For real operating, please think about the effect of AD's offset voltage. If converter the range of (VRT - VRB), the AD converter's opposite result will be précised.

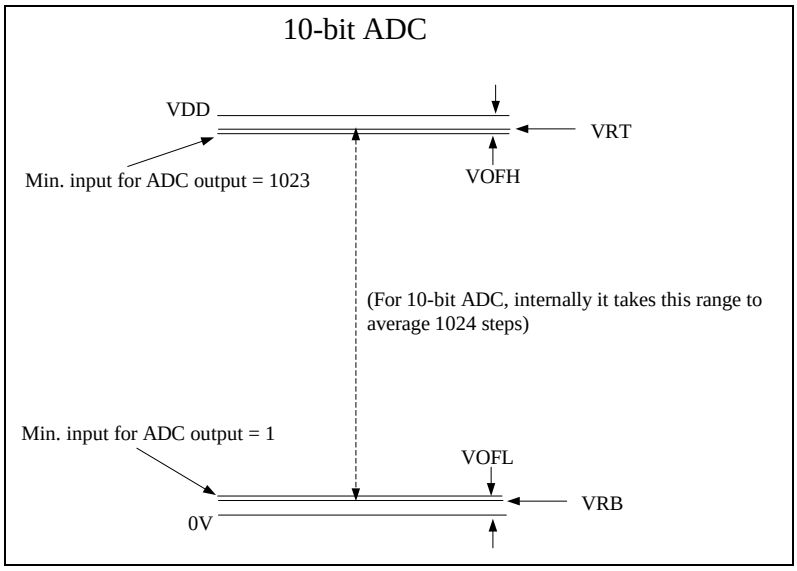
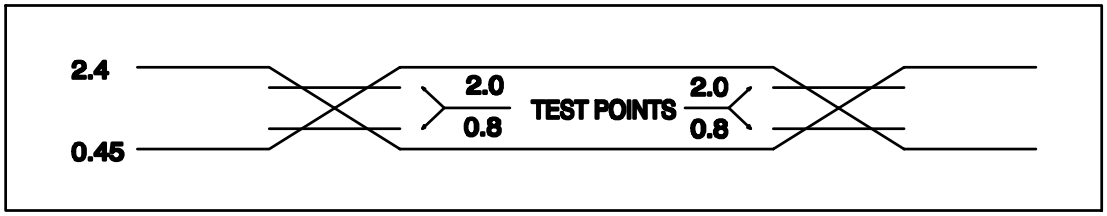


Fig.19 The relative between ADC and offset voltage

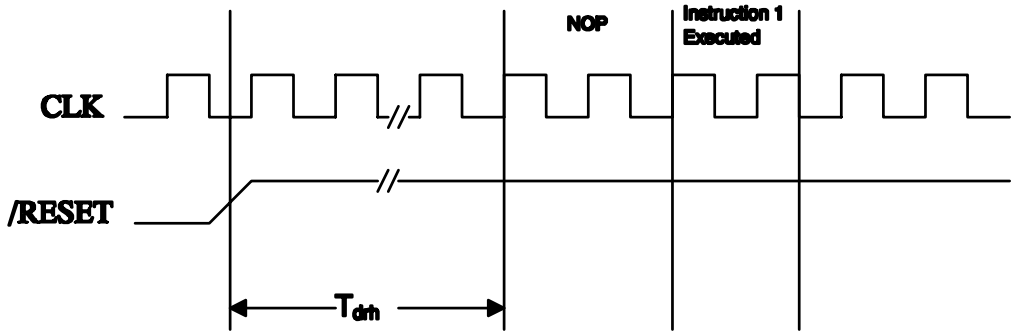
XII. Timing Diagrams

AC Test Input/Output Waveform



AC Testing: Input are driven at 2.4V for logic "1", and 0.45V for logic "0". Timing measurements are made at 2.0V for logic "1", and 0.8V for logic "0".

RESET Timing



TCC Input Timing

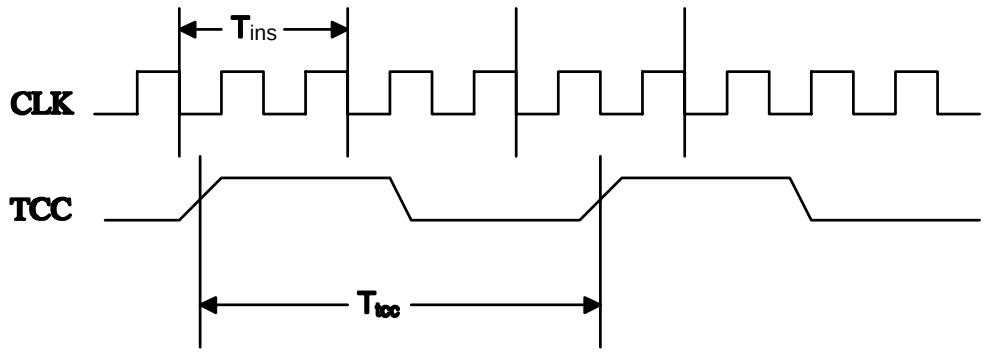


Fig.20 AC timing

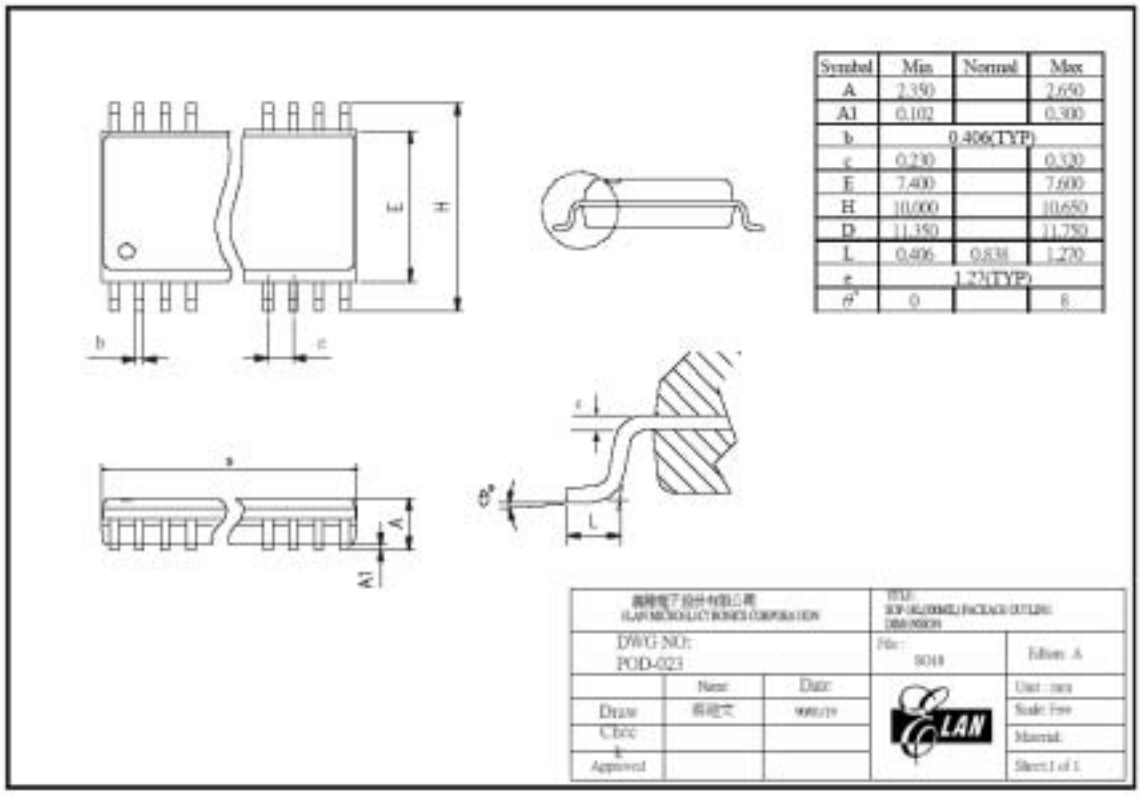
XIII. EM78P5840 OTP ROM burning pins

One time programmable ROM burner pin

OTP PIN NAME	MASK ROM PIN NAME	P.S.
VDD	AVDD	
VPP	/RESET	
DINCK	P65	
ACLK	P64	
PGMB	P63	
OEB	P62	
DATA	P73	
GND	AVSS	

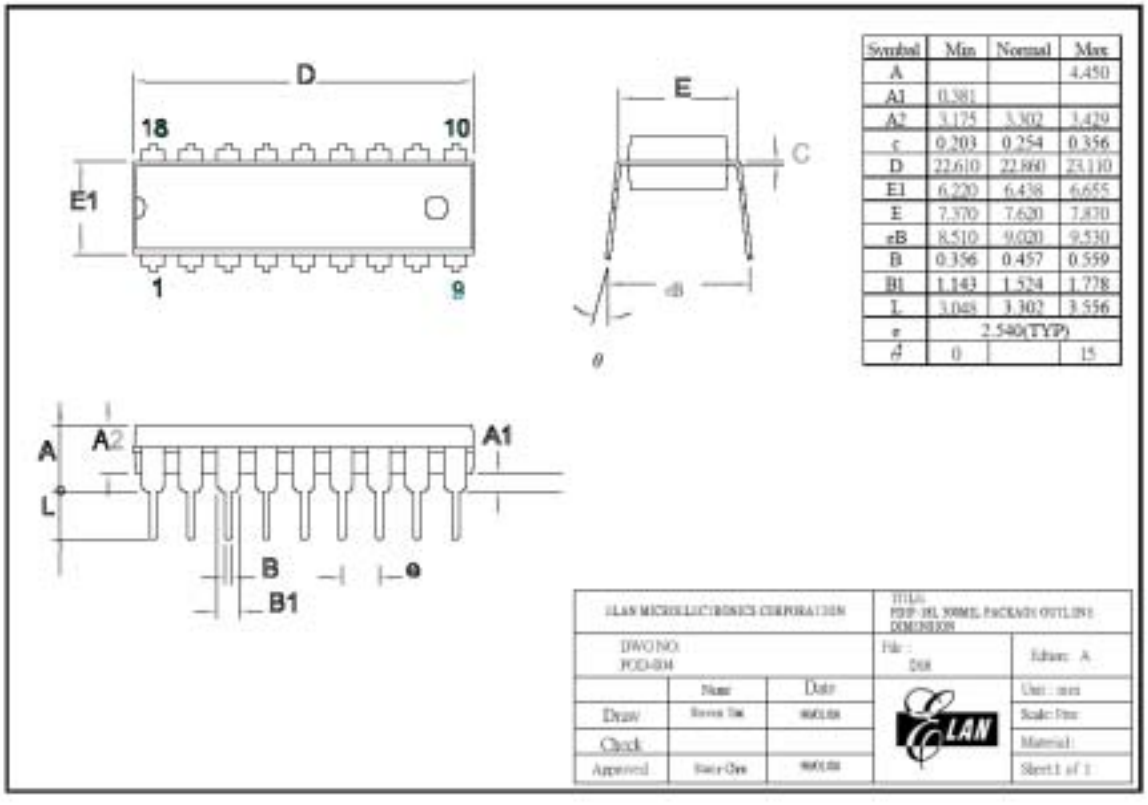
Appendix: Package spec of EM78P5840/5841/5842

EM78P5840M



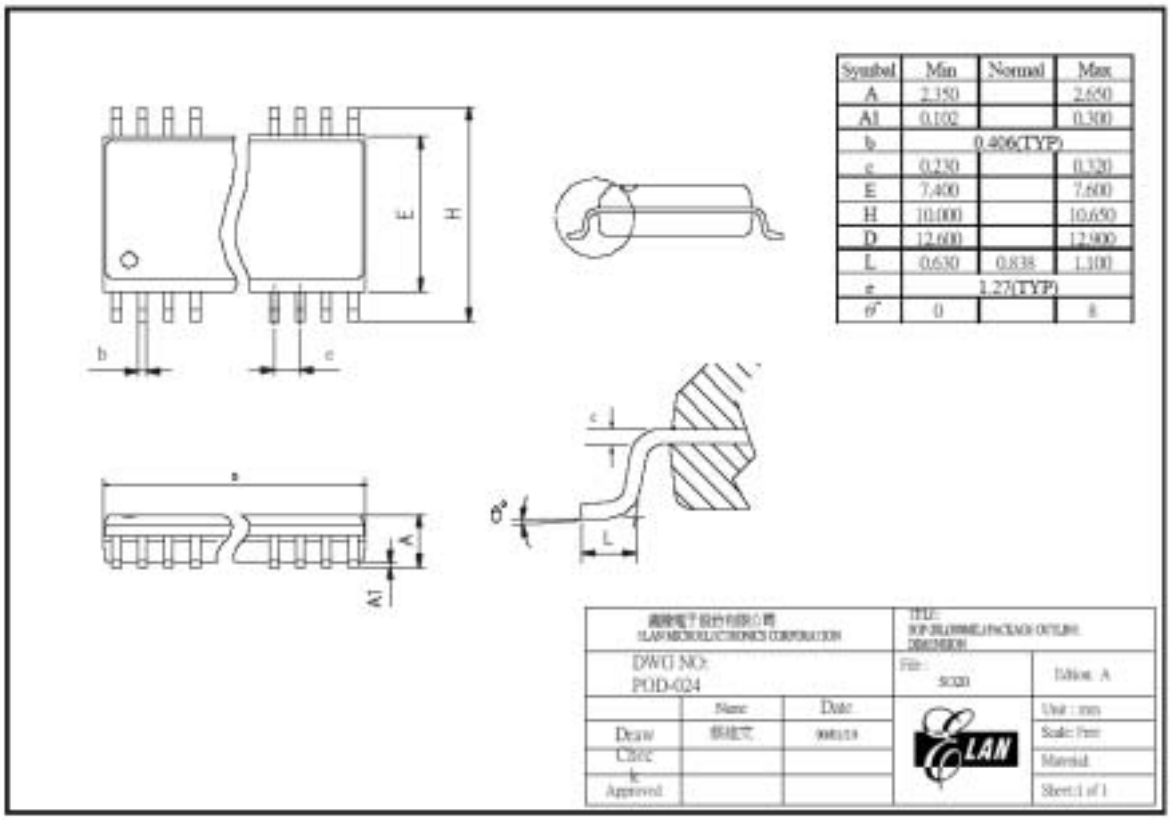
Symbol	Min	Normal	Max
A	2.350		2.650
A1	0.102		0.300
b		0.406(TYP)	
c	0.230		0.320
E	7.400		7.600
H	10.000		10.650
D	11.350		11.750
L	0.406	0.838	1.270
e		1.27(TYP)	
θ°	0		8

EM78P5840P



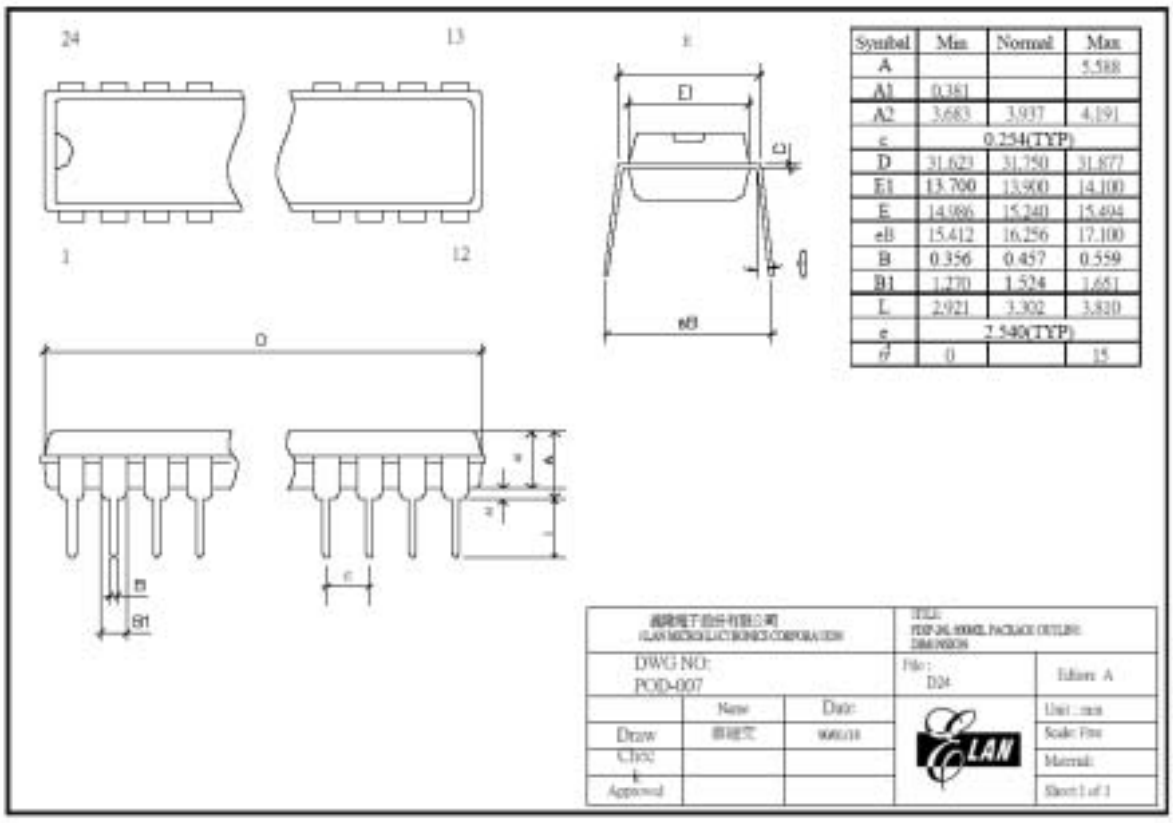
Symbol	Min	Normal	Max
A			4.450
A1	0.381		
A2	3.175	3.302	3.429
c	0.203	0.254	0.356
D	22.610	22.860	23.110
E1	6.220	6.438	6.655
E	7.370	7.620	7.870
eB	8.510	9.020	9.530
B	0.356	0.457	0.559
B1	1.143	1.524	1.778
L	3.048	3.302	3.556
e		2.540(TYP)	
θ	0		15

EM78P5841M



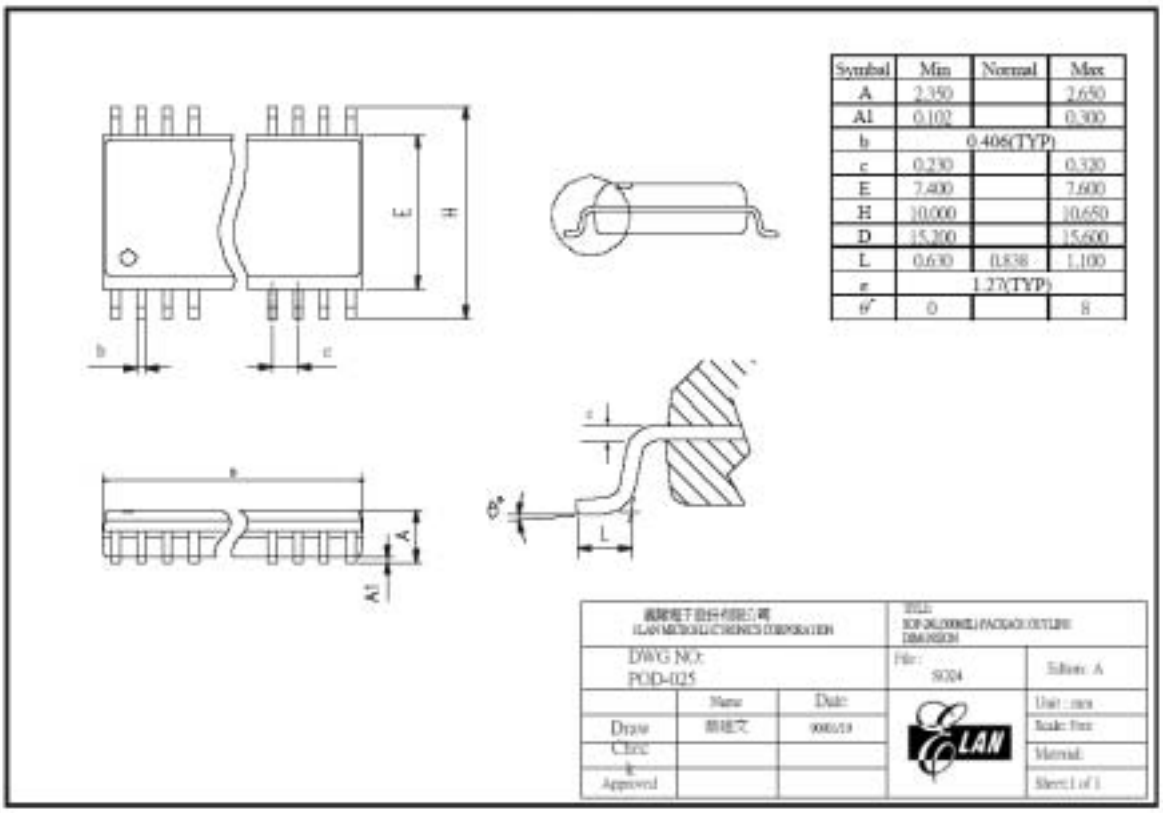
Symbol	Min	Normal	Max
A	2.350		2.650
A1	0.102		0.300
b		0.406(TYP)	
c	0.230		0.320
E	7.400		7.600
H	10.000		10.650
D	12.600		12.900
L	0.630	0.838	1.100
e		1.27(TYP)	
θ°	0		8

EM78P5841P



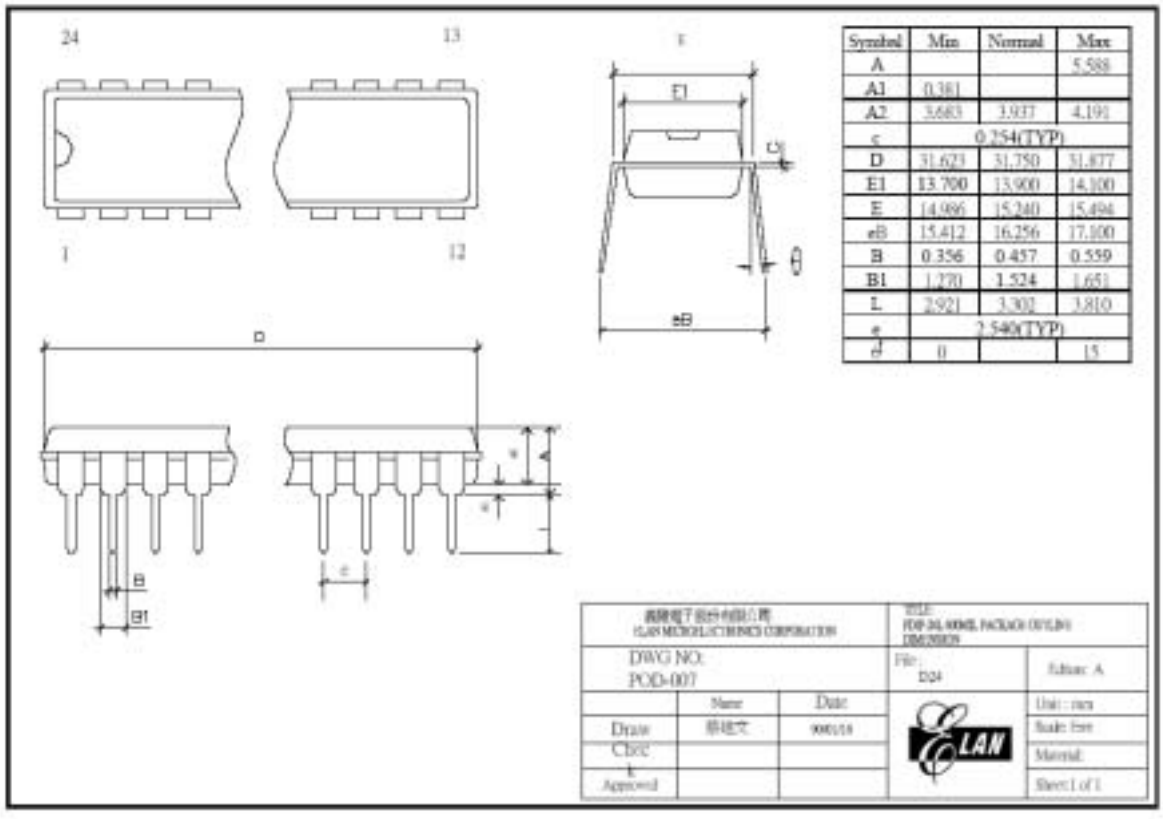
Symbol	Min	Normal	Max
A			5.588
A1	0.381		
A2	3.683	3.937	4.191
c		0.254(TYP)	
D	31.623	31.750	31.877
E1	13.700	13.900	14.100
E	14.986	15.240	15.494
eB	15.412	16.256	17.100
B	0.356	0.457	0.559
B1	1.270	1.524	1.651
L	2.921	3.302	3.810
e		2.540(TYP)	
θ°	0		15

EM78P5842M



Symbol	Min	Normal	Max
A	2.350		2.650
A1	0.102		0.300
b		0.406(TYP)	
c	0.230		0.320
E	7.400		7.600
H	10.000		10.650
D	15.200		15.600
L	0.630	0.838	1.100
e		1.27(TYP)	
θ°	0		8

EM78P5842P



Symbol	Min	Normal	Max
A			5.588
A1	0.381		
A2	3.683	3.937	4.191
c		0.254(TYP)	
D	31.623	31.750	31.877
E1	13.700	13.900	14.100
E	14.986	15.240	15.494
eB	15.412	16.256	17.100
B	0.356	0.457	0.559
B1	1.270	1.524	1.651
L	2.921	3.302	3.810
e		2.540(TYP)	
θ°	0		15