T-90-60
T-42-11-09

CG10 Gate Array Device Description

Device Name	2-input Gate Equivalency[1]	Cell Propagation Delay	Maximum Number of Signal Pins[2]	I/O Options	Supply Voltage	Operating Temperature Range
CG10272	3,256 gates	0.5 ns (F/O = 2, 2-input NAND gate)	108	Input: Normal buffer Clock driver Schmitt trigger CMOS input Input pull-up/ pull-down Output: Normal buffer 3-state Bidirectional Driver output Edge rate control	5 V ± 5% Extended Voltage range of operation optional Please contact Fujitsu	0 to 70°C Extended temperature range optional Please contact Fujitsu
CG10342	4,032 gates		123			
CG10492	5,572 gates		148			
CG10572	6,510 gates		163			
CG10692	7,684 gates		163			
CG10103	11,080 gates		188			
CG10133	14,720 gates		220			

[1]The gate counts in parentheses show the number of basic cells (BCs) on chip, including BCs used for I/O buffers. The UHB2 I/O buffers are implemented using basic cells.
[2]The maximum number of signal pins depends on the selected packages and output drive requirement.
[3]Design implementation dependent.
[4]Values for normal driver and clock buffer.

CG10 Gate Array Package Options

Device Name	Dual In-line Package							Quad Flat Package									
	22	24	28	40	42	48	64	44	48	64	80	100	120	160	176	196	208
CG10272	P	P	P, P_S	C ,P	C, C_S P, P_S	C,P, P_S	P_S	P	C,P^2	P	P	C,P	P				
CG10342		C,P	C, P	C, P	C_S,P_S P	C,P, P_S	P_S		C,P^2	P	P	C,P	P				
CG10492		P	P	P	C,P, P_S	C,P, P_S	P_S			P	P	P	P	P			
CG10572			P	P	P,P_S	P,P_S	P_S			P	P	P	C,P	P			
CG10692				P	P,P_S	P,P_S	P_S			P	P	P	C,P	P			
CG10103										P^1	P^1	P^1	C,P	C,P	P^1		
CG10133													P^1	P^1	P^1	P^1	P^1

C = Ceramic Package
P = Plastic Package
C_S = Ceramic shrink style package (DIP with pins spaced at 70 mils center to center; Quad flat packages with pins spaced at 20 mils center to center).
P_S = Plastic shrink style package (DIP with pins spaced at 70 mils center to center).
[1]Under development.
[2]48-pin flat packages has two body size options

Relative Power Dissipation at 10 MHz[3]	DC Characteristics					Device Name
	Output High Voltage	Output Low Voltage	Input High Voltage	Input Low Voltage	Input Leakage Current	
150 mW	4.0 V min. at I_{OH} = −2 mA I_{OH} = −4 mA I_{OH} = −8 mA	0.4 V max. at I_{OL} = 3.2 mA, I_{OL} = 8 mA I_{OL} = 12.0 mA 0.5 V max at I_{OL} = 24 mA	2.2 V min.[4]	0.8 V max.[4]	± 10 µA max. for Input Buffer and 3-state Output	CG10272
200 mW						CG10342
200 mW						CG10492
200 mW						CG10572
250 mW						CG10692
250 mW						CG10103
250 mW						CG10133

Leadless Chip Carrier				J-Leaded Chip Carrier				Pin Grid Array Package						Device Name
48	64	68	84	28	44	68	84	64	88	135	179	208	256	
C	C	C		P	P	P	P	C,P	C,P	C				CG10272
C	C	C		P	P	P	P	C,P	C,P	C				CG10342
C	C	C		P	P	P	P	C,P	C,P	C,P	C			CG10492
C	C	C			P	P	P	C,P	C,P	C,P	C	C		CG10572
	C	C			P	P	P	C,P	C,P	C,P	C	C		CG10692
	C	C	C					C,P	C,P	C,P	C	C	C	CG10103
								C	C	C	C	C	C	CG10133