



# CED75A3/CEU75A3

## N-Channel Enhancement Mode Field Effect Transistor

### FEATURES

- 25V, 60A,  $R_{DS(ON)} = 9m\Omega$  @  $V_{GS} = 10V$ .  
 $R_{DS(ON)} = 13m\Omega$  @  $V_{GS} = 4.5V$ .
- Super high dense cell design for extremely low  $R_{DS(ON)}$ .
- High power and current handling capability.
- Lead free product is acquired.
- TO-251 & TO-252 package.



### ABSOLUTE MAXIMUM RATINGS $T_C = 25^\circ C$ unless otherwise noted

Parameter	Symbol	Limit	Units
Drain-Source Voltage	$V_{DS}$	25	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D$	60	A
Drain Current-Pulsed <sup>a</sup>	$I_{DM}$	200	A
Maximum Power Dissipation @ $T_C = 25^\circ C$ - Derate above $25^\circ C$	$P_D$	56	W
		0.37	W/ $^\circ C$
Single Pulsed Avalanche Energy <sup>d</sup>	$E_{AS}$	60	mJ
Single Pulsed Avalanche Current <sup>d</sup>	$I_{AS}$	11	A
Operating and Store Temperature Range	$T_J, T_{stg}$	-55 to 175	$^\circ C$

### Thermal Characteristics

Parameter	Symbol	Limit	Units
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	2.7	$^\circ C/W$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	50	$^\circ C/W$



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## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	25			V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 25V, V_{GS} = 0V$			1	$\mu A$
Gate Body Leakage Current, Forward	$I_{GSSF}$	$V_{GS} = 20V, V_{DS} = 0V$			100	nA
Gate Body Leakage Current, Reverse	$I_{GSSR}$	$V_{GS} = -20V, V_{DS} = 0V$			-100	nA
<b>On Characteristics<sup>b</sup></b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = 250\mu A$	1		3	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 30A$		7	9	$m\Omega$
		$V_{GS} = 4.5V, I_D = 30A$		10	13	$m\Omega$
<b>Dynamic Characteristics<sup>c</sup></b>						
Forward Transconductance	$g_{FS}$	$V_{DS} = 10V, I_D = 15A$		12		S
Input Capacitance	$C_{iss}$	$V_{DS} = 15V, V_{GS} = 0V, f = 1.0\text{ MHz}$		1180		pF
Output Capacitance	$C_{oss}$			270		pF
Reverse Transfer Capacitance	$C_{rss}$			145		pF
<b>Switching Characteristics<sup>c</sup></b>						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15V, I_D = 1A, V_{GS} = 10V, R_{GEN} = 6\Omega$		12	25	ns
Turn-On Rise Time	$t_r$			4	10	ns
Turn-Off Delay Time	$t_{d(off)}$			32	65	ns
Turn-Off Fall Time	$t_f$	$V_{DS} = 15V, I_D = 20A, V_{GS} = 5V$		6	15	ns
Total Gate Charge	$Q_g$			10	13	nC
Gate-Source Charge	$Q_{gs}$			3.6		nC
Gate-Drain Charge	$Q_{gd}$			2.9		nC
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
Drain-Source Diode Forward Current	$I_S$				60	A
Drain-Source Diode Forward Voltage <sup>b</sup>	$V_{SD}$	$V_{GS} = 0V, I_S = 20A$		0.85	1.2	V
<b>Notes :</b> □ a.Repetitive Rating : Pulse width limited by maximum junction temperature b.Pulse Test : Pulse Width < 300 $\mu s$ , Duty Cycle < 2%. □ c.Guaranteed by design, not subject to production testing. □ d.L = 1mH, $I_{AS} = 11A, V_{DD} = 50V, R_G = 25\Omega$ , Starting $T_J = 25^\circ\text{C}$						



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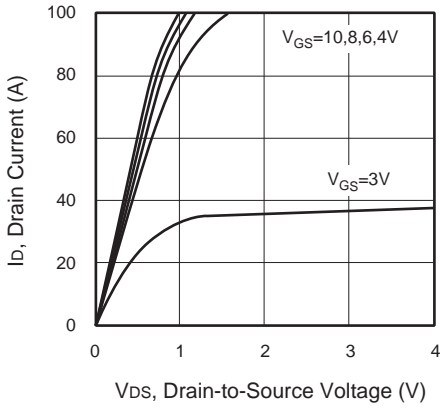


Figure 1. Output Characteristics

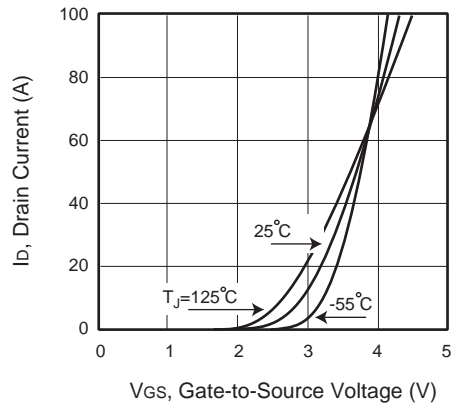


Figure 2. Transfer Characteristics

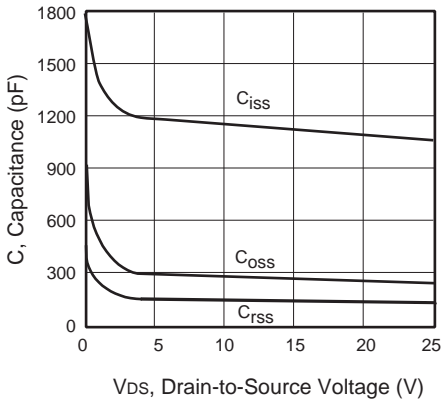


Figure 3. Capacitance

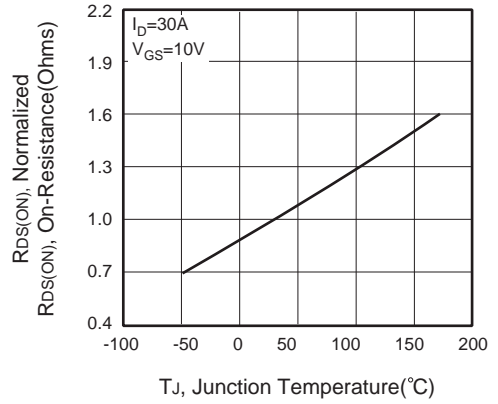


Figure 4. On-Resistance Variation with Temperature

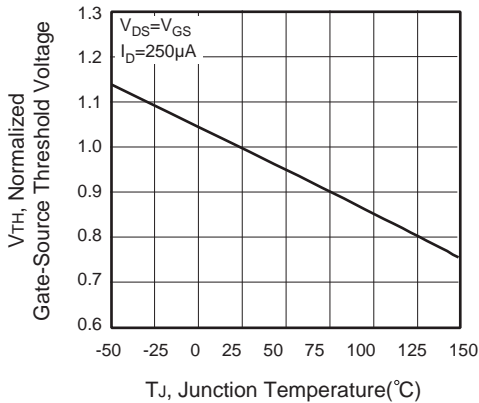


Figure 5. Gate Threshold Variation with Temperature

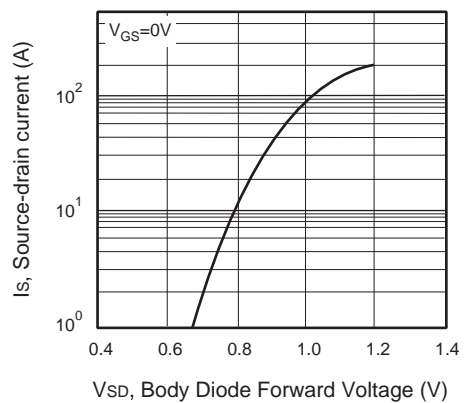


Figure 6. Body Diode Forward Voltage Variation with Source Current



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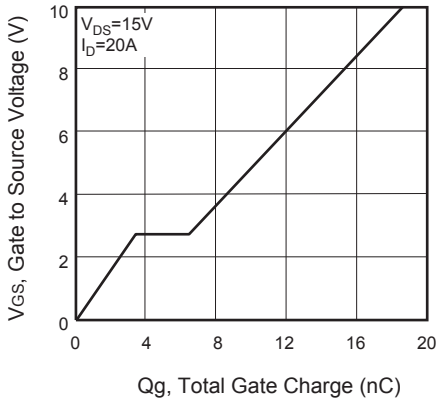


Figure 7. Gate Charge

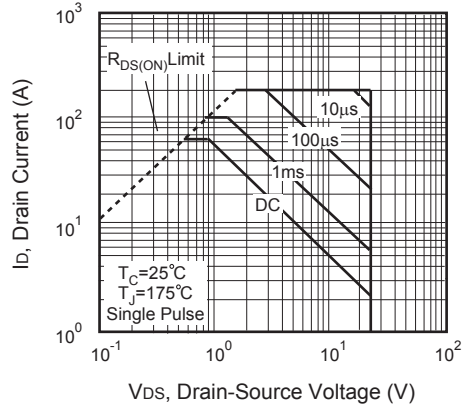


Figure 8. Maximum Safe Operating Area



Figure 9. Switching Test Circuit



Figure 10. Switching Waveforms

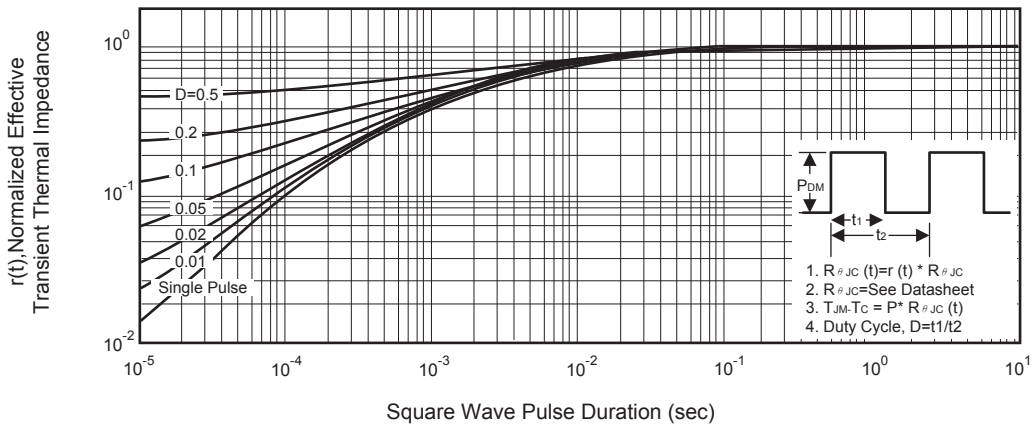


Figure 11. Normalized Thermal Transient Impedance Curve