SX8652

15kV ESD Low Power 4-Wire / 5-Wire Resistive Touchscreen Controller with SPI Interface

ADVANCED COMMUNICATIONS & SENSING DATASHEET

GENERAL DESCRIPTION

The SX8652 is a very low power, high reliability controller for 4-wire and 5-wire resistive touch screens used in PDAs, portable instruments and point-of-sales terminal applications. It features a wide input supply range from 1.65V to 3.7V and low power modes to preserve current when the screen is unintentionally touched.

To compute touch screen X-Y coordinates and touch pressure with precision, a low power 12-bit analog-digital converter is activated with the possibility to enable on-chip data averaging processing algorithms to reduce host activity and suppress system noise.

The touch screen controller inputs have been specially designed to provide robust on-chip ESD protection of up to ±15kV in both HBM and Contact Discharge, and eliminates the need for external protection devices. The SX8652 is controlled by a high speed SPI™ serial interface.

The SX8652 is available in a 4.0 mm x 3.0 mm 14-DFN package and a 1.5 mm x 2.0 mm wafer level chip scale package (WLCSP) for space conscience applications.

APPLICATIONS

- DSC, DVR, Cell Phones
- PDA, Pagers
- Point-of-Sales Terminals
- Touch-Screen Monitors

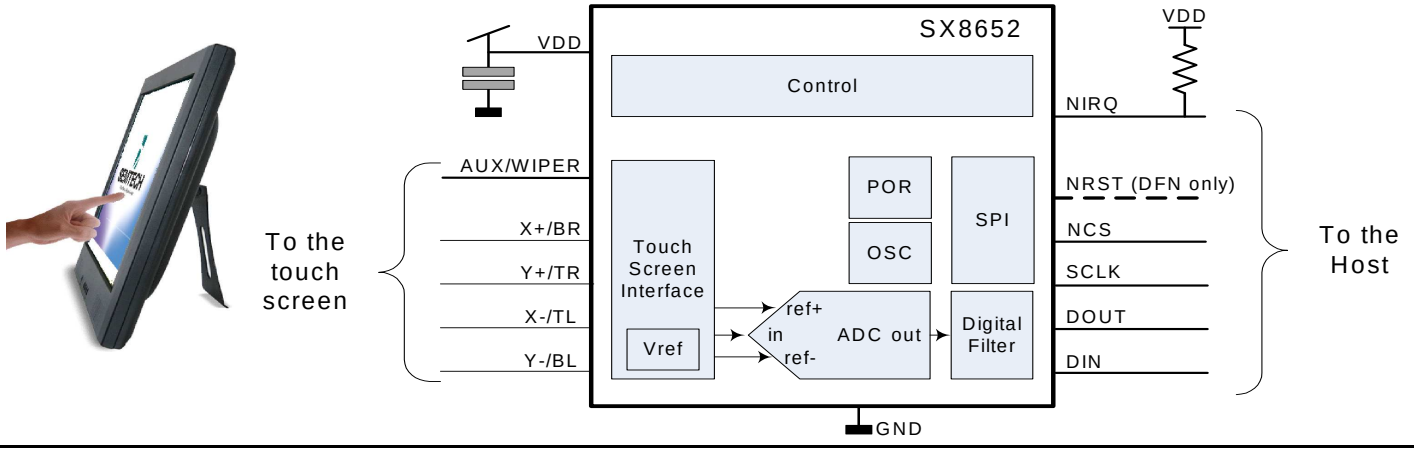
ORDERING INFORMATION

Part Number	Package (Dimension in mm)	Marking
SX8652ICSTRT[1]	12 - Ball WLCSP (1.5x2.0)	FG97
SX8652IWLTRT[1]	14 - Lead DFN (4.0x 3.0)	FG97

1. 3000 Units / reel

KEY PRODUCT FEATURES

- Extremely Low Power Consumption: 23uA@1.8V 8kSPS
- Superior On-chip ESD Protection
  - ➪±15kV HBM (X+,X-,Y+,Y-)
  - ➪±2kV CDM
  - ➪±25kV Air Gap Discharge
  - ➪±15kV Contact Discharge
  - ➪±300V MM
- Single 1.65V to 3.7V Supply/Reference
- 4-Wire or 5-Wire Resistive Touch Screen Interface
- Integrated Preprocessing Block to Reduce Host Loading and Bus Activity
- Four User Programmable Operation Modes provides Flexibility to address Different Application Needs
  - ➪Manual, Automatic, Pen Detect, Pen Trigger
- Low Noise Ratiometric Conversion
- Precision, High Speed 12-bit SAR ADC Operating At 74k SPS
- Throughput: 5000 (X-Y) coordinates/second (c/s) with 7-Sample Averaging
- Low Power Shut-Down Mode < 1uA
- SPI™ Serial Interface
- Touch Pressure Measurement (4-Wire)
- Auxiliary Input (4-Wire) For Alternate ADC Input or Start of Conversion Trigger
- Hardware & Software reset
- -40℃ to +85℃ operation
- Pb-Free, Halogen Free, RoHS/WEEE compliant product
- Windows CE 6.0, Linux Driver Support Available
- Packages: 14-LD (4.0 mm x 3.0 mm) DFN
  12-Ball (1.5 mm x 2.0 mm) WLCSP



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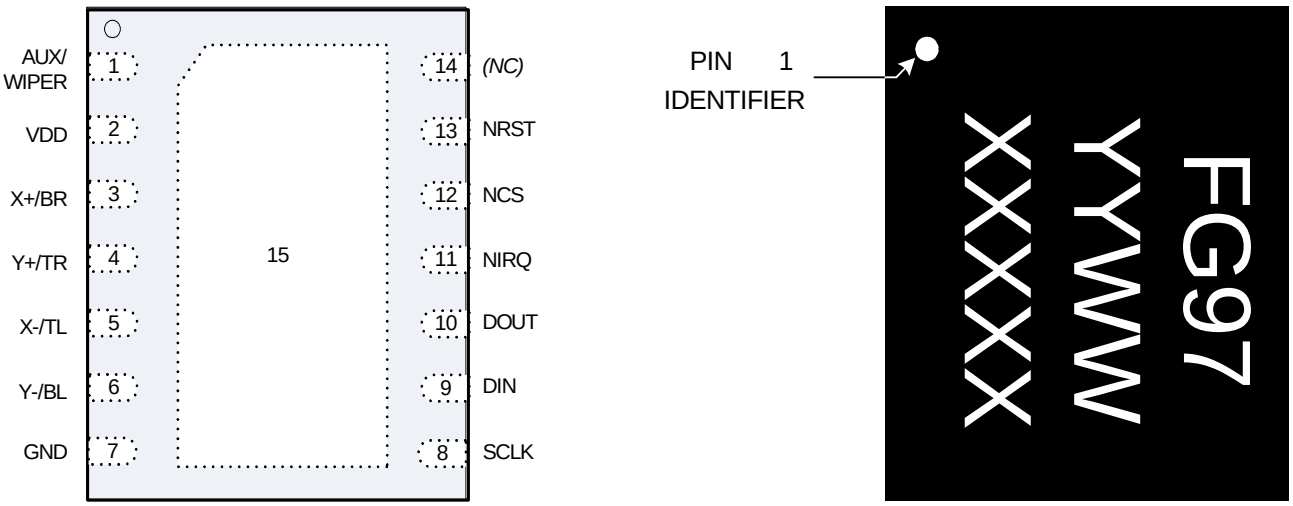


Figure 1. SX8652 DFN Top View, Pad on Bottom Side

YYWW: date code

XXXXX: Lot Number

1.2. WLCSP Pinout Diagram and Marking Information (Top View)

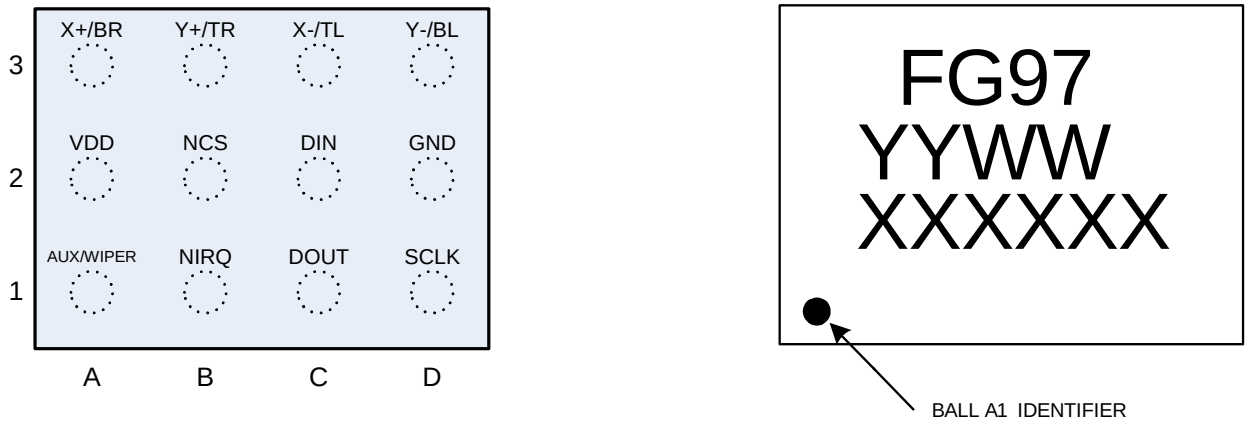


Figure 2. SX8652 WLCSP Top View, Solder Bumps on Bottom Side

YYWW: date code

XXXXX: Lot Number

1.3. Pin Description

Pin Number #		Name	Type	Description
DFN	WLCSP			
1	A1	AUX/WIPER	Digital Input / Analog Input	Conversion Synchronization (4-wire) or Analog Auxiliary Input (4-wire) / Wiper Input (5-wire)
2	A2	VDD	Power Input	Input power supply, connect to a 0.1uF capacitor to GND
3	A3	X+/BR	Analog IO	X+ Right electrode (4-wire) / Bottom Right (5-wire) channel
4	B3	Y+/TR	Analog IO	Y+ Top electrode (4-wire) /Top Right (5-wire) channel
5	C3	X-/TL	Analog IO	X- Left electrode (4-wire) /Top Left (5-wire) channel
6	D3	Y-/BL	Analog IO	Y- Bottom electrode (4-wire) /Bottom Left (5-wire) channel
7	D2	GND	Ground	Ground
8	D1	SCLK	Digital Input	SPI Serial Clock Input
9	C2	DIN	Digital Output	SPI Serial Data Input
10	C1	DOUT	Digital Output	SPI Serial Data Output
11	B1	NIRQ	Digital Output, open drain	Interrupt Request Output, Active low, Need external pullup
12	B2	NCS	Digital Input	SPI Chip Select Input, Active low
13	-	NRST	Digital Input	DFN package only, Reset Input, Active low, Internal pull-up resistor
14	-	(NC)		Not Connected
15	-	GND	Power input	Backside Ground

Table 1. Pin description

1.4. Simplified Block Diagram

The SX8652 simplified block diagram is shown in Figure 3.

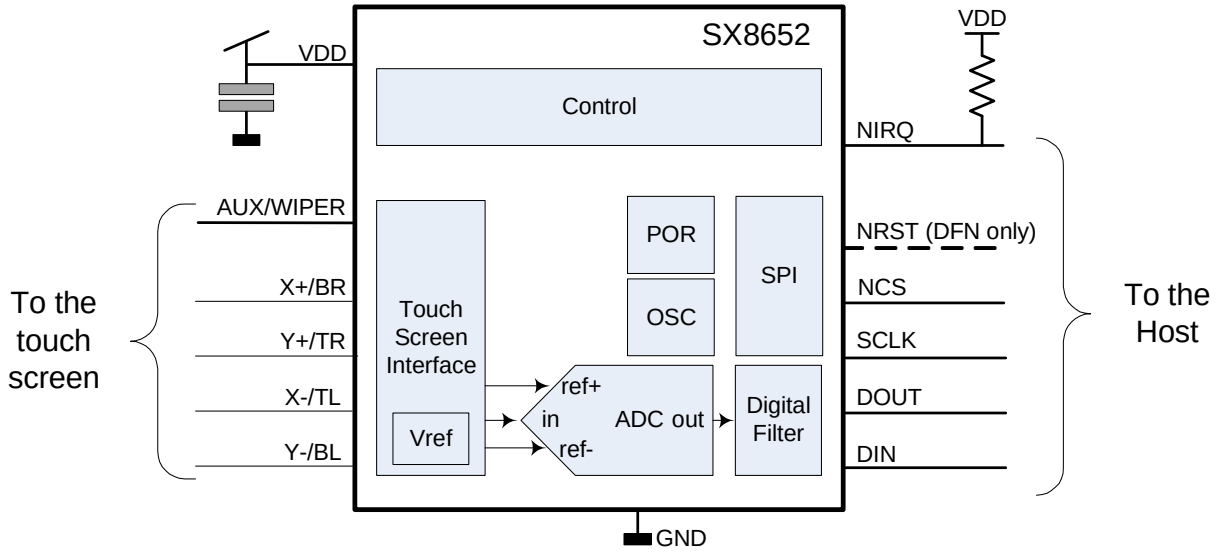


Figure 3. Simplified block diagram of the SX8652

2. Electrical Characteristics

2.1. Absolute Maximum Ratings

Stresses above the values listed in “Absolute Maximum Ratings” may cause permanent damage to the device.

This is a stress rating only and functional operation of the device at these, or any other conditions beyond the “Recommended Operating Conditions”, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameter		Symbol	Min.	Max.	Unit
Supply Voltage		V_{DDABS}	-0.5	3.9	V
Input voltage (non-supply pins)		V_{IN}	-0.5	3.9	V
Input current (non-supply pins)		I_{IN}		10	mA
Operating Junction Temperature		T_{JCT}		125	℃
Reflow temperature		T_{RE}		260	℃
Storage temperature		T_{STOR}	-50	150	℃
ESD HBM (Human Body Model)	High ESD pins: X+/BR, X-/TL, Y+/TR, Y-/BL, Aux/Wiper	ESD_{HBM1}	± 15(i)		kV
			± 8(ii)		kV
	All pins except high ESD pins	ESD_{HBM2}	± 2		kV
ESD (Contact Discharge)	High ESD pins: X+/BR, X-/TL, Y+/TR, Y-/BL, Aux/Wiper	ESD_{CD}	± 15		kV
Latchup(iii)		I_{LU}	± 100		mA

Table 2. Absolute Maximum Ratings

(i) Tested to TLP (10A)

(ii) Tested to JEDEC standard JESD22-A114

(iii) Tested to JEDEC standard JESD78

2.2. Recommended Operating Conditions

Parameter	Symbol	Min.	Max	Unit
Supply Voltage	V_{DD}	1.65V	3.7	V
Ambient Temperature Range	T_A	-40	85	℃

Table 3. Recommended Operating Conditions

2.3. Thermal Characteristics

Parameter	Symbol	Min.	Max	Unit
Thermal Resistance with DFN package - Junction to Ambient (iii)	θ_{JA}		39	℃/W
Thermal Resistance with WLCSP package - Junction to Ambient (iii)	θ_{JA}		65	℃/W

Table 4. Thermal Characteristics

(iii) θ_{JA} is calculated from a package in still air, mounted to 3" x 4.5", 4 layer FR4 PCB with thermal vias under exposed pad (if applicable) per JESD51 standards.

2.4. Electrical Specifications

All values are valid within the recommended operating conditions unless otherwise specified.

Parameter	Symbol	Conditions	Min.	Typ	Max	Unit
Current consumption						
Mode = MANUAL	I_{pwd}	Converter stopped, pen detection off, SPI listening, OSC stopped		0.4	1	uA
Mode = PENDET	I_{pndt}	Converter stopped, pen detection activated, device generates interrupt upon detection, SPI listening, OSC stopped		0.4	1	uA
Mode =PENTRIG	I_{pntr}	Converter stopped, pen detection activated, device starts conversion upon pen detection. SPI listening, OSC stopped		0.4	1	uA
Mode=AUTO	I_{auto}	Converter stopped, pen detection off, SPI listening, OSC on, timer on		1.5		uA
Operation @8kSPS, VDD=1.8V	I_{opl}			23	50	uA
Operation @42kSPS, VDD=3.3V	I_{oph}			105	140	uA
Digital I/O						
High-level input voltage	V_{IH}		$0.8V_{DD}$		V_{DD}+0.2	V
Low-level input voltage	V_{IL}		V_{SS}-0.3		$0.2V_{DD}$	V
Hysteresis	V_{HysLow}	VDD > 2V		0.05 V_{DD}		V
	$V_{HysHigh}$	VDD < 2V		0.1 V_{DD}		V
Output Logic High	V_{OH}	I_{OL}<-4mA	$0.8V_{DD}$			
Output Logic Low	V_{OL}	I_{OL}<4mA	0		0.4	V
Input leakage current	L_I	CMOS input			±1	uA
High ESD Input - Output capacitance	$C_{X+/BR}$,$C_{X-/TL}$,$C_{Y+/TR}$, $C_{Y-/BL}$, C_{AUX}			50		pF
Input - Output capacitance	C_{NRST} , C_{NIRQ} ,C_{NCS} ,C_{DIN} , C_{DOUT}, C_{SCLK}			5		pF

Table 5. Electrical Specifications

Parameter	Symbol	Conditions	Min.	Typ	Max	Unit
Startup						
Power-up time	t_{por}	Time between rising edge VDD and rising NIRQ			1	ms
ADC						
Resolution	A_{res}		12			bits
Offset	A_{off}			±1		LSB
Gain error	A_{ge}	At full scale		0.5		LSB
Differential Non Linearity	A_{dnl}			±1		LSB
Integral Non Linearity	A_{inl}			±1.5		LSB
Resistors						
X+, X-, Y+, Y- resistance	R_{chn}	Touch Pad Biasing Resistance		5		Ohm
Pen detect resistance	R_{PNDT_00}	R_{PNDT} = 0		100		kOhm
	R_{PNDT_01}	R_{PNDT} = 1		200		kOhm
	R_{PNDT_10}	R_{PNDT} = 2		50		kOhm
	R_{PNDT_11}	R_{PNDT} = 3		25		kOhm
External components		**recommendations**				
Capacitor between VDD, GND	C_{vdd}	Type 0402, tolerance +/-50%		0.1		uF

Table 5. Electrical Specifications

2.5. Host Interface Specifications

Parameter	Symbol	Condition	Min	Typ	Max	Unit
SPI TIMING SPECIFICATIONS (i)						
SCLK Clock Frequency Duty Cycle	f_{SCLK} duty		 40		5000 60	kHz %
NCS edge to first SCLK "↑"	T_{CSS}		50			ns
NCS edge to DOUT Low	T_{DCD}				100	
SCLK High Pulse Width	T_{CKH}		80			
SCLK Low Pulse Width	T_{CKL}		80			
Data Setup Time	T_{DS}		40			
Data Valid to SCLK Hold Time	T_{DH}		70			
Data Output Delay after SCLK "↓"	T_{DOD}				70	
NCS "↑" to SCLK Ignored	T_{CSI}		50			
NCS "↑" to DOUT Hi-Z state	T_{CCZ}				90	
NCS Hold Time	T_{CSW}		150			

Table 6. Host Interface Specifications

(i) All timing specifications refer to voltage levels (50% VDD, V_{OH}, V_{OL}) defined in Table 6 unless otherwise mentioned.

2.6. Host Interface Timing Waveforms

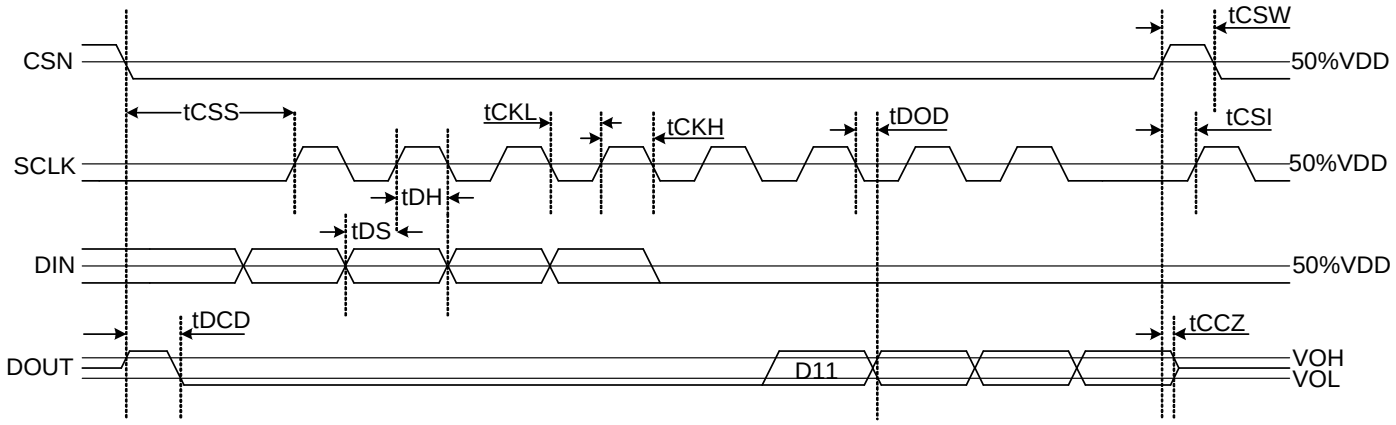


Figure 4. SPI Timing Waveform

3. Functional Description

3.1. General Introduction

This section provides an overview of the SX8652 architecture, device pinout and a typical application.

The SX8652 is designed for 4-wire and 5-wire resistive touch screen applications. The touch screen or touch panel is the resistive sensor and can be activated by either a finger or stylus.

As shown in Figure 5 with a 4-wire panel, the touch screen coordinates and touch pressure are converted into SPI format by the SX8652 for transfer to the host. The auxiliary input can be used to convert with 12-bit resolution any analog input in the supply range. It can also serves as an external synchronisation input to trig the touchscreen acquisition as described in the Application Information section.

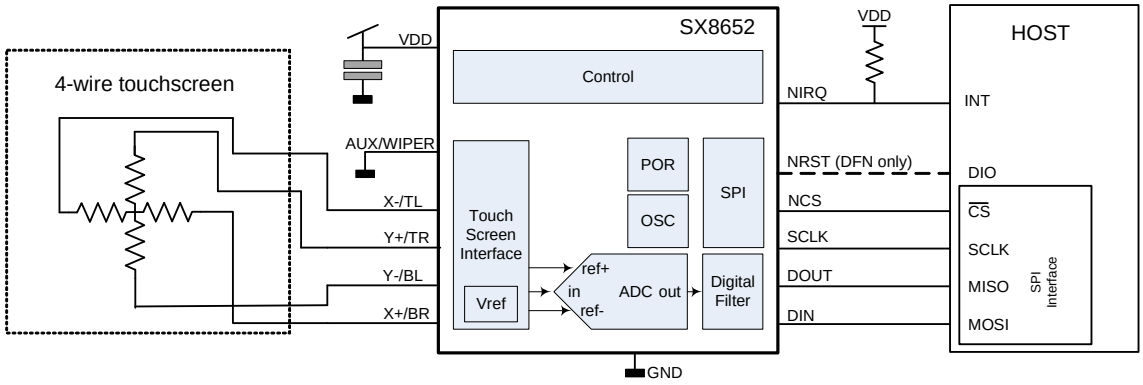


Figure 5. SX8652 with a 4-wire touch screen

A 5-wire touchscreen application is shown in Figure 6. In this application, the touch pressure can not be calculated.

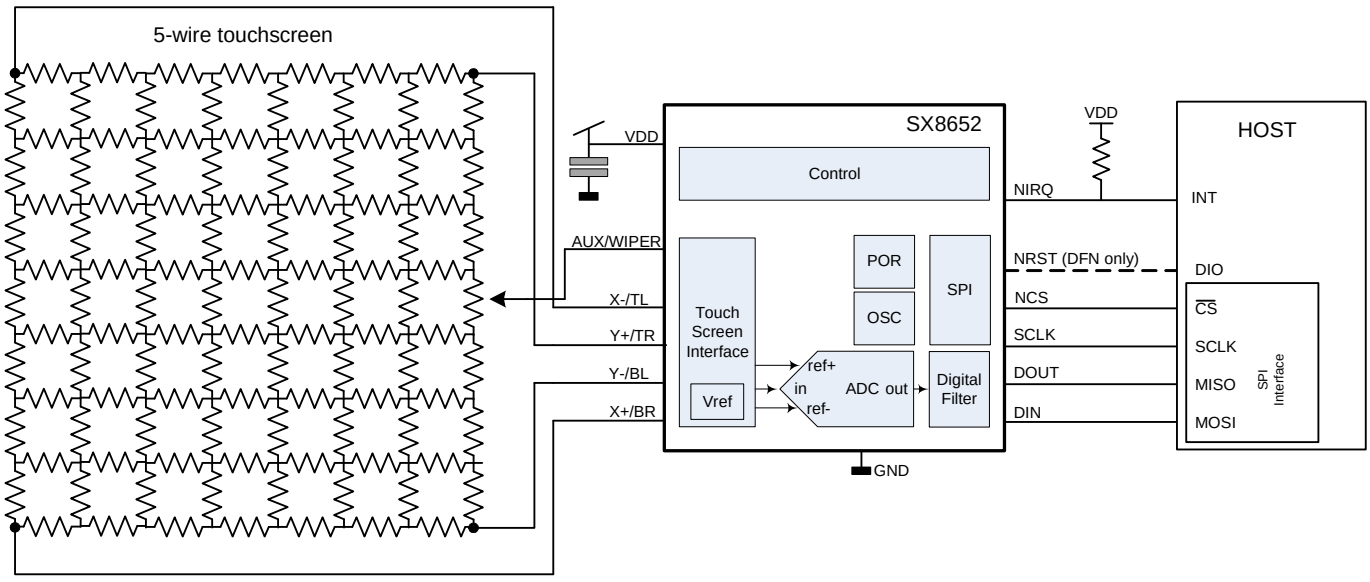
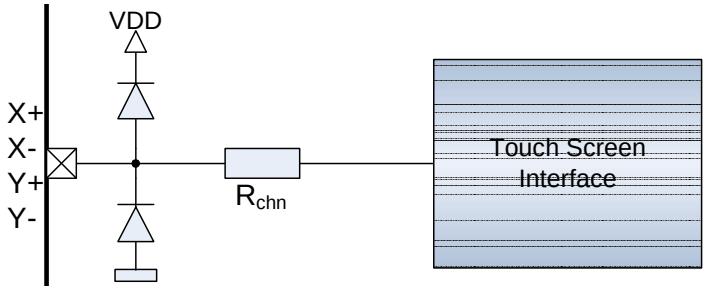


Figure 6. SX8652 with a 5-wire touch screen

3.2. Channel Pins

3.2.1. X+/BR, X-/TL, Y+/TR. Y-/BL



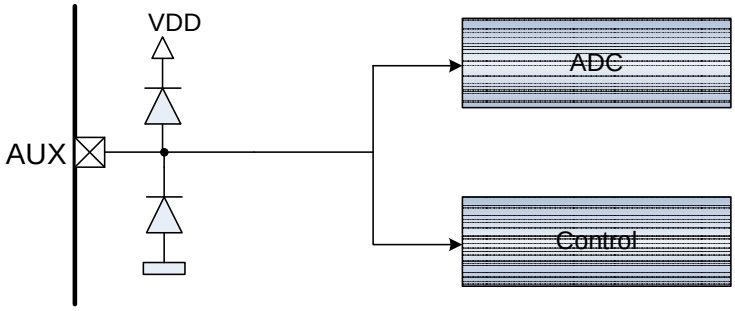
The SX8652's channel pins directly connect to standard touch screen X and Y resistive layers. The SX8652 separately biases each of these layers and converts the resistive values into (X,Y) coordinates.

The channel pins are protected to VDD and GROUND.

Figure 7 shows the simplified diagram of the X+, X-, Y+, Y- pins.

Figure 7. Simplified diagram of touchscreen pins

3.2.2. AUX/WIPER



The AUX/WIPER has 2 functions.

With 4-wire touchscreen, it is a single ended input for the 12 bit ADC with an input range from GND to VDD.

It can also be used to start the channel acquisition.

With 5-wire touchscreen, it is the sense channel of the touchpanel.

The AUX/WIPER pin is protected to VDD and GROUND.

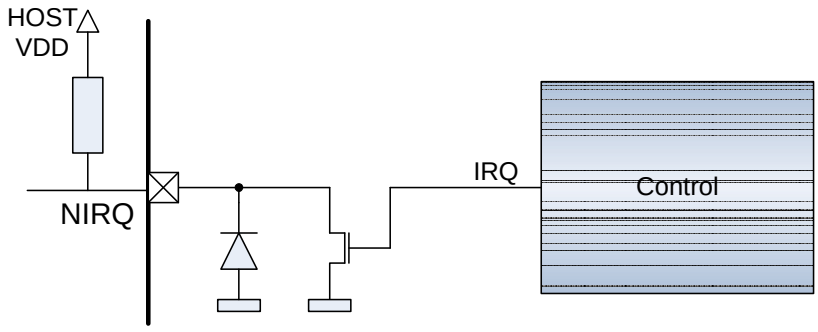
Figure 8 shows a simplified diagram of this pin.

Figure 8. Simplified diagram of AUX/WIPER pin

3.3. Host Interface and Control Pins

The SX8652 host and control interface consists of the SPI interface with NIRQ and NRST.

3.3.1. NIRQ

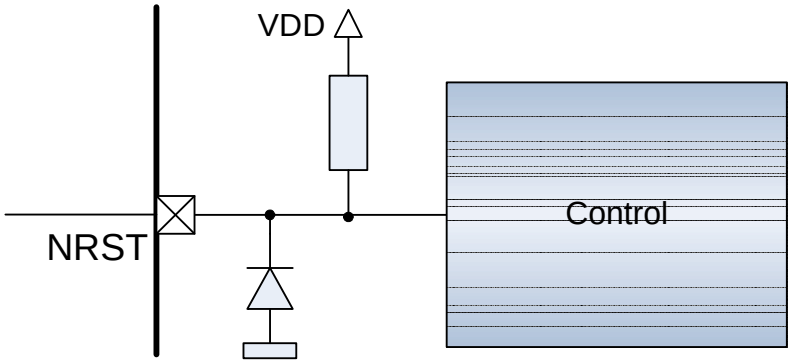


The NIRQ pin is an active low, open drain output to facilitate interfacing to different supply voltages and thus requires an external pull-up resistor (1-10 kOhm). NIRQ provides an interrupt to the host processor when a pen is detected, or when channel data is available.

As shown in Figure 9, the NIRQ pin does not have protection to VDD.

Figure 9. Simplified diagram of NIRQ

3.3.2. NRST



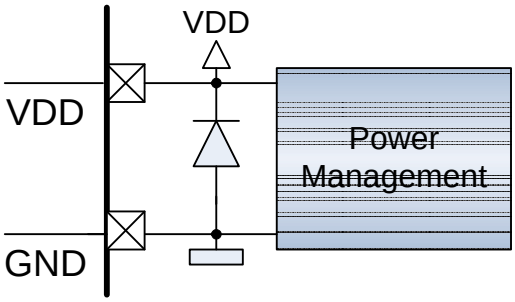
The NRST pin is an active low input that provides a hardware reset of the SX8652's control circuitry.

The NRST pin is protected to GROUND and have an internal pull-up to enable interfacing with devices at different supply voltages.

Figure 10 shows a simplified diagram of the NRST pin.

Figure 10. Simplified diagram of NRST

3.4. Power Management Pins



VDD and GND are power pins.

The VDD has ESD protection to GROUND.

The GND has ESD protection to VDD.

Figure 11 shows a simplified diagram of the VDD pin.

Figure 11. Simplified diagram of VDD and GND

4. 4-wire Touch Screen Detailed Description

4.1. Touch Screen Operation

A 4-wire resistive touch screen consists of two (resistive) conductive sheets separated by an insulator when not pressed. Each sheet is connected through 2 electrodes at the border of the sheet (Figure 12). When a pressure is applied on the top sheet, a connection with the lower sheet is established. Figure 13 shows how the Y coordinate can be measured. The electrode plates are connected through terminals X+, X- and Y+, Y- to an analog to digital converter (ADC) and a reference voltage. The resistance between the terminals X+ and X- is defined by Rxtot. Rxtot will be split in 2 resistors, R1 and R2, in case the screen is touched. The resistance between the terminals Y+ and Y- is represented by R3 and R4. The connection between the top and bottom sheet is represented by the touch resistance (R_T).

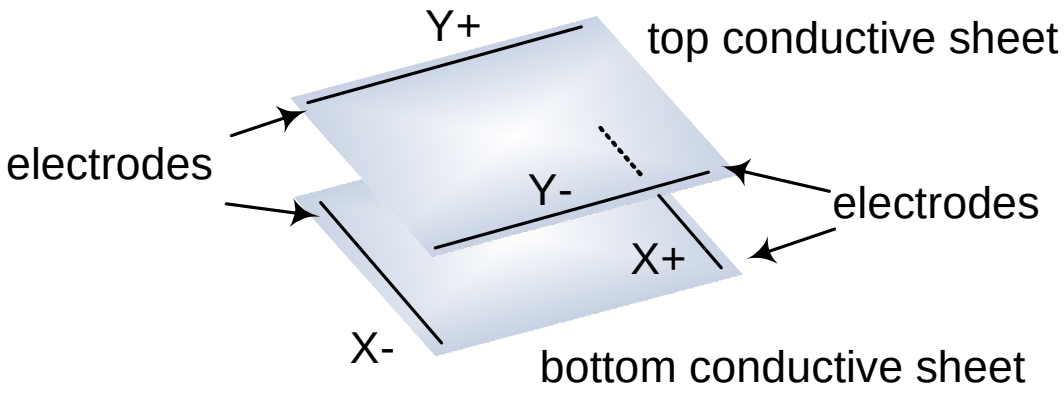


Figure 12. 4-wire Touch Screen

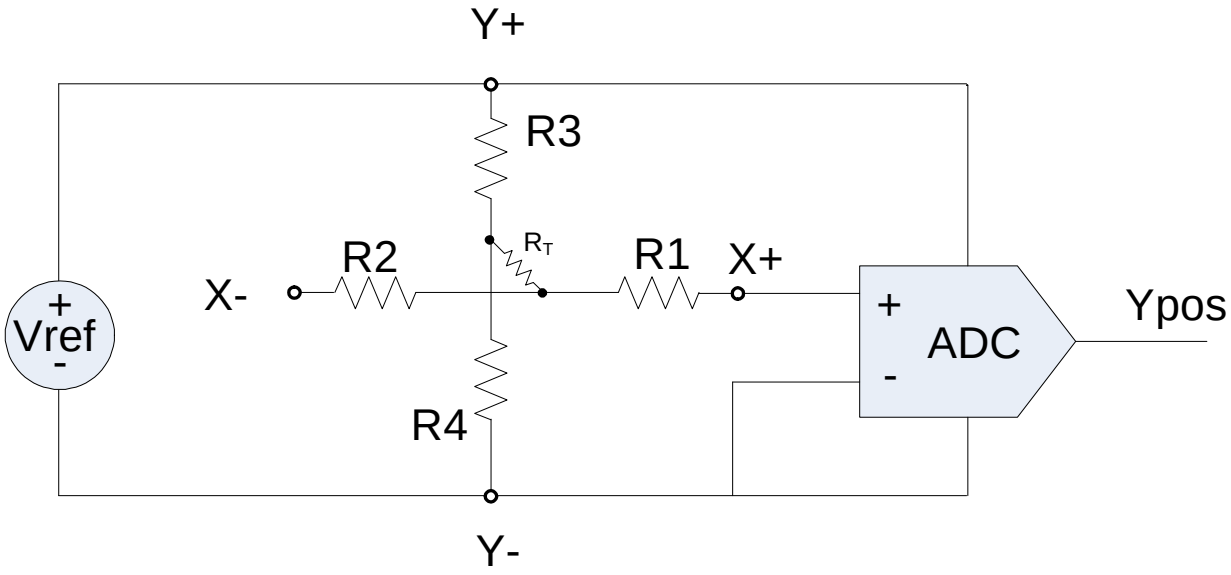


Figure 13. Touch Screen Operation ordinate measurement (Y)

4.2. Coordinates Measurement

The top resistive sheet (Y) is biased with a voltage source. Resistors R3 and R4 determine a voltage divider proportional to the Y position of the contact point. Since the converter has a high input impedance, no current flows through R1 so that the voltage X+ at the converter input is given by the voltage divider created by R3 and R4.

The X coordinate is measured in a similar fashion with the bottom resistive sheet (X) biased to create a voltage divider by R1 and R2, while the voltage on the top sheet is measured through R3. Figure 14 shows the coordinates measurement setup. The resistance R_T is the resistance obtained when a pressure is applied on the screen. R_T is created by the contact area of the X and Y resistive sheet and varies with the applied pressure.

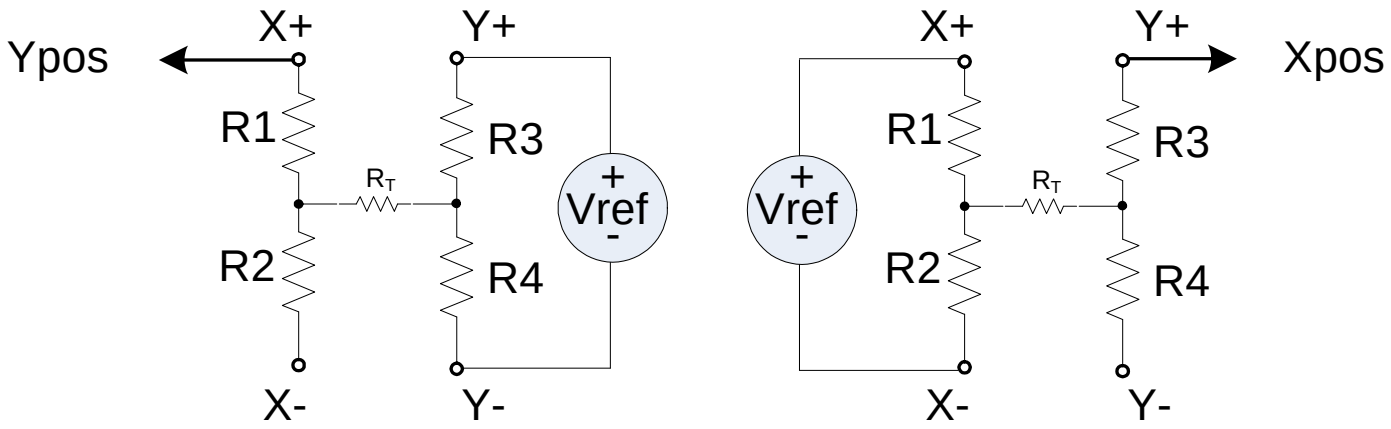


Figure 14. Ordinate (Y) and abscissa (X) coordinates measurement setup

The X and Y position are found by: $Xpos = 4095 \cdot \frac{R2}{R1 + R2}$ $Ypos = 4095 \cdot \frac{R4}{R3 + R4}$

4.3. Pressure Measurement

The pressure measurement consists of two additional setups: z1 and z2 (see Figure 15).

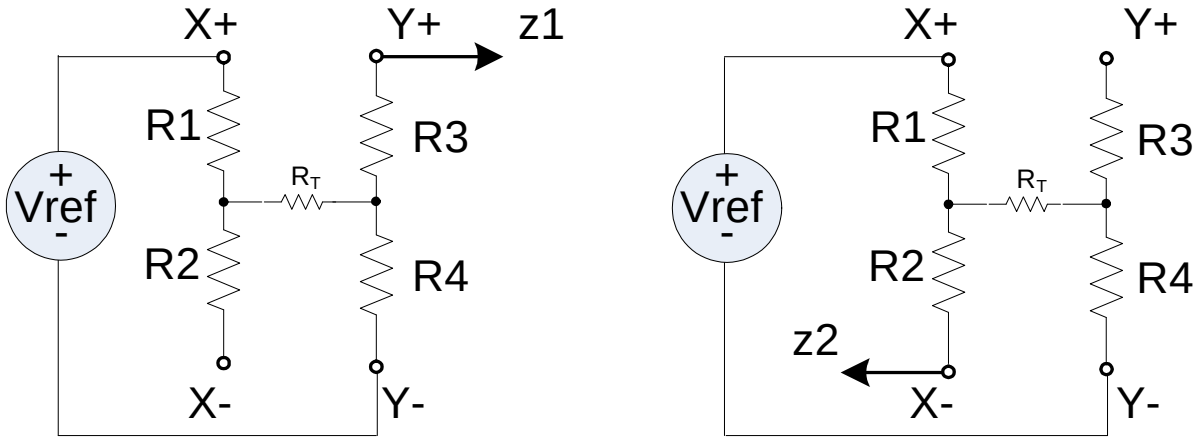


Figure 15. z1 and z2 pressure measurement setup

The corresponding equations for the pressure: $z1 = 4095 \cdot \frac{R4}{R1 + R4 + R_T}$ $z2 = 4095 \cdot \frac{R4 + Rt}{R1 + R4 + R_T}$

The X and Y total sheet resistance (Rxtot, Rytot) are known from the touch screen supplier.

$$Rxtot = R1 + R2$$

R4 is proportional to the Y coordinate.

$$Rytot = R3 + R4$$

The R4 value is given by the total Y plate resistance multiplied by the fraction of the Y position over the full coordinate range.

$$R4 = Rytot \cdot \frac{Ypos}{4095}$$

By re-arranging z1 and z2 one obtains

$$R_T = R4 \cdot \left[\frac{z2}{z1} - 1\right]$$

Which results in:

$$R_T = Rytot \cdot \frac{Ypos}{4095} \cdot \left[\frac{z2}{z1} - 1\right]$$

The touch resistance calculation above requires three channel measurements (Ypos, z2 and z1) and one specification data (Rytot).An alternative calculation method is using Xpos, Ypos, one z channel and both Rxtot and Rytot shown in the next calculations

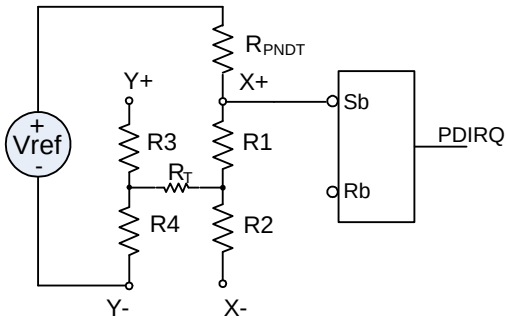
R1 is inverse proportional to the X coordinate.

$$R1 = Rxtot \cdot \left[1 - \frac{Xpos}{4095}\right]$$

Substituting R1 and R4 into z1 and rearranging terms gives:

$$R_T = \frac{Rytot \cdot Ypos}{4095} \cdot \left[\frac{4095}{z1} - 1\right] - Rxtot \cdot \left[1 - \frac{Xpos}{4095}\right]$$

4.4. Pen Detection



The pen detection circuitry is used both to detect a user action and generate an interrupt or start an acquisition in PENDET and PENTRG mode respectively. Doing a pen detection prior to conversion avoids feeding the host with dummy data and saves power.

If the touchscreen is powered between X+ and Y- through a resistor R_{PNDT}, no current will flow so long as pressure is not applied to the surface (see Figure 16). When some pressure is applied, a current path is created and brings X+ to the level defined by the resistive divider determined by R_{PNDT} and the sum of R1, R_T and R4. Due to the capacitive loading of the touchscreen, the bias delay is of 0.25 x POWDLY.

Figure 16. Pen detection

The resistor R_{PNDT} can be configured to 4 different values (see Table 13) to accommodate different screen resistive values.

R_{PNDT} should be set to a value greater than 7x(Rxtot + Rytot).

The pen detection will set the PENIRQ bit of the RegStat register.

In PENDET mode, the pen detection will set NIRQ low. The PENIRQ bit will be cleared and the NIRQ will be de-asserted as soon as the host reads the status register.

5. 5-wire Touch Screen Detailed Description

5.1. Touch Screen Operation

A 5-wire resistive touch screen consists of two (resistive) conductive sheets separated by an insulator when not pressed.

4 wires are connected on the 4 corners of the bottom conductive sheet. They are referred as Top Left, Top Right, Bottom Left, Bottom Right.

The fifth wire is used for sensing the electrode voltage and is referred as the wiper. It is embedded in the top sheet.

Higher reliability and better endurance are the advantages of 5-wire touchscreen.

On the other hand, 5-wire touchscreen does not permit pressure measurement.

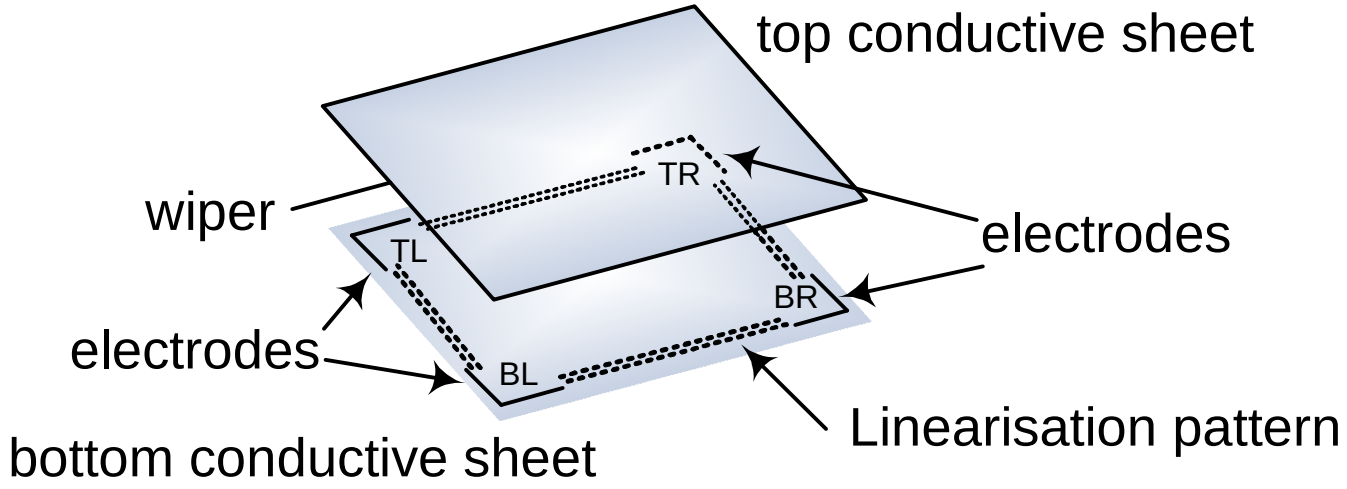


Figure 17. 5-wire touchscreen

5.2. Coordinates Measurement

The top resistive sheet is biased with a voltage source. Resistors R3 and R4 determine a voltage divider proportional to the Y position of the contact point. Since the converter has a high input impedance, no current flows through R1 so that the voltage X+ at the converter input is given by the voltage divider created by R3 and R4.

The X coordinate is measured in a similar fashion with the bottom resistive sheet biased to create a voltage divider by R1 and R2, while the voltage on the top sheet is measured through R3. Figure 18 shows the coordinates measurement setup.

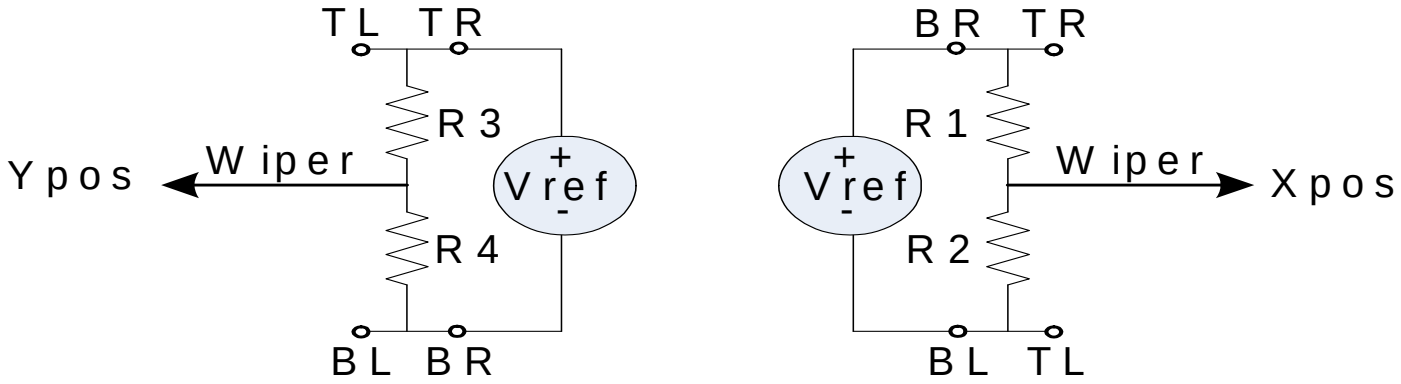


Figure 18. Ordinate (Y) and abscissa (X) coordinates measurement setup

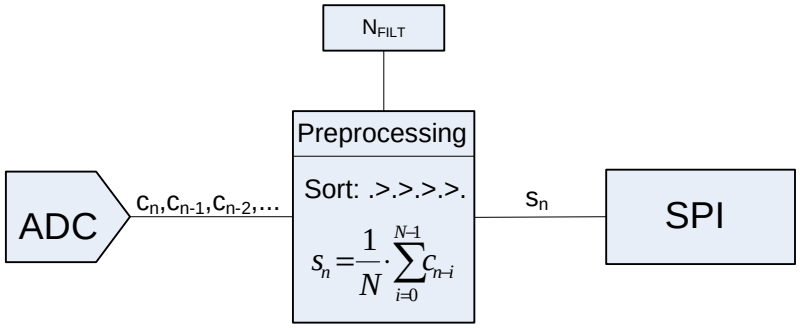
The X and Y position are found by: $Xpos = 4095 \cdot \frac{R2}{R1 + R2}$ $Ypos = 4095 \cdot \frac{R4}{R3 + R4}$

5.3. Pen Detection

The pendetect pull-up resistor and detector continue to monitor the X+/BR pin as in 4-wire mode. The wiper panel is grounded at the AUX_WIPER pin to provide the grounding path for a screen touch event.

If a pressure is applied to the surface, a current path is created and will bias the touchscreen between BR and the wiper probe.

6. Data Processing



The SX8652 offers 4 types of data processing which allows the user to make trade-offs between data throughput, power consumption and noise rejection.

The parameter FILT is used to select the filter order N_{filt} as seen in Table 7. The noise rejection will be improved with a high order to the detriment of the power consumption.

Figure 19. Filter structure

.

FILT	N_{filt}	Processing
0	1	$s_n = c_n$ No average.
1	3	$= \frac{1}{3} \cdot \frac{4079}{4095}(c_n + c_{n-1} + c_{n-2})$ 3 ADC samples are averaged
2	5	$= \frac{1}{5} \cdot \frac{4079}{4095}(c_n + c_{n-1} + c_{n-2} + c_{n-3} + c_{n-4})$ 5 ADC samples are averaged
3	7	$c_{max1} \geq c_{max2} \geq c_a \geq c_b \geq c_c \geq c_{min1} \geq c_{min2}$ $= \frac{1}{3} \cdot \frac{4079}{4095}(c_a + c_b + c_c)$ 7 ADC samples are sorted and the 3 center samples are averaged

Table 7. Filter order

6.1. Host Interface and Control

The host interface consists of SPI (DIN, DOUT, SCLK, NCS) and the NIRQ, NRST signals.

The SPI implemented on the SX8652 is set to the common setting CPOL=0 and CPHA=0.

It means data are sampled on the rising edge of the clock, and shifted on the falling one. The default state of the clock when NCS gets asserted is low.

If a host send a command while the system is busy, the command is discarded.

The supported SPI access formats are described in the next sections:

- Read/Write Registers
- Read Channels Data
- Host Commands

6.1.1. SPI Read/Write Registers

The host can write to and read from registers of the SX8652 by the write and read commands as defined in Table 8.

W/R command name	CR(7:0)								Function
	7	6	5	4	3	2	1	0	
WRITE(RA)	0	0	0	RA(4:0)					Write register (see Table 12 for RA)
READ(RA)	0	1	0	RA(4:0)					Read register (see Table 12 for RA)

Table 8. W/R commands

With the WRITE command, the host can write a single or multiple registers in the SX8652 register. This command is generated by setting the CMD(7:5) bits to write command (000). The register address is latched after the address is received and used for the first write.

With the READ command the host can read a single or multiple registers in the SX8652 register file. The frame starts by issuing a write command indicating the address of the first register to be read and the data are put on the DOUT line.

6.1.2. SPI Reading Channel Data

W/R command name	CR(7:0)								Function
	7	6	5	4	3	2	1	0	
READCHAN	0	0	1	x	x	x	x	x	Read Channel Data

Table 9. Read Channels Data

The data read process is the same as the register read process, but with a different command. Channel data are stored in a FIFO stack with the order: First: X,Y, Z1, Z2, Last: AUX. It is not possible to read two times the same coordinate. When the channel data buffer gets empty, the data will carry an invalid data as explained in the channel data format.

For example, if the value 0xC0 is set in RegChanMsk (X and Y conversion), the first READCHAN command will read X value, the second will read Y value and the third one will get invalid data.

The channel data D(11:0) is of unsigned format and corresponds to a value between 0 and 4095.

This is send on 2 bytes of 8 bits. A mask with the value 0x0FFF (4095) must be done to get correct values.

6.1.3. Multiple Read/Write

The SPI protocol is designed to be able to do multiple read/write during a transaction. During one single operation, as long as NCS stay asserted, the register address is automatically increased to allow sequential read/write (or sequential retrieval of data). Between each different operation though (READ/WRITE/READCHAN), the communication should be restarted.

This is described in Figure 20.

6.1.4. SPI Host Commands

.The host can issue commands to change the operation mode or perform manual actions as defined in Table 10.

command name	CR(7:0)								Function
	7	6	5	4	3	2	1	0	
SELECT(CHAN)	1	0	0	0	x	CHAN(2:0)			Bias channel (see Table 11 for CHAN)
CONVERT(CHAN)	1	0	0	1	x	CHAN(2:0)			Bias channel (see Table 11 for CHAN) Wait POWDLY settling time Run conversion
MANAUTO	1	0	1	1	x	x	x	x	Enter manual or automatic mode.
PENDET	1	1	0	0	x	x	x	x	Enter pen detect mode.
PENTRG	1	1	1	0	x	x	x	x	Enter pen trigger mode.

Table 10. Host Commands

The channels are defined in Table 11

.

Channel	CHAN(2:0)			Function
	2	1	0	
X	0	0	0	X channel
Y	0	0	1	Y channel
Z1	0	1	0	First channel for pressure measurement
Z2	0	1	1	Second channel for pressure measurement
AUX	1	0	0	Auxiliary channel
reserved	1	0	1	
reserved	1	1	0	
SEQ	1	1	1	Channel sequentially selected from RegChanMsk register, (see Table 13)

Table 11. Channel definition

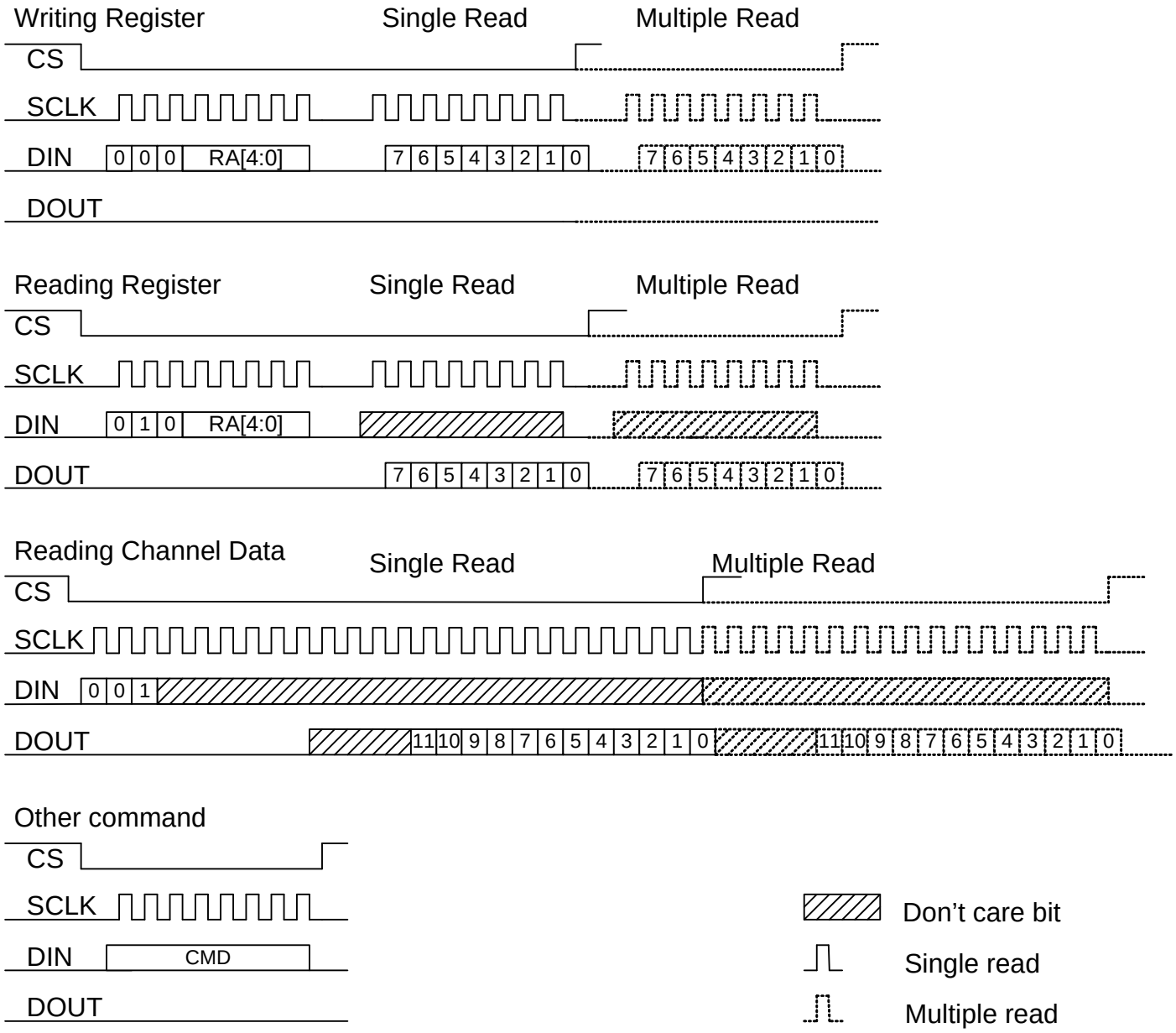


Figure 20. Data channel format

6.1.5. Invalid Qualified Data

The SX8652 will return 0xFFFF data in case of invalid qualified data.

This occurs:

- When the SX8652 has read all the channel data in the FIFO
- When a conversion is done without a pen being detected.

6.2. Register Map

Register Address RA(4:0)	Register	Description
0 0000	RegCtrl0	Write, Read
0 0001	RegCtrl1	Write, Read
0 0010	RegCtrl2	Write, Read
0 0100	RegChanMsk	Write, Read
0 0101	RegStat	Read
1 1111	RegSoftReset	Write

Table 12. Register address

The details of the registers are described in the next sections.

6.3. Host Control Writing

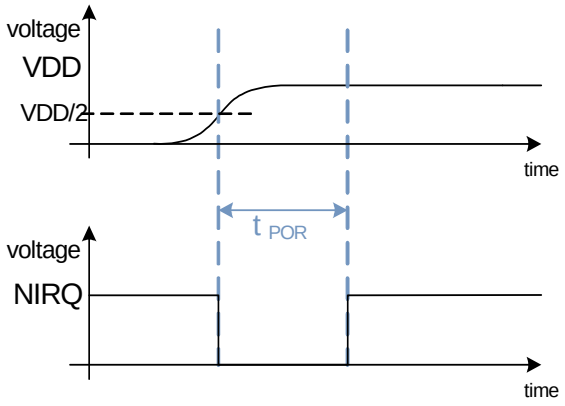
Register	Bits	Default	Description		
RegCtrl0	7:4	0000	RATE	Set rate in coordinates per sec (cps) (± 20%) If RATE equals zero then Manual mode. if RATE is larger than zero then Automatic mode	
				0000: Timer disabled -Manual mode 0001: 10 cps 0010: 20 cps 0011: 40 cps 0100: 60 cps 0101: 80 cps 0110: 100 cps 0111: 200 cps	1000: 300 cps 1001: 400 cps 1010: 500 cps 1011: 1k cps 1100: 2k cps 1101: 3k cps 1110: 4k cps 1111: 5k cps
	3:0	0000	POWDLY	Settling time (± 10%): The channel will be biased for a time of POWDLY before each channel conversion	
				0000: Immediate (0.5 us) 0001: 1.1 us 0010: 2.2 us 0011: 4.4 us 0100: 8.9 us 0101: 17.8 us 0110: 35.5 us 0111: 71.0 us	1000: 0.14 ms 1001: 0.28 ms 1010: 0.57 ms 1011: 1.14 ms 1100: 2.27 ms 1101: 4.55 ms 1110: 9.09 ms 1111: 18.19 ms
RegCtrl1	7:6	00	AUXAQC	00: AUX is used as an analog input (4-wire only) 01: On rising AUX edge, wait POWDLY and start acquisition	10: On falling AUX edge, wait POWDLY and start acquisition 11: On rising and falling AUX edges, wait POWDLY and start acquisition
				The AUX trigger works only in manual mode with 4-wire touchscreen	
	5	1	CONDIRQ	Enable conditional interrupts 0: interrupt always generated at end of conversion cycle. If no pen is detected the data is set to 'invalid qualified'. 1: interrupt generated when pen detect is successful	
	4	0	SCREEN	Select the type of screen: 0: 4-wire 1: 5 -wire	
	3:2	00	RPDNT	Select the Pen Detect Resistor 00: 100 kOhm 01: 200 kOhm 10: 50 kOhm 11: 25 kOhm	
	1:0	00	FILT	Digital filter control 00: Disable 01: 3 sample averaging 10: 5 sample averaging 11: 7 sample acquisition, sort, average 3 middle samples	

Table 13. SX8652 Register

Register	Bits	Default	Description		
RegCtrl2	7:4	0	reserved		
	3:0	0000	SETDLY	Settling time while filtering (± 10%) When filtering is enabled, the channel will initially bias for a time of POWDLY for the first conversion, and for a time of SETDLY for each subsequent conversion in a filter set.	
				0000: Immediate (0.5 us) 0001: 1.1 us 0010: 2.2 us 0011: 4.4 us 0100: 8.9 us 0101: 17.8 us 0110: 35.5 us 0111: 71.0 us	1000: 0.14 ms 1001: 0.28 ms 1010: 0.57 ms 1011: 1.14 ms 1100: 2.27 ms 1101: 4.55 ms 1110: 9.09 ms 1111: 18.19 ms
RegChanMsk	7	1	XCONV	0: no sample 1: Sample X channel	
	6	1	YCONV	0: no sample 1: Sample Y channel	
	5	0	Z1CONV	0: no sample 1: Sample Z1 channel	
	4	0	Z2CONV	0: no sample 1: Sample Z2 channel	
	3	0	AUXCONV	0: no sample 1: Sample AUX channel	
	0	0	reserved		
	0	0	reserved		
	0	0	reserved		
RegStat	The host status reading allows the host to read the status of the SX8652. The data goes from the SX8652 towards the host. Host writing to this register is ignored.				
	7	0	CONVIRQ	0: no IRQ pending 1: Conversion sequence finished IRQ is cleared by the channel data read command	
	6	0	PENIRQ	Operational in pen detect mode 0: no IRQ pending 1: Pen detected IRQ pending IRQ is cleared by the RegStat reading	
	5	1	RSTEVENT	A reset event has occurred	
	4:0	00000	reserved		
RegSoftReset	7:0	0x00	If the host writes the value 0xDE to this register, then the SX8652 will be reset. Any other data will not affect the SX8652		

Table 13. SX8652 Register

6.4. Power-Up



The NIRQ pin is kept low during SX8652 power-up.

During power-up, the SX8652 is not accessible and SPI communications are ignored.

As soon as NIRQ rises, the SX8652 is ready for SPI communication.

Figure 21. Power-up, NIRQ

6.5. Reset

The POR of the SX8652 will reset all registers and states of the SX8652 at power-up.

Additionally the host can reset the SX8652 by asserting the NRST pin (active low) and also via the SPI bus.

If NRST is driven LOW, then NIRQ will be driven low by the SX8652. When NRST is released (or set to high) then NIRQ will be released by the SX8652.

The circuit has also a soft reset capability. When writing the code 0xDE to the register RegSoftReset, the circuit will be reset.

7. Modes of Operation

The SX8652 has four operation modes that are configured using the SPI commands as defined in Table 10 and Table 13.

These 4 modes are:

- manual (command ‘MANAUTO’ and RATE=0),
- automatic (command ‘MANAUTO’ and RATE>0),
- pen detect (command ‘PENDET’),
- pen trigger mode (command ‘PENTRG’).

At startup the SX8652 is set in manual mode.

In the manual mode the SX8652 is entirely stopped except for the SPI peripheral which accepts host commands. This mode requires RATE equal to be zero (RATE = 0, see Table 13).

In the automatic mode the SX8652 will sequence automatic channel conversions. This mode requires RATE to be larger than zero (RATE > 0, see Table 13).

In the PENDET mode the pen detection is activated. The SX8652 will generate an interrupt (NIRQ) upon pen detection and set the PENIRQ bit in the SPI status register. To quit the PENDET mode the host needs to configure the manual mode.

In the PENTRG mode the pen detection is activated and a channel conversion will start after the detection of a pen. The SX8652 will generate an interrupt (NIRQ) upon pen detection and set the CONVIRQ bit in the SPI status register. To quit the PENTRIG mode the host needs to configure the manual mode. The PENTRG mode offers the best compromise between power consumption and coordinate throughput.

7.1. Manual Mode

In manual mode (RATE=0) single actions are triggered by the SPI commands described in Table 14.

When a command is received, the SX8652 executes the associated task and waits for the next command. It is up to the host to sequence all actions.

Command	Action
CONVERT(CHAN)	Select and bias a channel Wait for the programmed settling time (POWDLY) Start conversion
SELECT(CHAN)	Select and bias a channel

Table 14. CONVERT and SELECT command

The channel can be biased for an arbitrary amount of time by first sending a SELECT command and then a CONVERT command once the settling time requirement is met.

The SELECT command can be omitted if the large range of POWDLY settings cover the requirements. In the latter case, the CONVERT command alone is enough to perform an acquisition.

With CHAN=SEQ, multiple channels are sampled. This requires programming the POWDLY field in register RegCTRL0. The selected channel will be powered during POWDLY before a conversion is started. The channel bias is automatically removed after the conversion has completed.

7.2. Automatic mode

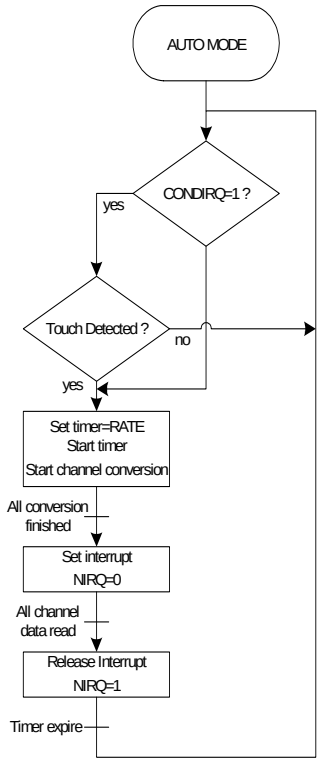


Figure 22. AUTO Mode Flowchart

In automatic mode (RATE > 0), SX8652 will automatically decide when to start acquisition, sequence all the acquisitions and alerts the host if data is available for download with a NIRQ. The host will read the channels and the SX8652 will start again with the next conversion cycle.

The fastest coordinate rate is obtained if the host reads the channels immediately after the NIRQ.

To not loose data, the SX8652 will not begin conversion before the host read the channels. If after the NIRQ a delay superior to the sampling period is made by the host to read the channels a slower coordinate rate is obtained.

When the control CONDIRQ bit (see register RegStat Table 13) is set to '1' then the interrupts will only be generated if the pen detect occurred. This result in a regular interrupt stream, as long as the host performs the read channel commands, and the screen is touched. When the screen is not touched, interrupts does not occur.

If the control CONDIRQ bit is cleared to '0', the interrupts will be always generated. In case there is no pen detected on the screen then the coordinate data will be qualified as invalid, see section [6.1.5]. This result in a regular interrupt stream, as long as the host performs the read channel commands, independent of the screen being touched or not.

This working is illustrated in Figure 22.

Figure 23 shows the SPI working in automatic mode with CONDIRQ=1. After the first sentence send through the SPI to make the initialization, traffic is reduced as only reads are required.

The processing time is the necessary time for the SX8652 to makes the pendetection, the settling time (POWDLY) and the conversion. This time increases with the number of channel selected and the filter used.All succeeding conversions notifies the host by an interrupt signal and the host only needs to issue the SPI read command.

The reads occur at the RATE interval.

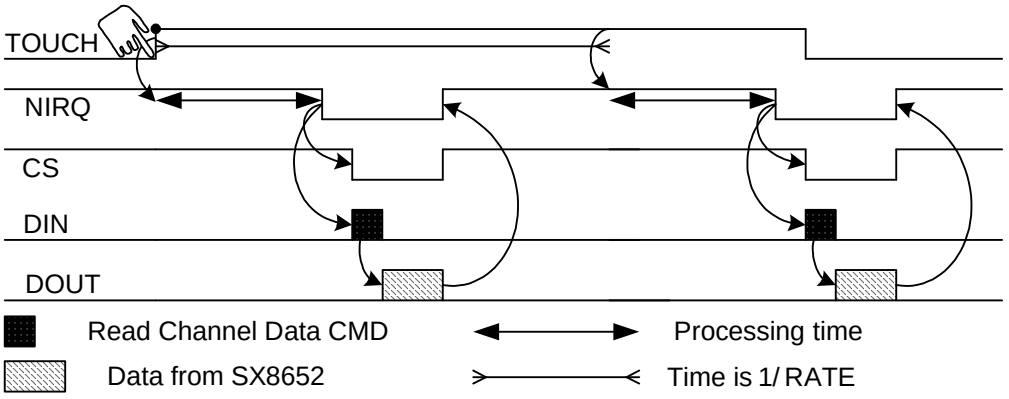
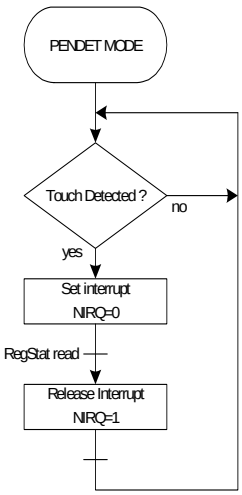


Figure 23. SPI working in AUTO mode

7.3. PENDET Mode



The PENDET mode can be used if the host only needs to know if the screen has been touched or not and take from that information further actions. When pen detect circuitry is triggered the interrupt signal NIRQ will be generated and the status register bit 'PENIRQ' will be set. The bit is cleared by reading the status register RegStat.

Figure 24. PENDET Mode Flowchart

7.4. PENTRIG Mode

The PENTRIG mode offers the best compromise between power consumption and coordinate throughput.

In this mode the SX8652 will wait until a pen is detected on the screen and then starts the coordinate conversions. The host will be signalled only when the screen is touched and coordinates are available.

The coordinate rate in pen trigger mode is determined by the speed of the host reading the channels and the conversion times of the channels. The host performs the minimum number of SPI commands in this mode.

The host has to wait for the NIRQ interrupt to make the acquisition of the data.

The flowchart and the SPI working is illustrated in Figure 25.

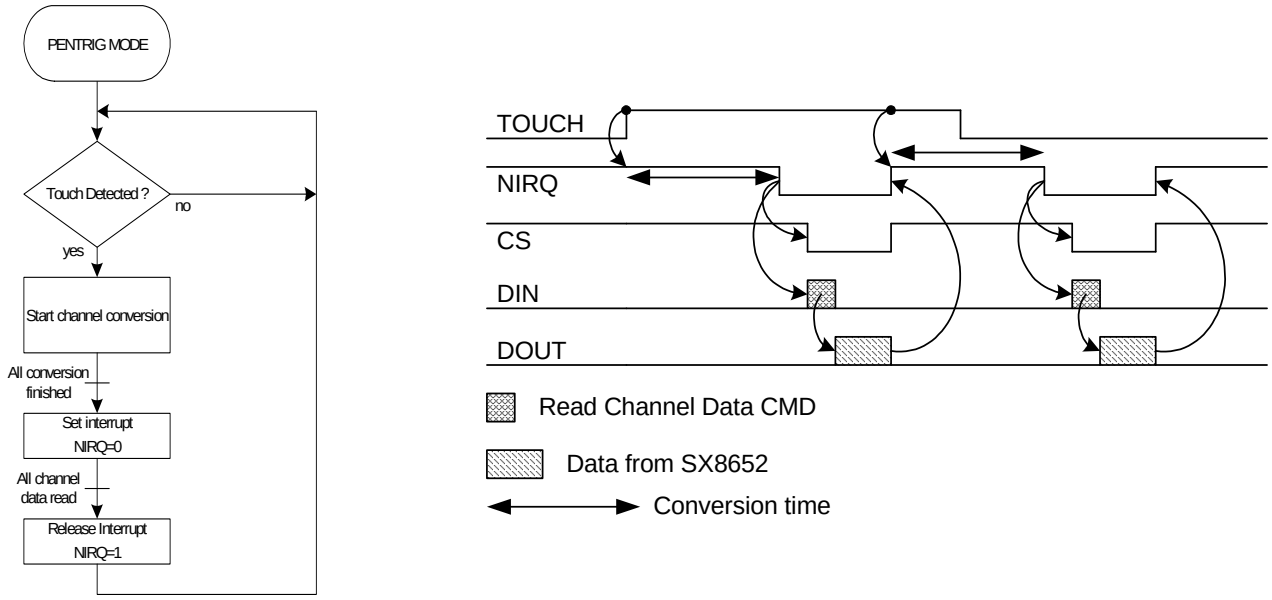


Figure 25. PENTRIG Mode Flowchart and SPI working in PENTRIG mode

8. Application Information

This section describes in more detail application oriented data.

8.1. Acquisition Setup

Prior to an acquisition, the SX8652 can be setup by writing the control registers. Registers are written by issuing the register write command. They can be read by issuing the read command. Please refer to the section [6.3].

If no registers are written, the circuit will start in manual mode.

8.2. Channel Selection

The SX8652 can be setup to start a single channel conversion or to convert several channels in sequence. For a single conversion, the channel to be converted is determined from the CHAN(2:0) field in the command word (defined in Table 11).

Several channels can be acquired sequentially by setting the CHAN(2:0) field to SEQ. The channels will be sampled in the order defined by register RegChanMsk from MSB to LSB.

If a “one” is written in a channel mask, the corresponding channel will be sampled, in the opposite case, it is ignored and the next selected channel is chosen.

8.3. Noise Reduction

A noisy environment can decrease the performance of the controller. For example, an LCD display located just under the touch screen can adds a lot of noise on the high impedance A/D converter inputs.

8.3.1. POWDLY

In order to perform correct coordinates acquisition properly, some time must be given for the touch screen to reach a proper level. It is a function of the PCB trace resistance connecting the SX8652 to the touchscreen and also the capacitance of the touchscreen. If tau is this RC time constant then POWDLY duration must be programmed to 10 tau to reach 12 bit accuracy.

Adding a capacitor from the touch screen drivers to ground is a solution to minimize external noise. A low-pass filter created by the capacitor may increase settling time. Therefore, use POWDLY to stretch the acquisition period. POWDLY can be estimated by the following formula: $PowDly = 10 \times Rtouch \times Ctouch$

Rtouch is the sum of the panel resistances plus any significant series input resistance, Rxtot + Rytot + Ri.

Ctouch is the sum of the touch panel capacitance plus any noise filtering and routing capacitances.

8.3.2. SETDLY

A second method of noise filtering uses an averaging filter as described in section [6] (Data processing). In this case, the chip will sequence up to 7 conversions on each channel. The parameter SETDLY sets the settling time between the consecutive conversions.

In most applications, SETDLY can be set to 0. In some particular applications, where accuracy of 1LSB is required and Ctouch is less than 100nF a specific value should be determined.

8.3.3. AUX Input

An alternate conversion trigger method can be used with 4-wire touchscreen if the host system provides additional digital signals that indicate noisy or noise-free periods. The SX8652 can be set up to start conversions triggered by the AUX pin. A rising edge, a falling edge or both can trigger the conversion. To enter this mode, AUXACQ must be set to a different value than '00' as defined in Table 13. The AUX edge will first trigger the bias delay (POWDLY). Following the programmed delay, the channel acquisition takes place.

8.4. Interrupt Generation

An interrupt (NIRQ=0) will be generated:

- During the power-up phase or after a reset
- After completion of a conversion in MANUAL, PENTRIG or AUTO mode. CONVIRQ (bit [7] of RegStat) will be set at the same time.
- After a touch on the panel is detected in PENDET mode. PENIRQ (bit [6] of RegStat) will be set at the same time.

The NIRQ will be released and pulled high(NIRQ=1) by the external pull-up resistor:

- When the power-up phase is finished
- When the host read all channels data that were previously converted by the SX8652 in MANUAL, PENTRIG or AUTO mode. CONVIRQ will be cleared at the same time.
- When the host read the status register in PENDET mode. PENIRQ, will be cleared at the same time.

An active NIRQ (low) needs to be cleared before any new conversions will occur.

8.5. Coordinate Throughput Rate

The coordinate throughput rate depends on the following factors:

- The SPI communication time: T_{com}
- The conversion time: T_{conv}

The coordinate rate is the frequency to get the X, Y, Z1 and Z2 coordinate: $CoordRate = \frac{1}{T_{com} + T_{conv}}$

8.5.1. SPI Communication Time

The minimum time to read the channel data in PENTRIG mode is: $T_{com} = (8 + 16 \times N_{chan}) \times T_{SPI}$

The highest throughput will be obtained with a SPI frequency of 5MHz when the host read the channel data as quickly as possible after the NIRQ falling edge.

8.5.2. Conversion Time

The maximum possible throughput can be estimated with the following equation

$$T_{conv} = 47 \cdot T_{osc} + N_{chan}[POWDLY + SETDLY(N_{filt} - 1) + T_{osc}(21N_{filt} + 1)]$$

with:

- N_{filt} = {1,3,5,7} based on the order defined for the filter FILT (see Figure 7).
- N_{chan} = {1,2,3,4,5} based on the number of channels defined in RegChanMsk
- POWDLY = 0.5us to 18.19ms, settling time as defined in RegCtrl0
- SETDLY = 0.5us to 18.19ms, settling time when filtering as defined in RegCtrl2
- Tosc is the oscillator period (555ns +/- 15%)

Table 15 gives some examples of Coordinate Rate and Sample Rate for various setting in PENTRIG mode.

Nch [1..5]	Nfilt [1 3 5 7]	PowDly [uS]	SetDly [uS]	Tconv [uS]	Tcomm [uS]	CoordRate [kSPS]
2	1	0.5	-	51	8	16.7
2	3	71	0.5	190	8	5.0
4	3	140	0.5	740	14	1.3

Table 15. Coordinate throughput examples

8.5.3. AUTO MODE

In AUTO mode, the coordinate throughput rate is the RATE set in RegCtrl0 if the host retrieve channel data at this RATE.

The RATE set should be superior or equal to the CoordRate.

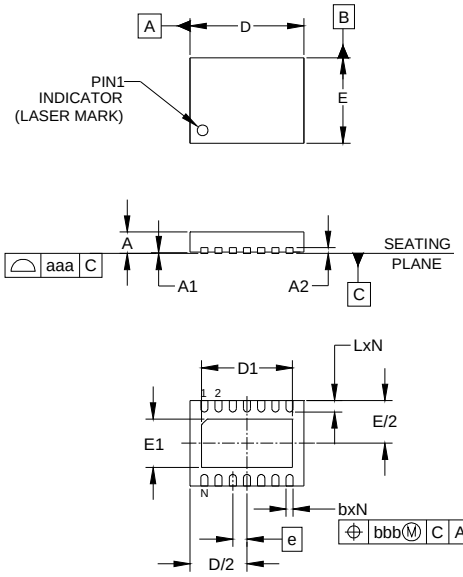
8.6. ESD event

In case of ESD event, the chip can reset to protect its internal circuitry. The bit *RSTEVENT* indicates that a reset event has occurs.

ESD event may trig the pen detection circuitry. In this case wrong data will be send to the host. To detect this false coordinates on 4-wire touchscreen, a pressure measurement can be done. The conditions Z1<10 and Z2>4070 indicate an ESD event.

9. Packaging Information

9.1. DFN Package

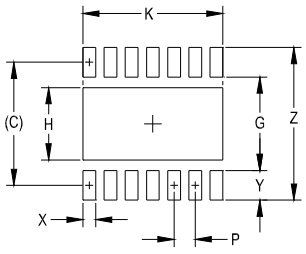


DIMENSIONS			
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.70	-	0.80
A1	0.00	0.02	0.05
A2	-	(0.20)	-
b	0.18	0.25	0.30
D	3.90	4.00	4.10
D1	3.05	3.20	3.30
E	2.90	3.00	3.10
E1	1.55	1.70	1.80
e	0.50 BSC		
L	0.30	0.40	0.50
N	14		
aaa	0.08		
bbb	0.10		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

Figure 26. DFN Package Outline Drawing



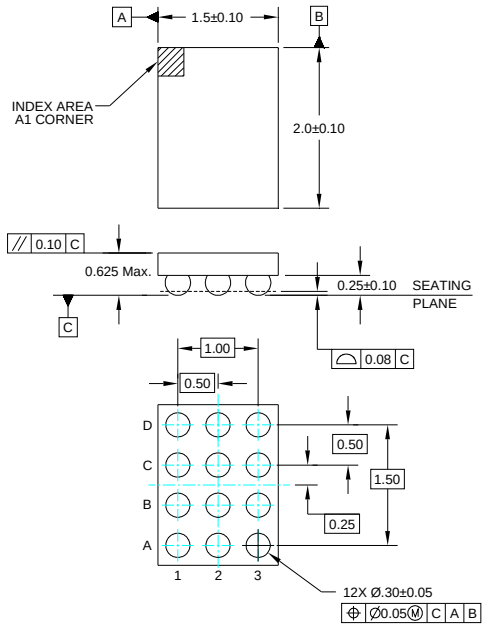
DIMENSIONS	
DIM	MILLIMETERS
C	(2.90)
G	2.20
H	1.70
K	3.30
P	0.50
X	0.30
Y	0.70
Z	3.60

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
3. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD SHALL BE CONNECTED TO A SYSTEM GROUND PLANE. FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR FUNCTIONAL PERFORMANCE OF THE DEVICE.

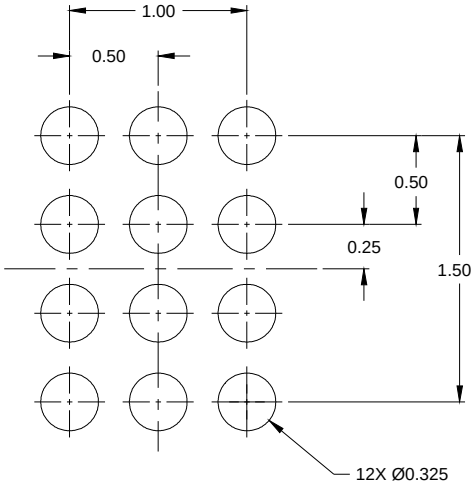
Figure 27. DFN Package Land Pattern

9.2. WLCSP Package



NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS

Figure 28. WLCSP Package Outline Drawing



NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

Figure 29. WLCSP Land Pattern of WLCSP

Contact information

Semtech Corporation Advanced Communications & Sensing Products

	E-mail: sales@semtech.comacsupport@semtech.comInternet: http://www.semtech.com
USA	200 Flynn Road, Camarillo, CA 93012-8790. Tel: +1 805 498 2111 Fax: +1 805 498 3804
FAR EAST	12F, No. 89 Sec. 5, Nanking E. Road, Taipei, 105, TWN, R.O.C. Tel: +886 2 2748 3380 Fax: +886 2 2748 3390
EUROPE	Semtech Ltd., Units 2 & 3, Park Court, Premier Way, Abbey Park Industrial Estate, Romsey, Hampshire, SO51 9DN. Tel: +44 (0)1794 527 600 Fax: +44 (0)1794 527 601

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