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April 1st, 2010 Renesas Electronics Corporation

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MOS FIELD EFFECT TRANSISTOR μ PA2743T1A

SWITCHING N-CHANNEL POWER MOSFET

DESCRIPTION

The μ PA2743T1A is N-channel MOS Field Effect Transistor designed for power management applications of a notebook computer.

FEATURES

• Low on-state resistance

 $R_{DS(on)1} = 3.3 \text{ m}\Omega \text{ MAX.} \text{ (Vgs = 10 V, ID = 15 A)}$

 $R_{DS(on)2} = 4.6 \text{ m}\Omega \text{ MAX}. \text{ (Vgs} = 4.5 \text{ V, Ip} = 15 \text{ A)}$

- Built-in gate protection diode
- Thin type surface mount package with heat spreader (8-pin HVSON (6051))
- RoHS Compliant

ABSOLUTE MAXIMUM RATINGS (TA = 25°C, All terminals are connected.)

Drain to Source Voltage (VGS = 0 V)	VDSS	30	V
Gate to Source Voltage (VDS = 0 V)	Vgss	±20	V
Drain Current (DC)	I _{D(DC)}	±29	Α
Drain Current (pulse) Note1	I _{D(pulse)}	±170	Α
Total Power Dissipation Note2	P _{T1}	1.5	W
Total Power Dissipation (PW = 10 sec) Note2	P _{T2}	4.6	W
Channel Temperature	Tch	150	°C
Storage Temperature	Tstg	-55 to +150	°C
Single Avalanche Current Note3	las	29	Α
Single Avalanche Energy Note3	Eas	84.1	mJ

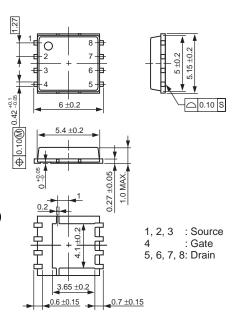
THERMAL RESISTANCE

Channel to Ambient Thermal Resistance Note2	Rth(ch-A)	83.3	°C/W
Channel to Case (Drain) Thermal Resistance	Rth(ch-C)	1.5	°C/W

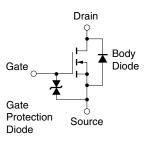
Notes 1. PW \leq 10 μ s, Duty Cycle \leq 1%

- 2. Mounted on a glass epoxy board of 25.4 mm x 25.4 mm x 0.8 mmt
- 3. Starting T_{ch} = 25°C, V_{DD} = 15 V, R_G = 25 Ω , V_{GS} = 20 \rightarrow 0 V, L = 100 μ H

PACKAGE DRAWING (Unit: mm)



EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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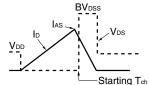
ELECTRICAL CHARACTERISTICS (TA = 25°C, All terminals are connected.)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	IDSS	V _{DS} = 30 V, V _{GS} = 0 V			10	μA
Gate Leakage Current	Igss	V _{GS} = ±20 V, V _{DS} = 0 V			±10	μΑ
Gate to Source Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	1.0		2.5	V
Forward Transfer Admittance Note	yfs	V _{DS} = 10 V, I _D = 15 A	13			S
Drain to Source On-state Resistance Note	RDS(on)1	V _{GS} = 10 V, I _D = 15 A		2.1	3.3	mΩ
	RDS(on)2	V _{GS} = 4.5 V, I _D = 15 A		3.7	4.6	mΩ
Input Capacitance	Ciss	V _{DS} = 15 V,		5080		pF
Output Capacitance	Coss	V _{GS} = 0 V,		650		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		380		pF
Turn-on Delay Time	t _{d(on)}	V _{DD} = 15 V, I _D = 15 A,		28		ns
Rise Time	tr	V _{GS} = 10 V,		29		ns
Turn-off Delay Time	t _{d(off)}	R _G = 10 Ω		109		ns
Fall Time	t f			32		ns
Total Gate Charge	Q _G	V _{DD} = 15 V,		39		nC
Gate to Source Charge	Qgs	V _{GS} = 5 V,		16		nC
Gate to Drain Charge	Q _{GD}	ID = 29 A		17		nC
Body Diode Forward Voltage Note	V _{F(S-D)}	I _F = 29 A, V _{GS} = 0 V		0.79	1.2	V
Reverse Recovery Time	trr	I _F = 29 A, V _{GS} = 0 V,		38		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A/μs		39		nC

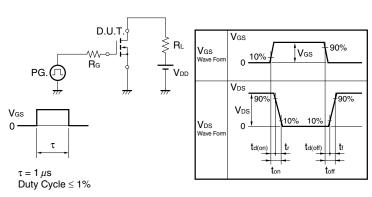
Note Pulsed

TEST CIRCUIT 1 AVALANCHE CAPABILITY

$\begin{array}{c|c} D.U.T. \\ \hline R_G = 25 \ \Omega \\ \hline V_{DD} \\ \hline \end{array}$



TEST CIRCUIT 2 SWITCHING TIME



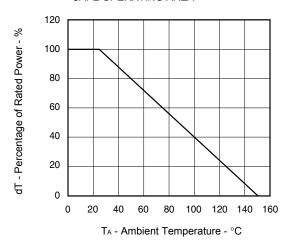
TEST CIRCUIT 3 GATE CHARGE

$$\begin{array}{c|c} D.U.T.. \\ \hline I_G = 2 \begin{array}{c} MA \\ \hline \end{array} \\ \hline \end{array}$$

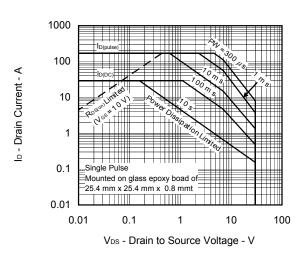
$$\begin{array}{c} PG. \\ \hline \end{array} \begin{array}{c} 50 \Omega \\ \hline \end{array} \begin{array}{c} V_{DD} \\ \hline \end{array}$$

TYPICAL CHARACTERISTICS (TA = 25°C)

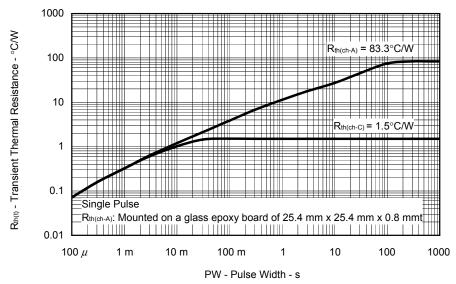
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



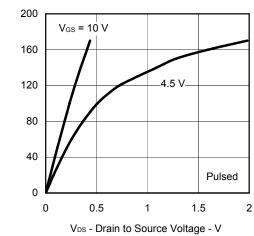
FORWARD BIAS SAFE OPERATING AREA



TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

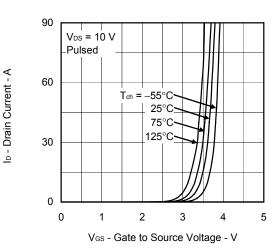


DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



Ip - Drain Current - A

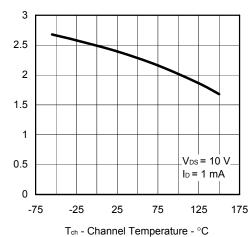
FORWARD TRANSFER CHARACTERISTICS



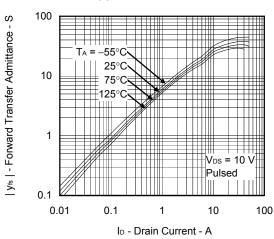
VGS(off) - Gate to Source Cut-off Voltage - V

R_{DS(m)} - Drain to Source On-state Resistance - mΩ

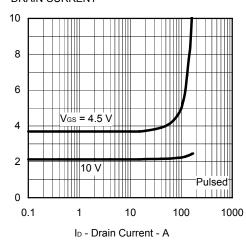
GATE TO SOURCE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



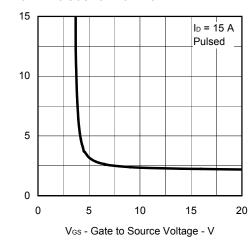
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



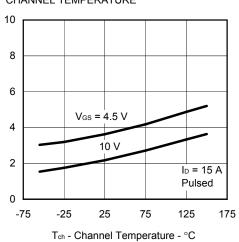
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



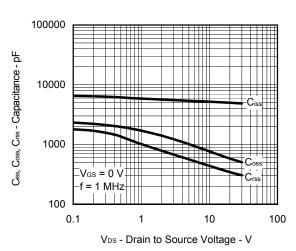
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



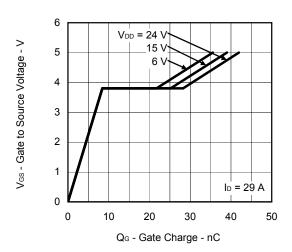
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



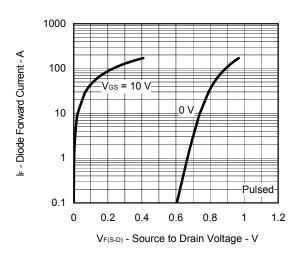
 $\mathsf{R}_{\mathsf{DS}(\mathsf{on})}$ - Drain to Source On-state Resistance - $m\Omega$

 $\mathsf{Res}_{^{(m)}}$ - Drain to Source On-state Resistance - $m\Omega$

DYNAMIC INPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE



ORDERING INFORMATION

PART NUMBER	LEAD PLATING	PACKING	PACKAGE	
μPA2743T1A-E1-AY Note	Duna Ca	Tana 2000 m/mad	8-pin HVSON (6051)	
μPA2743T1A-E2-AY Note	Pure Sn	Tape 3000 p/reel	0.10 g TYP.	

Note Pb-free (This product does not contain Pb in the external electrode.)

NEC μ PA2743T1A

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