19-0550; Rev 0; 5/06

Low-Cost Stereo Audio DACs

General Description

The MAX5556–MAX5559 stereo audio sigma-delta digital-to-analog converters (DACs) offer a simple and complete stereo digital-to-analog solution for media servers, set-top boxes, video-game hardware, automotive rear-seat entertainment and other general consumer audio applications. These DACs feature built-in digital interpolation/filtering, sigma-delta digital-to-analog conversion and analog output filtering. Control logic and mute circuitry minimize audible pops and clicks during power-up, power-down, clock changes, or when invalid clock conditions occur.

The MAX5556–MAX5559 receive input data over a flexible 3-wire interface, supporting I^2S-compatible, left-justified, right-justified 16-bit, and right-justified 18-bit audio data. Data can be clocked by either an external or internal serial clock. The internal serial clock frequency is programmable by selection of a master clock (MCLK) and sample clock (LRCLK) ratio. Sampling rates from 2kHz to 50kHz are supported.

The MAX5556–MAX5559 operate from a single +4.75V to +5.5V analog supply with total harmonic distortion plus noise below -87dB. These devices are available in 8-pin SO packages and are specified over the -40°C to +85°C industrial temperature range.

Applications

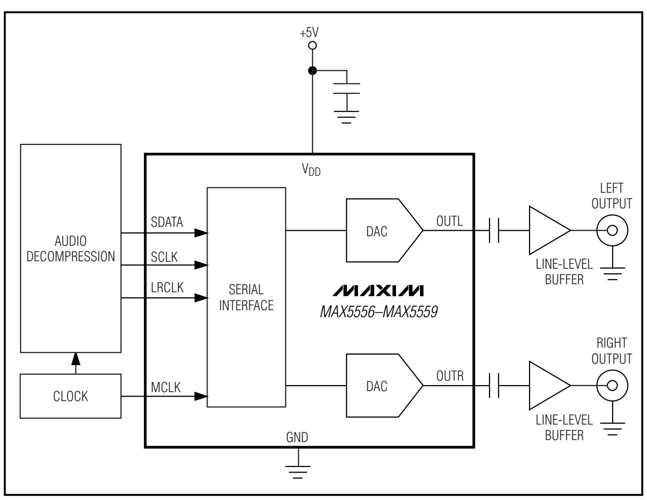
Digital Video Recorders and Media Servers

Set-Top Boxes

Video-Game Hardware

Automotive Rear-Seat Entertainment

Typical Operating Circuit



Features

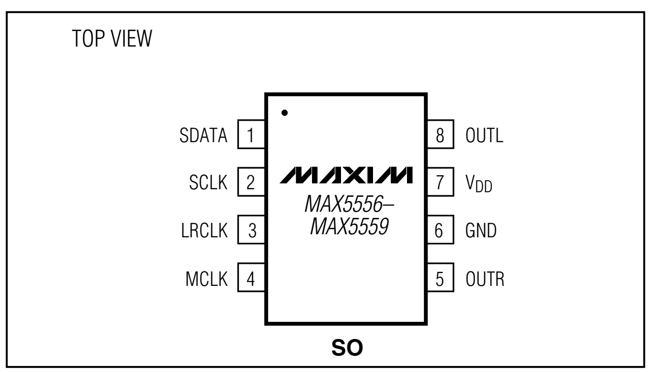
- ♦ **Simple and Complete Stereo Audio DAC Solutions, No Controls to Set**
- ♦ **Sigma-Delta Stereo DACs with Built-In Interpolation and Analog Output Filters**
- ♦ **I^2S-Compatible Digital Audio Interface (MAX5556)**
- ♦ **Clickless/Popless Operation**
- ♦ **Output Voltage Swing: 3.5V_{P-P}**
- ♦ **-87dB THD+N**
- ♦ **+87dB Dynamic Range**
- ♦ **Sample Frequencies (f_S) from 2kHz to 50kHz**
- ♦ **Master Clock (MCLK) up to 25MHz**
- ♦ **Automatic Detection of Clock Ratio (MCLK/LRCLK)**

Ordering Information

PART	PIN-PACKAGE	PKG CODE	DATA FORMAT
MAX5556ESA	8 SO	S8-5	Left-justified I^2S data
MAX5557ESA*	8 SO	S8-5	Left-justified data
MAX5558ESA*	8 SO	S8-5	Right-justified 16-Bit data
MAX5559ESA*	8 SO	S8-5	Right-justified 18-Bit data

Note: *All devices are specified over the -40°C to +85°C operating temperature range. Contact factory for +105°C operation.*
**Future product—contact factory for availability.*

Pin Configuration



ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND ....-0.3V to +6.0V
OUTL, OUTR, SDATA to GND.................. -0.3V to (V_{DD} + 0.3V)
Current Into Any Pin (excluding V_{DD} and GND)..............±10mA
OUTL, OUTR Shorted to GND...................................Continuous
SCLK, LRCLK, MCLK to GND ....-0.3V to +6.0V
Continuous Power Dissipation (T_A = +70°C)
8-Pin SO (derate 5.88mW above +70°C)...................471mW

Package Thermal Resistance (θ_{JA}) ....170°C/W
Operating Temperature Range ....-40°C to +85°C
Junction Temperature ....+150°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +4.75V to +5.5V, GND = 0V, $R_{OUT\_}$ = 10kΩ, $C_{OUT\_}$ = 10pF, 0dBFS sine-wave signal at 997Hz, f_{LRCLK} (f_S) = 48kHz, f_{MCLK} = 12.288MHz, measurement bandwidth 10Hz to 20kHz, unless otherwise specified. T_A = -40°C to +85°C, unless otherwise noted. Outputs are unloaded, unless otherwise noted. Typical values at V_{DD} = +5V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Supply Voltage	V_{DD}		4.75	5.0	5.50	V
Supply Current	I_{DD}	Up to 48ksps		13	15	mA
		Static digital		6	8.5	
Power Dissipation		Up to 48ksps		65	82.5	mW
		Static digital		30	44	
DYNAMIC PERFORMANCE (Note 2)						
Dynamic Range, 16-Bit		Unweighted	84	86		dB
		A-weighted	86	90		
Dynamic Range, 18-Bit to 24-Bit		Unweighted		87		dB
		A-weighted		91		
Total Harmonic Distortion Plus Noise, 16-Bit	THD+N	0dBFS		-86	-81	dB
		-20dBFS		-67		
		-60dBFS		-26	-24	
Total Harmonic Distortion Plus Noise, 18-Bit to 24-Bit	THD+N	0dBFS		-87		dB
		-20dBFS		-68		
		-60dBFS		-27		
Interchannel Isolation		1kHz full-scale output (crosstalk)		94		dB
COMBINED DIGITAL AND INTEGRATED ANALOG FILTER FREQUENCY RESPONSE (Note 3)						
Passband		-0.5dB corner	0.46			f_S
		-3dB corner			0.49	
		-6dB corner			0.50	
Frequency Response/Passband Ripple		10Hz to 20kHz (f_S = 48kHz)	-0.025		+0.08	dB
		10Hz to 20kHz (f_S = 44.1kHz)	-0.025		+0.08	
		10Hz to 16kHz (f_S = 32kHz)	-6.000		+0.073	
Stopband					0.5465	f_S
Stopband Attenuation			52			dB
Group Delay	t_{gd}			20 / f_S		s
Passband Group-Delay Variation	Δt_{gd}	20Hz to 20kHz		±0.4 / f_S		s

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +4.75V to +5.5V, GND = 0V, $R_{OUT\_}$ = 10kΩ, $C_{OUT\_}$ = 10pF, 0dBFS sine-wave signal at 997Hz, f_{LRCLK} (f_S) = 48kHz, f_{MCLK} = 12.288MHz, measurement bandwidth 10Hz to 20kHz, unless otherwise specified. T_A = -40°C to +85°C, unless otherwise noted. Outputs are unloaded, unless otherwise noted. Typical values at V_{DD} = +5V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS						
Interchannel Gain Mismatch				0.1	0.4	dB
Gain Error			-5		+5	%
Gain Drift				100		ppm/°C
ANALOG OUTPUTS						
Full-Scale Output Voltage	V_{OUTR}, V_{OUTL}		3.25	3.5	3.75	V_{P-P}
DC Quiescent Output Voltage	V_Q	Input code = 0		2.4		V
Minimum Load Resistance	R_L			3		kΩ
Maximum Load Capacitance	C_L			100		pF
Power-Supply Rejection Ratio	PSRR	V_{RIPPLE} = 100mV_{P-P}, frequency = 1kHz		66		dB
POP AND CLICK SUPPRESSION						
Mute Attenuation				100		dB
Power-Up Until Bias Established		Figure 14		360		ms
Valid Clock to Normal Operation		Soft-start ramp time, Figure 15 (Note 5)		20		ms
DIGITAL AUDIO INTERFACE (SCLK, SDATA, MCLK, LRCLK)						
Input-Voltage High	V_{IH}		2.0			V
Input-Voltage Low	V_{IL}				0.8	V
Input Leakage Current	I_{IN}		-10		+10	µA
Input Capacitance				8		pF
TIMING CHARACTERISTICS						
Input Sample Rate	f_S		2		50	kHz
MCLK Pulse-Width Low	t_{MCLKL}	MCLK/LRCLK = 512	10			ns
		MCLK/LRCLK = 384	20			
		MCLK/LRCLK = 256	20			
MCLK Pulse-Width High	t_{MCLKH}	MCLK/LRCLK = 512	10			ns
		MCLK/LRCLK = 384	20			
		MCLK/LRCLK = 256	20			
EXTERNAL SCLK MODE						
LRCLK Duty Cycle		(Note 6)	25		75	%
SCLK Pulse-Width Low	t_{SCLKL}		20			ns
SCLK Pulse-Width High	t_{SCLKH}		20			ns
SCLK Period	t_{SCLK}		1 / (128 x f_S)			ns
LRCLK Edge to SCLK Rising	t_{SLRS}		20			ns
LRCLK Edge to SCLK Rising	t_{SLRH}		20			ns
SDATA Valid to SCLK Rising	t_{SDS}		20			ns
SCLK Rising to SDATA Hold Time	t_{SDH}		20			ns

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +4.75V to +5.5V, GND = 0V, $R_{OUT\_}$ = 10kΩ, $C_{OUT\_}$ = 10pF, 0dBFS sine-wave signal at 997Hz, f_{LRCLK} (f_S) = 48kHz, f_{MCLK} = 12.288MHz, measurement bandwidth 10Hz to 20kHz, unless otherwise specified. T_A = -40°C to +85°C, unless otherwise noted. Outputs are unloaded, unless otherwise noted. Typical values at V_{DD} = +5V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INTERNAL SCLK MODE						
LRCLK Duty Cycle		(Note 7)		50		%
Internal SCLK Period	t_{ISCLK}	(Note 8)	1 / f_{SCLK}			ns
LRCLK Edge to Internal SCLK	t_{ISCLKR}			t_{ISCLK} / 2		ns
SDATA Valid to Internal SCLK	t_{ISDS}	MCLK period = t_{MCLK}	t_{MCLK} + 10			ns
SDATA Valid to Internal SCLK	t_{ISDH}	MCLK period = t_{MCLK}	t_{MCLK}			ns

Note 1: 100% production tested at T_A = +85°C. Limits to -40°C are guaranteed by design.
Note 2: 0.5 LSB of triangular PDF dither added to data.
Note 3: Guaranteed by design, not production tested.
Note 4: PSRR test block diagram shown in Figure 1 denotes the test setup used to measure PSRR.
Note 5: Volume ramping interval starts from establishment of a valid MCLK to LRCLK ratio. Total time is proportional to the sample rate (f_S). 20ms based on 48ksps operation.
Note 6: In external SCLK mode, LRCLK duty cycles are not limited, provided all data formatting requirements are met. See Figures 4–7.
Note 7: The LRCLK duty cycle must be 50% ±1/2 MCLK period in internal SCLK mode.
Note 8: The SCLK/LRCLK ratio can be set to 32, 48, or 64, depending on the device and the MCLK/LRCLK ratio selected. See Figures 4–7.

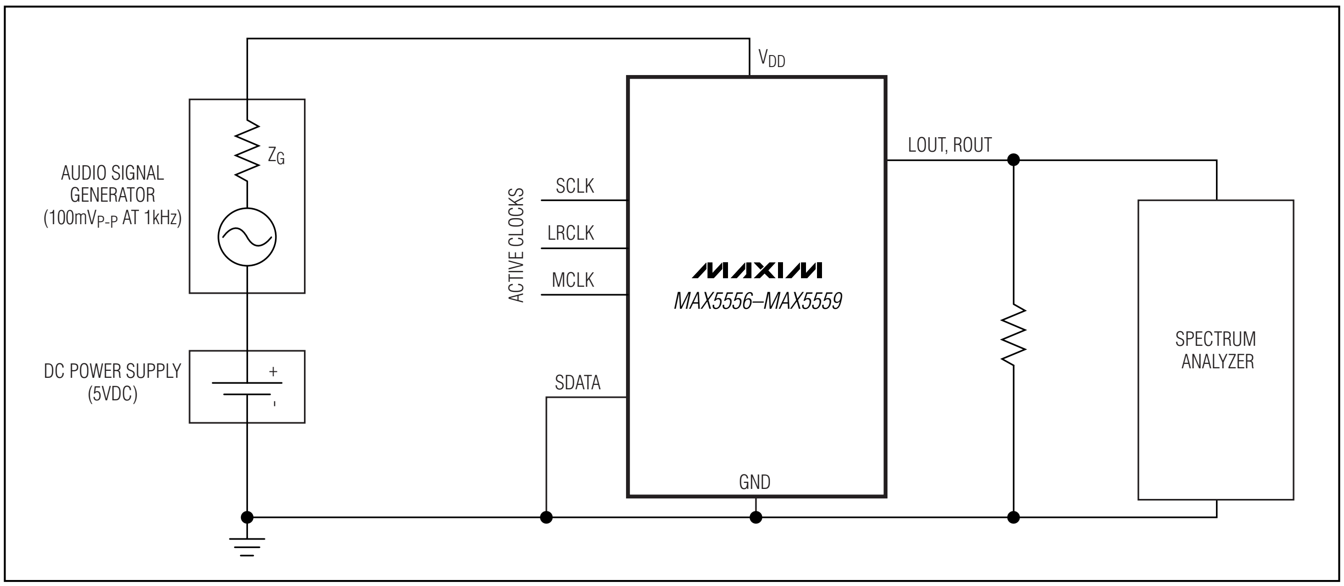
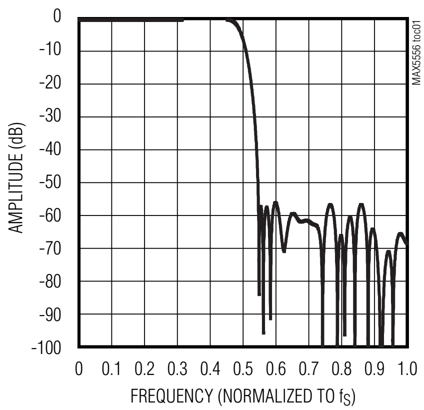


Figure 1. PSRR Test Block Diagram

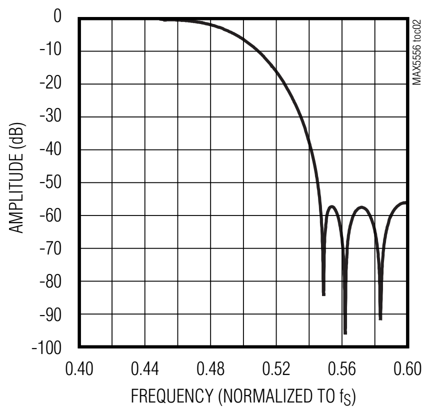
Typical Operating Characteristics

(V_{DD} = +5V, GND = 0V, $R_{OUT\_}$ = 10kΩ, $C_{OUT\_}$ = 10pF, T_A = +25°C, unless otherwise noted.)

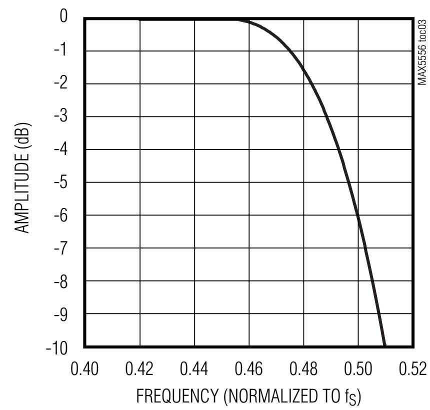
STOPBAND REJECTION



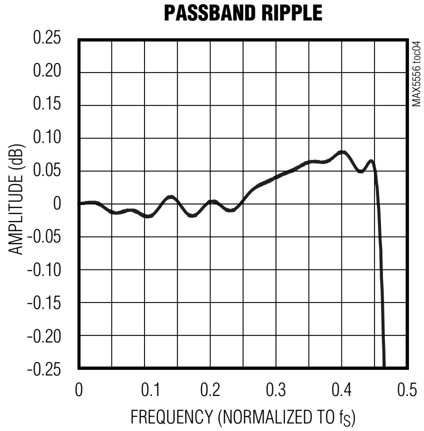
TRANSITION BAND



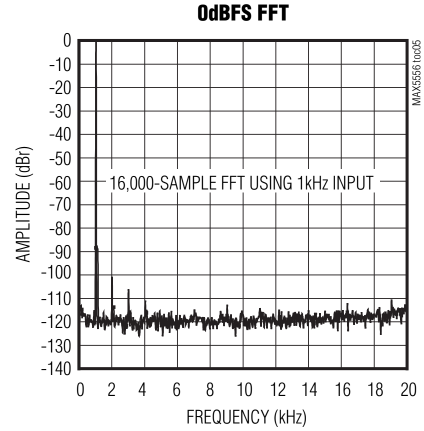
TRANSITION BAND DETAIL



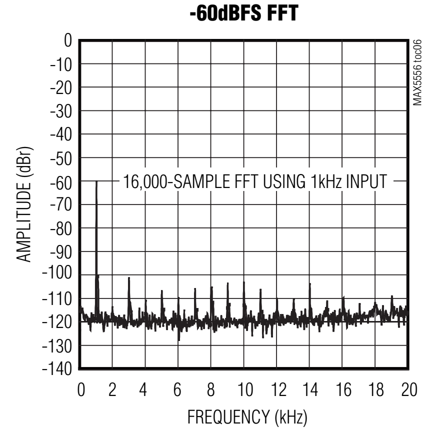
PASSBAND RIPPLE



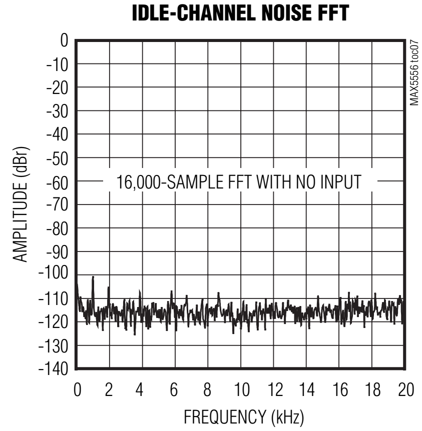
0dBFS FFT



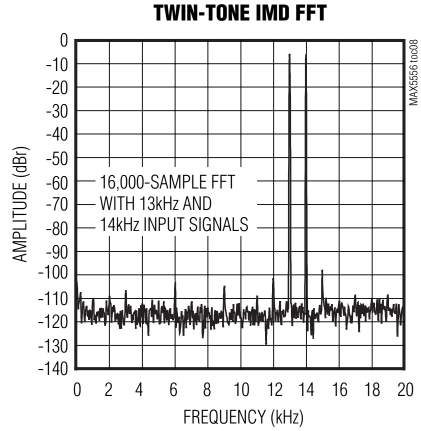
-60dBFS FFT



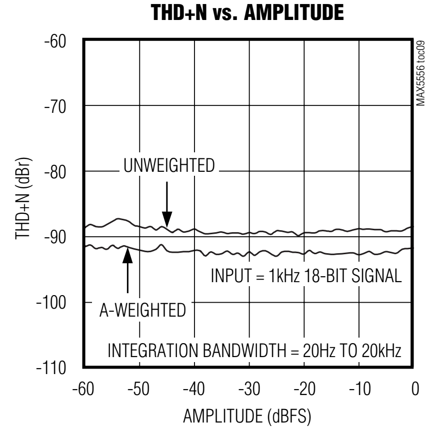
IDLE-CHANNEL NOISE FFT



TWIN-TONE IMD FFT

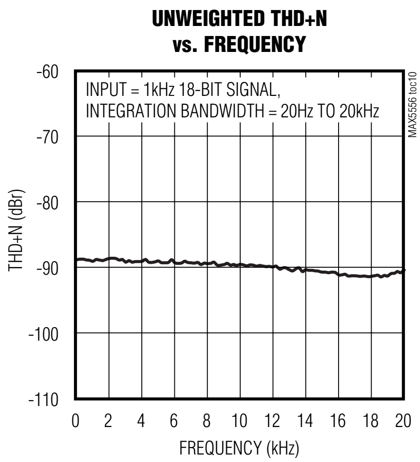


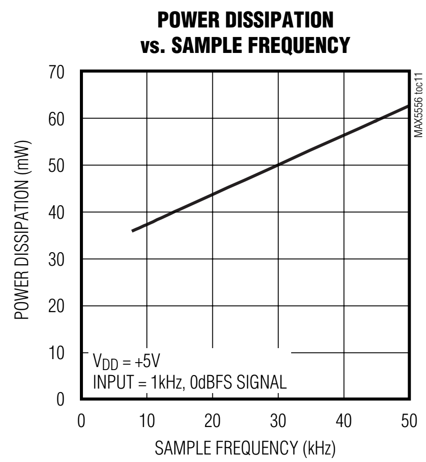
THD+N vs. AMPLITUDE

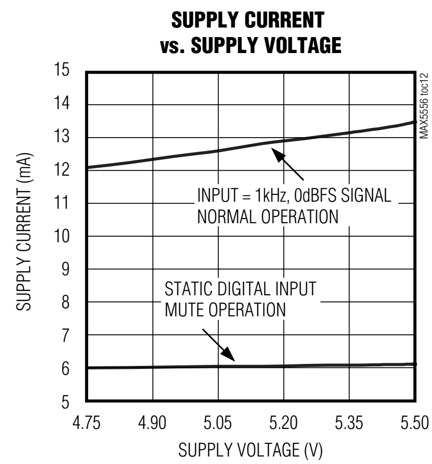


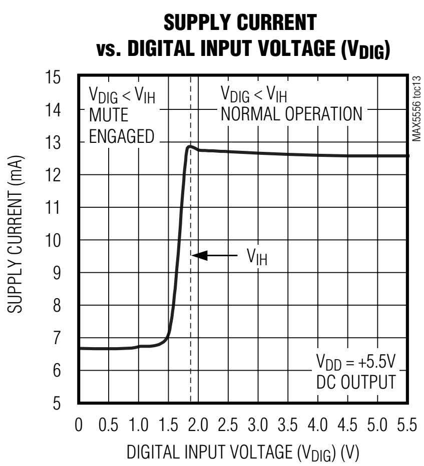
Typical Operating Characteristics (continued)

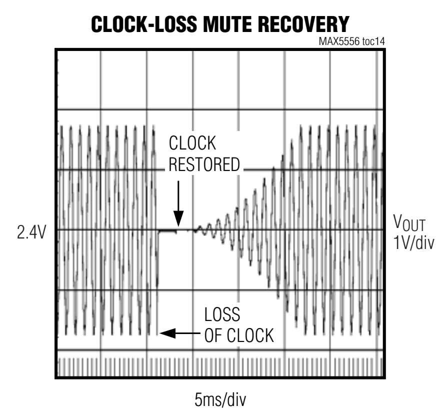
(V_{DD} = +5V, GND = 0V, $R_{OUT\_}$ = 10kΩ, $C_{OUT\_}$ = 10pF, T_A = +25°C, unless otherwise noted.)

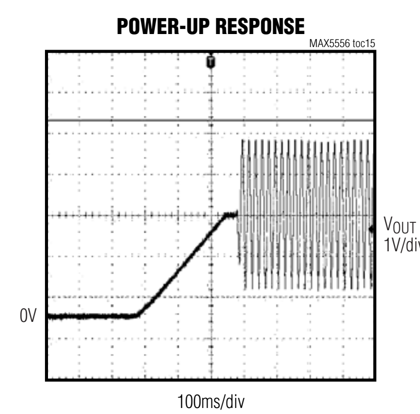












Pin Description

PIN	NAME	FUNCTION
1	SDATA	Serial Audio Data Input. Data is clocked into the MAX5556–MAX5559 on the rising edge of the internal or external SCLK. Data is input in two's complement format, MSB first. The state of LRCLK determines whether data is directed to OUTL or OUTR.
2	SCLK	External Serial Clock Input. Data is strobed on the rising edge of SCLK.
3	LRCLK	Left-/Right-Channel Select Clock. For the MAX5556, drive LRCLK low to direct data to OUTL or LRCLK high to direct data to OUTR. For the MAX5557/MAX5558/MAX5559, drive LRCLK high to direct data to OUTL or LRCLK low to direct data to OUTR.
4	MCLK	Master Clock Input. The MCLK/LRCLK ratio must equal to 256, 384, or 512.
5	OUTR	Right-Channel Analog Output
6	GND	Ground
7	V_{DD}	Power-Supply Input. Bypass V_{DD} to GND with a 0.1µF capacitor in parallel with a 4.7µF capacitor as close to V_{DD} as possible. Place the 0.1µF capacitor closest to V_{DD}.
8	OUTL	Left-Channel Analog Output

Detailed Description

The MAX5556–MAX5559 stereo audio sigma-delta DACs offer a complete stereo digital-to-analog system for consumer audio applications. The MAX5556–MAX5559 feature built-in digital interpolation/filtering, sigma-delta digital-to-analog conversion and analog output filters (Figure 2). Control logic and mute circuitry minimize audible pops and clicks during power-up, power-down, and whenever invalid clock conditions occur.

These stereo audio DACs receive input data over a 3-wire interface that supports up to 24 bits of left-justified, right-justified, or I^2S-compatible audio data. The MAX5556 accepts left-justified I^2S data, up to 24 bits. The MAX5557 accepts left-justified data, up to 24 bits. The MAX5558 accepts right-justified 16-bit data. The MAX5559 accepts right-justified 18-bit data. These DACs also support a wide range of sample rates from 2kHz to 48kHz. Direct analog output data is routed to the right or left output by driving LRCLK high or low. See the *Clock and Data Interface* section.

The MAX5556–MAX5559 support MCLK/LRCLK ratios of 256, 384, or 512. These devices allow a change to the clock speed ratio without causing glitches on the analog outputs by internally muting the audio during invalid clock conditions. The internal mute function ramps down the audio amplitude and forces the analog outputs to a 2.4V quiescent voltage immediately upon clock loss or change of ratio. A soft-start routine is then engaged when a valid clock ratio is re-established, producing clickless and popless continuous operation.

The MAX5556–MAX5559 operate from a +4.75V to +5.5V analog supply and feature +87dB dynamic range with total harmonic distortion typically below -87dB.

Interpolator

The digital interpolation filter eliminates images of the baseband audio signal that exist at multiples of the input sample rate (f_S). The resulting upsampled frequency spectrum has images of the input signal at multiples of 8 x f_S. An additional upsampling sinc filter further reduces upsampling images up to 64 x f_S. These images are ultimately removed through the internal analog lowpass filter and the external analog output filter.

Sigma-Delta Modulator/DAC

The MAX5556–MAX5559 use a multibit sigma-delta DAC with an oversampling ratio (OSR) of 64 to achieve a wide dynamic range. The sigma-delta modulator accepts a 3-bit data stream from the interpolation filter at a rate of 64 x f_S (f_S = LRCLK frequency) and provides an analog voltage representation of that data stream.

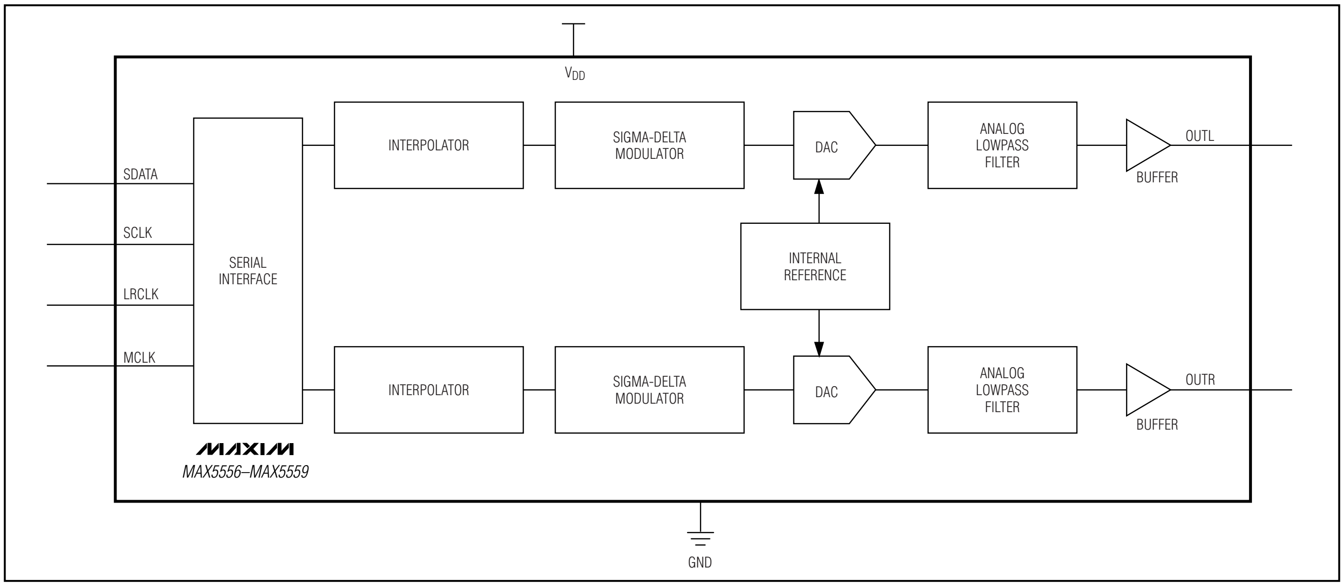


Figure 2. Functional Diagram

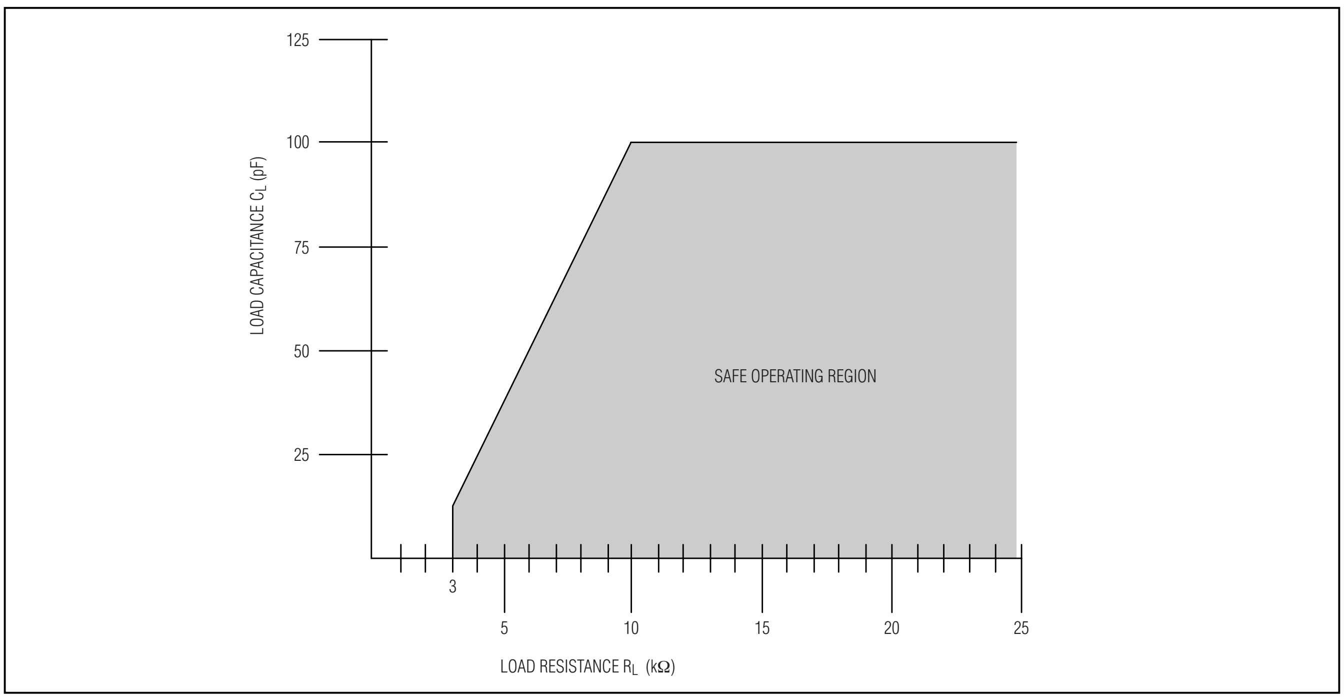


Figure 3. Load-Impedance Operating Region

Integrated Analog Lowpass Filter

The DAC output of the sigma-delta modulator is followed by an analog smoothing filter that attenuates high-frequency quantization noise. The corner frequency of the filter is approximately 2 x f_S.

Integrated Analog Output Buffer

Following the analog lowpass filter, the analog signal is routed through internal buffers to OUTR and OUTL. The buffer can directly drive load resistances larger than 3kΩ and load capacitances up to 100pF (Figure 3).

Clock and Data Interface

The MAX5556–MAX5559 strobe serial data (SDATA) in on the rising edge of SCLK. LRCLK routes data to the left or right outputs and, along with SCLK, defines the number of bits per sample transferred. The digital interpolators filter data at internal clock rates derived from the MCLK frequency. Each device supports both internal and external serial clock (SCLK) modes.

SDATA Input

The serial interface strobes data (SDATA) in on the rising edge of SCLK, MSB first. The MAX5556–MAX5559 support four different data formats, as detailed in Figures 4–7.

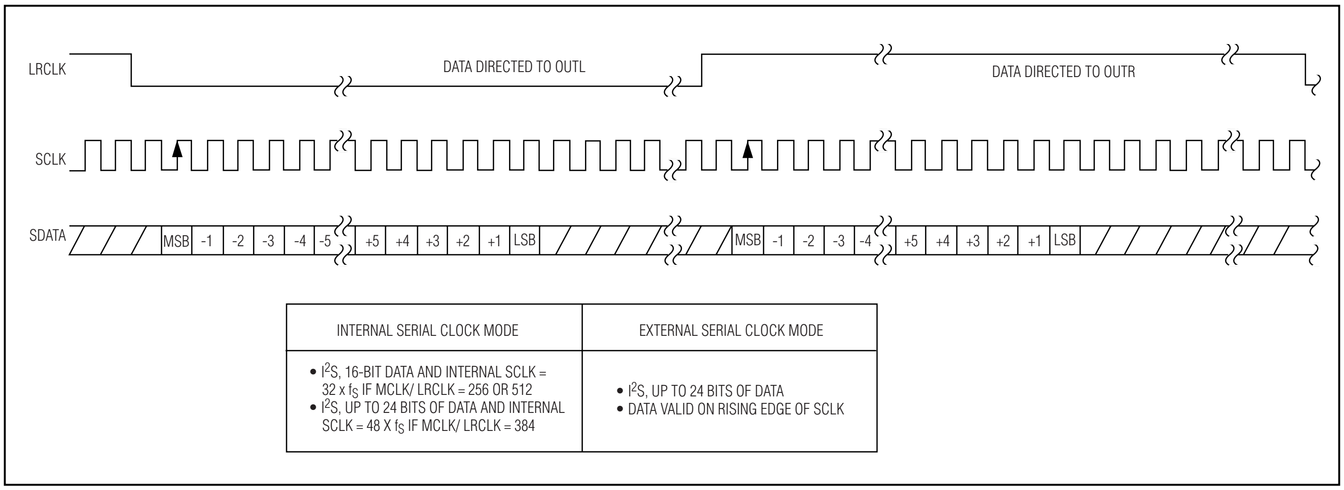


Figure 4. MAX5556 Data Format Timing

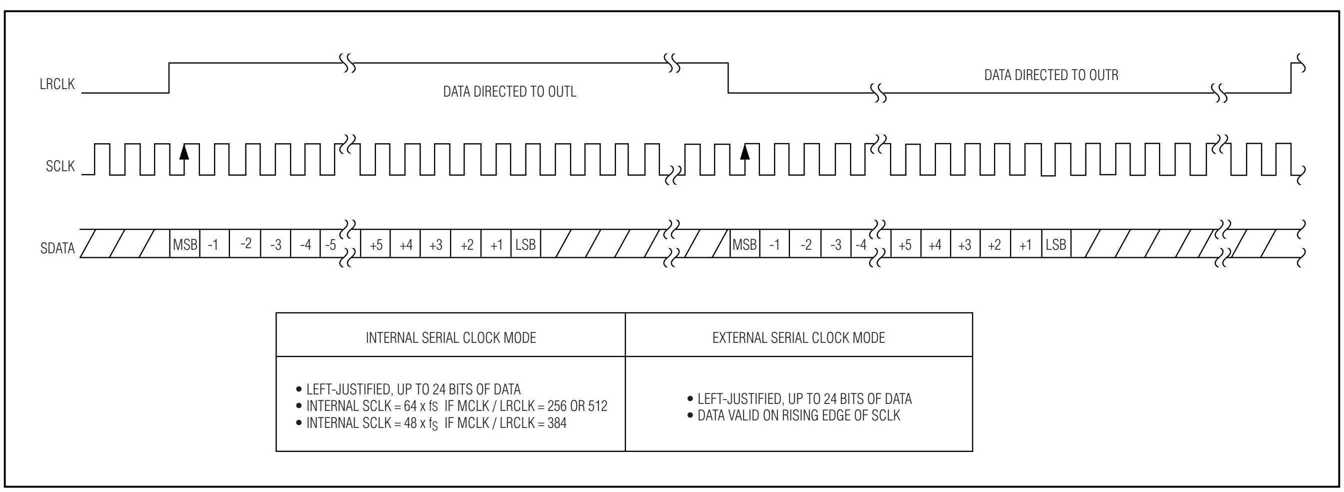
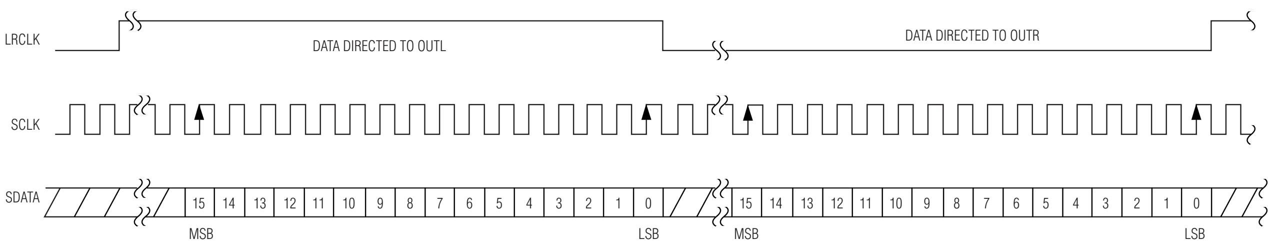


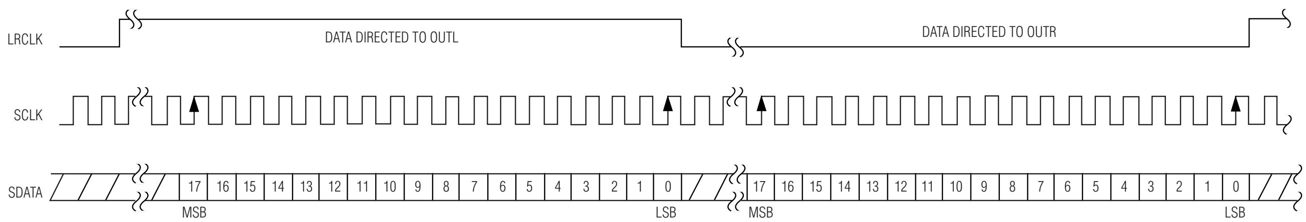
Figure 5. MAX5557 Data Format Timing

Low-Cost Stereo Audio DACs



INTERNAL SERIAL CLOCK MODE	EXTERNAL SERIAL CLOCK MODE
• RIGHT-JUSTIFIED, 16-BIT DATA • INTERNAL SCLK = 32 x fS IF MCLK / LRCLK = 256 OR 512 • INTERNAL SCLK = 48 x f_S IF MCLK / LRCLK = 384	• RIGHT-JUSTIFIED, 16-BIT DATA • DATA VALID ON RISING EDGE OF SCLK • SCLK MUST HAVE AT LEAST 32 CYCLES PER LRCLK PERIOD

Figure 6. MAX5558 Data Format Timing



INTERNAL SERIAL CLOCK MODE	EXTERNAL SERIAL CLOCK MODE
• RIGHT-JUSTIFIED, 18-BIT DATA • INTERNAL SCLK = 64 x fS IF MCLK / LRCLK = 256 OR 512 • INTERNAL SCLK = 48 x f_S IF MCLK / LRCLK = 384	• RIGHT-JUSTIFIED, 18-BIT DATA • DATA VALID ON RISING EDGE OF SCLK • SCLK MUST HAVE AT LEAST 36 CYCLES PER LRCLK PERIOD

Figure 7. MAX5559 Data Format Timing

Serial Clock (SCLK)

SCLK strobes the individual data bits at SDATA into the DAC. The MAX5556–MAX5559 operate in one of two modes: internal serial clock mode or external serial clock mode.

External SCLK Mode

The MAX5556–MAX5559 operate in external serial clock mode when SCLK activity is detected. All four devices return to internal serial clock mode if no SCLK signal is detected for one LRCLK period. Figure 8 details the external serial clock mode timing parameters.

Internal SCLK Mode

The MAX5556–MAX5559 transition from external serial clock mode to internal serial clock mode if no SCLK signal is detected for one LRCLK period. In internal clock mode, SCLK is derived from and is synchronous with MCLK and LRCLK (operation in internal clock mode is identical to an external clock mode when LRCLK is synchronized with MCLK). Figure 9 details the internal serial clock mode timing parameters. Figure 10 details the generation of the internal clock.

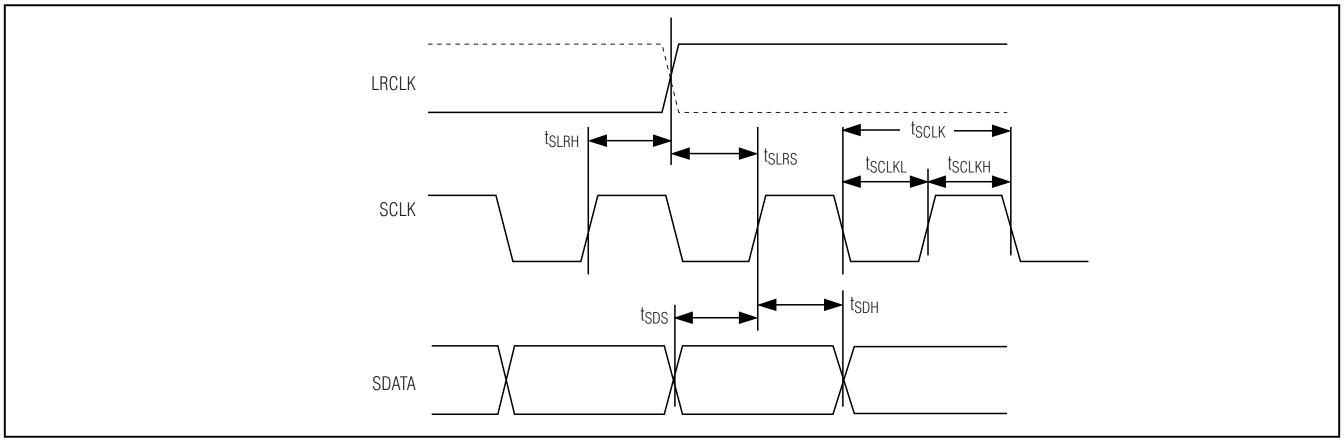


Figure 8. External SCLK Serial Timing Diagram

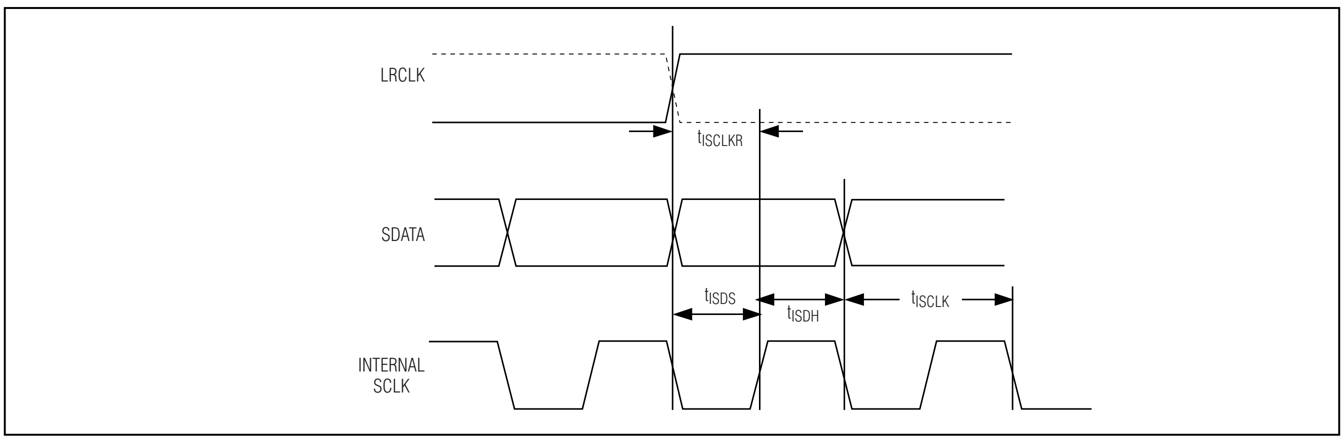


Figure 9. Internal SCLK Serial Timing Diagram

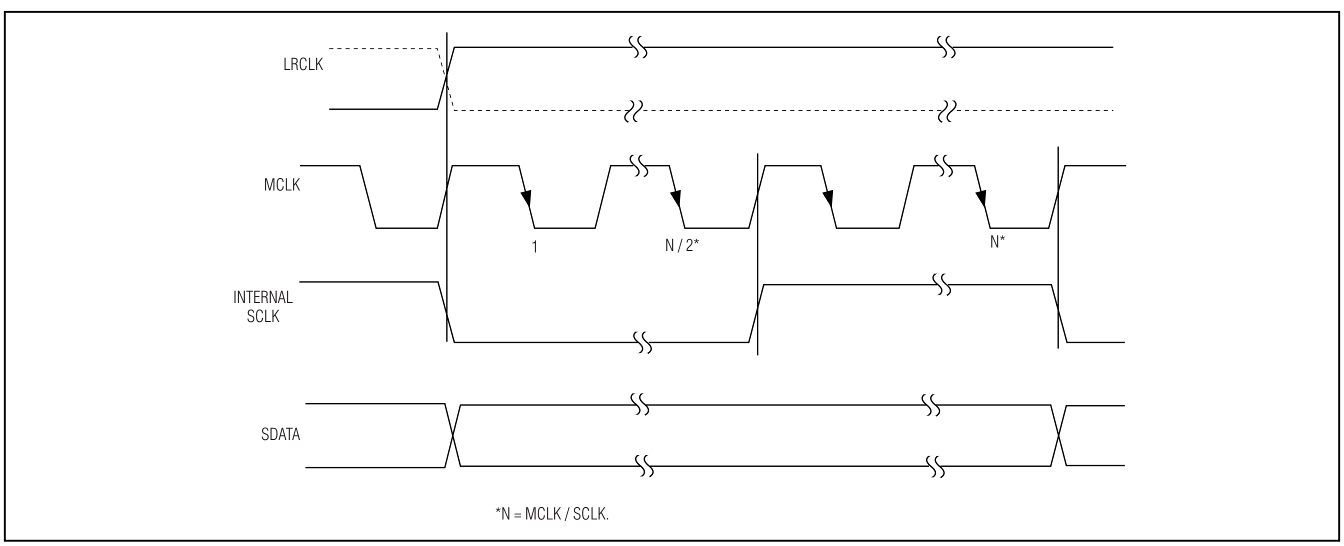


Figure 10. Internal Serial Clock Generation

Left/Right Clock Input (LRCLK)

LRCLK is the left/right clock input signal for the 3-wire interface and sets the sample frequency (f_S). On the MAX5556, drive LRCLK low to direct data to OUTL or LRCLK high to direct data to OUTR (Figure 4). On the MAX5557/MAX5558/MAX5559, drive LRCLK high to direct data to OUTL or LRCLK low to direct data to OUTR (Figures 5, 6, 7). LRCLK is internally resampled on each SCLK rising edge. The MAX5556–MAX5559 accept data at LRCLK audio sample rates from 2kHz to 50kHz.

Master Clock (MCLK)

MCLK accepts the master clock signal from an external clocking device and is used to derive internal clock frequencies. Set the MCLK/LRCLK ratio to 256, 384, or 512 to achieve the internal serial clock frequencies listed in Table 1. Table 2 details the MCLK/LRCLK ratios for three sample audio rates.

The MAX5556–MAX5559 detect the MCLK/LRCLK ratio during the initialization sequence by counting the number of MCLK transitions during a single LRCLK period. MCLK, SCLK, and LRCLK must be synchronous signals.

Table 1. Internal and External Clock Frequencies

PART	INTERNAL SERIAL CLOCK FREQUENCY		EXTERNAL SERIAL CLOCK FREQUENCY
	MCLK/LRCLK = 256 OR 512	MCLK/LRCLK = 384	
MAX5556	32 x f_S	48 x f_S	User defined (Figure 4)
MAX5557	64 x f_S	48 x f_S	User defined (Figure 5)
MAX5558	32 x f_S	48 x f_S	User defined (Figure 6)
MAX5559	64 x f_S	48 x f_S	User defined (Figure 7)

Table 2. MCLK/LRCLK Ratios

LRCLK (kHz)	MCLK (MHz)		
	MCLK/LRCLK = 256	MCLK/LRCLK = 384	MCLK/LRCLK = 512
32	8.1920	12.2880	16.3840
44.1	11.2896	16.9344	22.5792
48	12.2880	18.4320	24.5760

Data Formats

MAX5556 I²S Left-Justified Data Format

The MAX5556 accepts data with an I²S left-justified data format, accepting up to 24 bits of data. SDATA accepts data in two's complement format with the MSB first. The MSB is valid on the second SCLK rising edge after LRCLK transitions low to high or high to low (Figure 4). Drive LRCLK low to direct data to OUTL. Drive LRCLK high to direct data to OUTR. The number of SCLK pulses with LRCLK high or low determines the number of bits transferred per sample. If fewer than 24 bits of data are written, the remaining LSBs are set to 0. If more than 24 bits are written, any bits after the LSB are ignored.

The MAX5556 accepts up to 24 bits of data in external serial clock mode or when the MCLK/LRCLK ratio is 384 (internal serial clock = 48 x f_S) in internal serial clock mode. The DAC also accepts 16 bits of data in internal serial clock mode when the MCLK/LRCLK ratio is 256 or 512 (internal serial clock = 32 x f_S).

MAX5557 Left-Justified Data Format

The MAX5557 accepts data with a left-justified data format, allowing for up to 24 bits of data. SDATA accepts data in two's complement format with the MSB first. The MSB is valid on the first SCLK rising edge after LRCLK transitions low to high or high to low (Figure 5). Drive LRCLK high to direct data to OUTL. Drive LRCLK low to direct data to OUTR. The number of SCLK pulses with LRCLK high or low determines the number of bits transferred per sample. If fewer than 24 bits of data are written, the remaining LSBs are set to 0. If more than 24 bits are written, the bits after the LSB are ignored.

The MAX5557 accepts up to 24 bits of data in external serial clock mode and internal serial clock mode. Program the MCLK/LRCLK ratio to 384 to operate the internal serial clock at 48 x f_S. Program the MCLK/LRCLK ratio to 256 or 512 to operate the internal serial clock at 64 x f_S.

MAX5558 16-Bit Right-Justified Data Format

The MAX5558 operates from a 16-bit right-justified data format. The LSB is valid on the final SCLK rising edge prior to LRCLK transitioning low to high or high to low (Figure 6). In external serial clock mode, the MAX5558 requires a minimum of 32 SCLK cycles per LRCLK period (16 SCLK cycles with LRCLK low and 16 SCLK cycles with LRCLK high). Drive LRCLK high to direct data to OUTL. Drive LRCLK low to direct data to OUTR. Any additional SDATA bits prior to the MSB are ignored.

The MAX5558 accepts 16 bits of data in external serial clock mode and internal serial clock mode. Program the MCLK/LRCLK ratio to 384 to operate the internal serial clock at 48 x f_S. Program the MCLK/LRCLK ratio to 256 or 512 to operate the internal serial clock at 32 x f_S.

MAX5559 18-Bit Right-Justified Data Format

The MAX5559 accepts data with an 18-bit right-justified data format. The LSB is valid on the final SCLK rising edge prior to LRCLK transitioning low to high or high to low (Figure 7). In external serial clock mode, the MAX5559 requires a minimum of 36 SCLK cycles per LRCLK period (18 SCLK cycles with LRCLK low and 18 SCLK cycles with LRCLK high). Drive LRCLK high to direct data to OUTL. Drive LRCLK low to direct data to OUTR. Any additional SDATA bits prior to the MSB are ignored.

The MAX5559 accepts 18 bits of data in external serial clock mode and internal serial clock mode. Program the MCLK/LRCLK ratio to 384 to operate the internal serial clock at 48 x f_S. Program the MCLK/LRCLK ratio to 256 or 512 to operate the internal serial clock at 64 x f_S.

External Analog Filter

Use an external lowpass analog filter to further reduce harmonic images, noise, and spurs. The external analog filter can be either active or passive depending upon performance and design requirements. For example filters, see Figures 11 and 12 and the *Applications Information* section. Careful attention should be paid when selecting capacitors for audio signal path applications. NPO and C0G types are recommended as are aluminum electrolytics and some tantalum varieties. Use of generic ceramic types is not recommended and may result in degraded THD performance. Always consult manufacturers' data sheets and applications information.

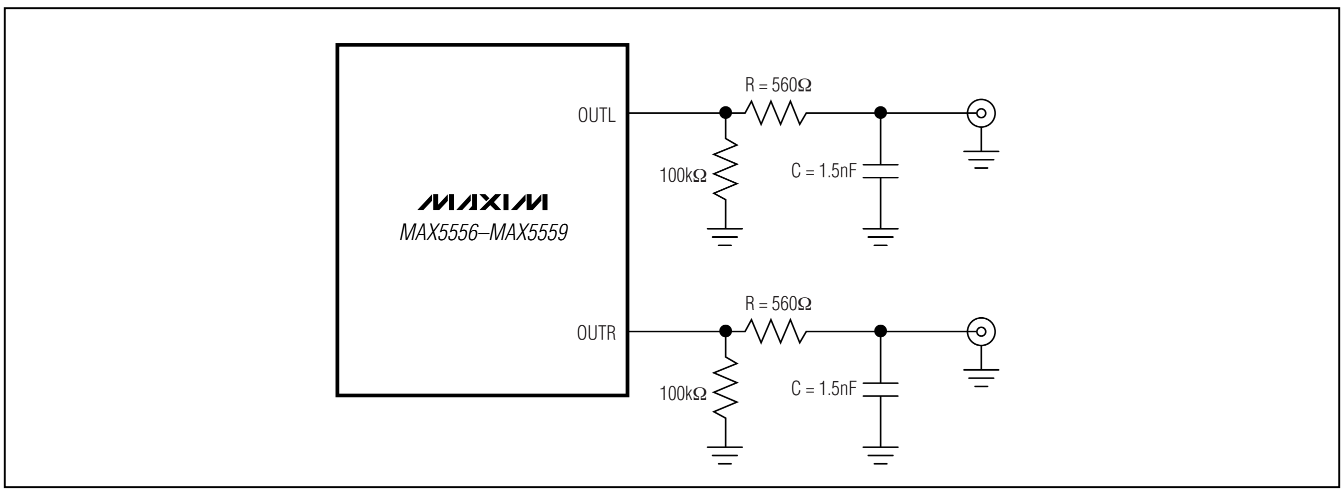


Figure 11. Passive Component Analog Output Filter

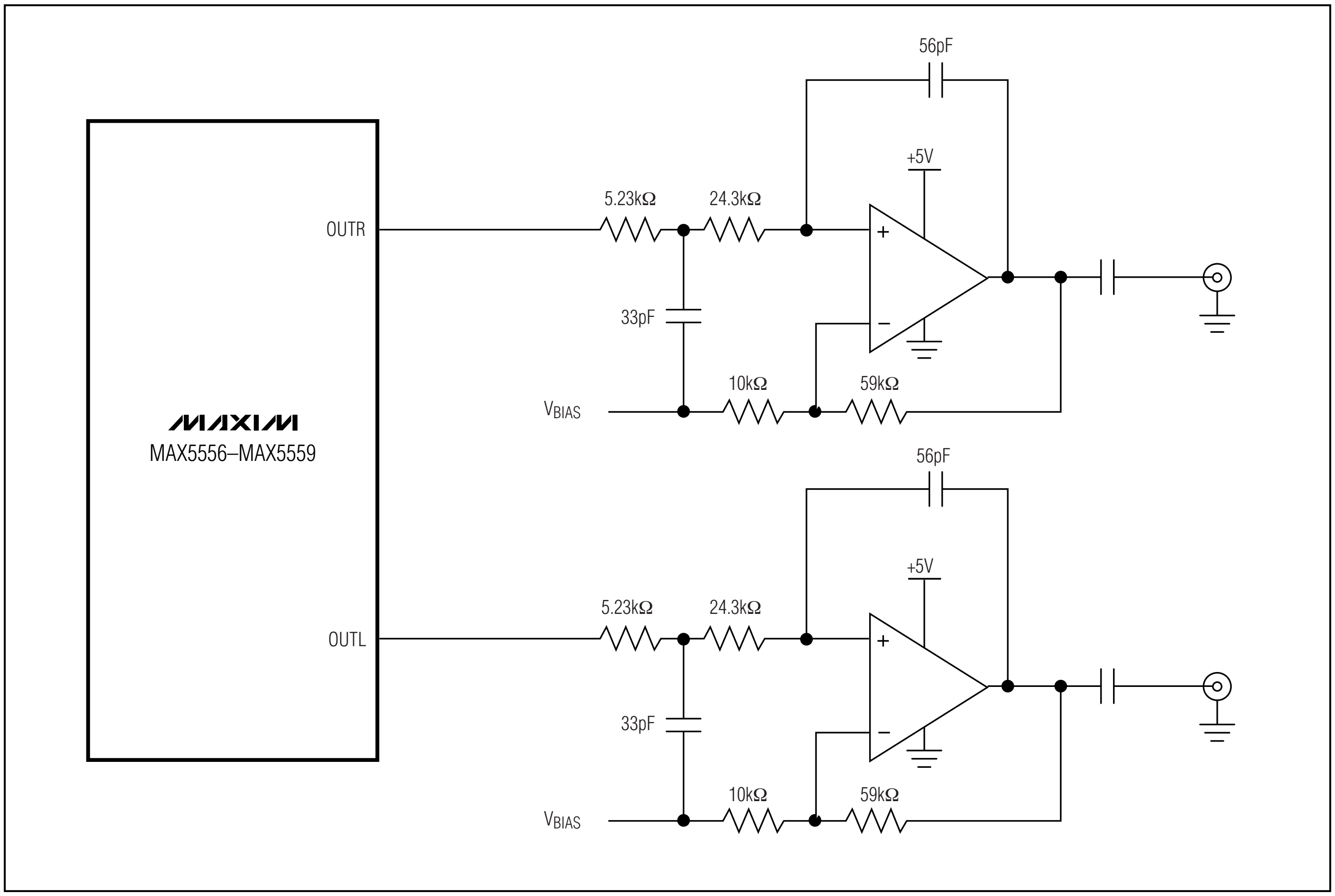


Figure 12. Active Component Analog Output Filter

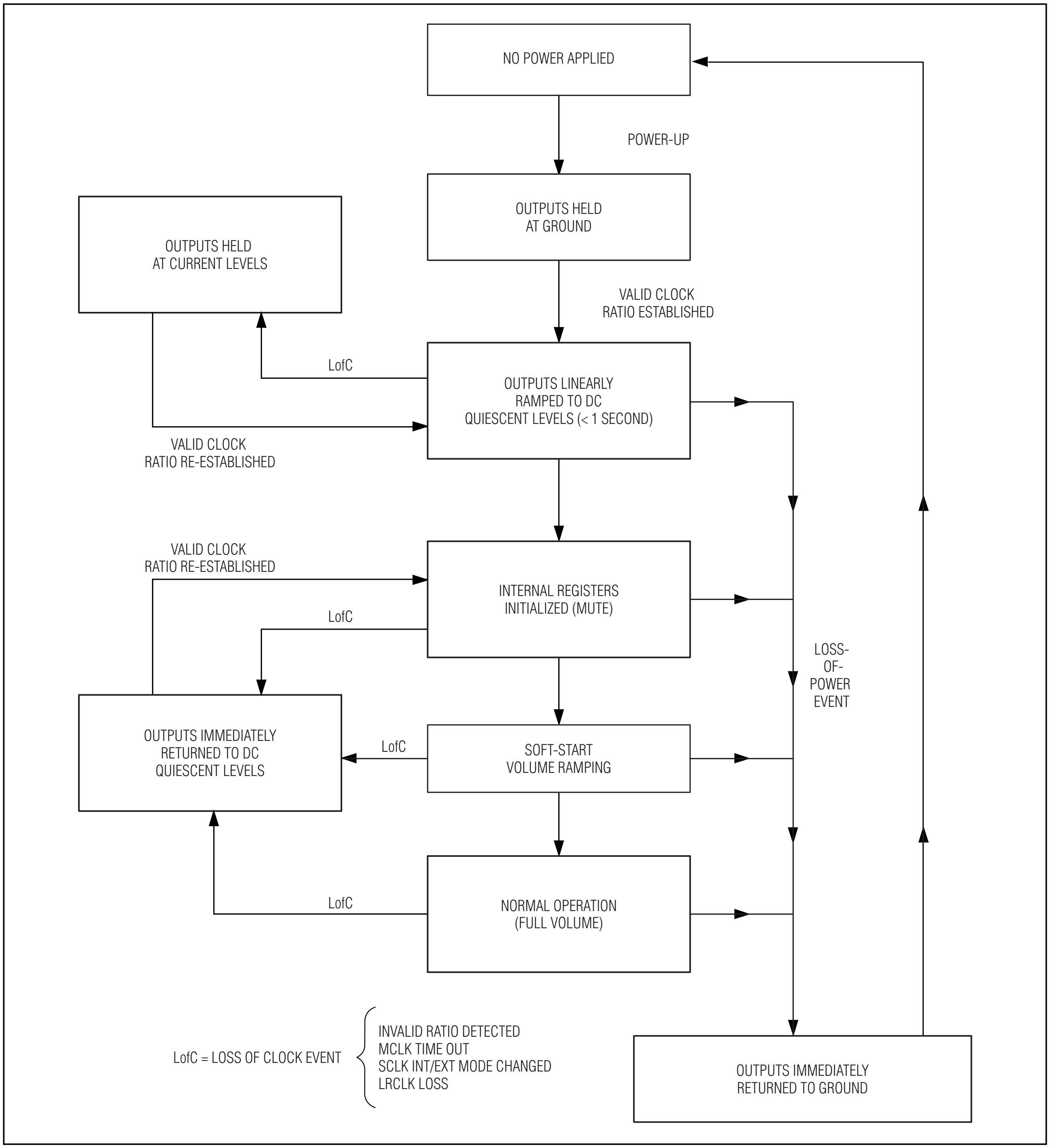


Figure 13. Internal State Diagram

Pop and Click Suppression

The MAX5556–MAX5559 feature a pop and click supression routine to reduce the unwanted audible effects of system transients. This routine produces glitch-free operation at the outputs during power-on, loss of clock, or invalid clock conditions. See Figure 13 for a detailed state diagram during transient conditions.

Power-Up

Once the MAX5556–MAX5559 recognize a valid MCLK/LRCLK ratio (256, 384, or 512), the analog outputs (OUTR and OUTL) are enabled in stages using a glitchless ramping routine. First, the outputs ramp up to the quiescent output voltage at a rate of 5V/s typ (see Figure 14). After the outputs reach the quiescent voltage, the converted data stream begins soft-start ramping, achieving the full-scale operation over a 20ms period.

If invalid clock signals are detected while the outputs are DC ramping to their quiescent state, the outputs stop ramping and hold their preset values until valid clock signals are restored (Figure 15).

Loss of Clock and Invalid Clock Conditions

The MAX5556–MAX5559 mute both outputs after detecting one of four invalid clock conditions. All four devices mute their outputs to prevent propagation of pops, clicks, or corrupted data through the signal path. The MAX5556–MAX5559 force the outputs to the quiescent DC voltage (2.4V) to prevent clicks in capacitive-coupled systems. Invalid clock conditions include:

1. MCLK/LRCLK ratio changes between 256, 384, and 512
2. Transition between internal and external serial-clock mode
3. Invalid MCLK/LRCLK ratio
4. MCLK falls below the minimum operating frequency 2kHz

When the MCLK/LRCLK ratio returns to 256, 384, or 512 and MCLK is equal or greater than its minimum operating frequency, the MAX5556–MAX5559 outputs return to their full-scale setting over a soft-start mute time of 20ms (Figure 15).

Power-Down

When the positive supply is removed from the MAX5556–MAX5559, the outputs discharge to ground. When power is restored, the power-up ramp routine engages once a valid clock ratio is established (see the *Power-Up* section).

Avoid violating absolute maximum conditions by supplying digital inputs to the part or forcing voltages on the analog outputs during a loss-of-power event.

Applications Information

Low-Cost Line-Level Solution

Connect the MAX5556–MAX5559 outputs through a passive output filter as detailed in Figure 11 for a low-cost solution. This lowpass filter yields single-pole (20dB/decade) roll-off at a corner frequency (f_C) determined by:

$$f_C = \frac{1}{2\pi RC}$$

In the case of Figure 11, f_C is approximately 190kHz.

High-Performance Line-Level Solution

For enhanced performance, connect the MAX5556–MAX5559 outputs to an active filter by using an operational amplifier as shown in Figure 12. The use of an active filter allows for steeper roll-off, more efficient filtering, and also adds the capability of a programmable output gain.

Power-Supply Sequencing

For correct power-up sequencing, apply V_{DD} and then connect the input digital signals. Do not apply digital signals before V_{DD} is applied.

Do not violate any of the absolute maximum ratings by removing power with the digital inputs still connected. To correctly power down the device, first disconnect the digital input signals, and then remove V_{DD}.

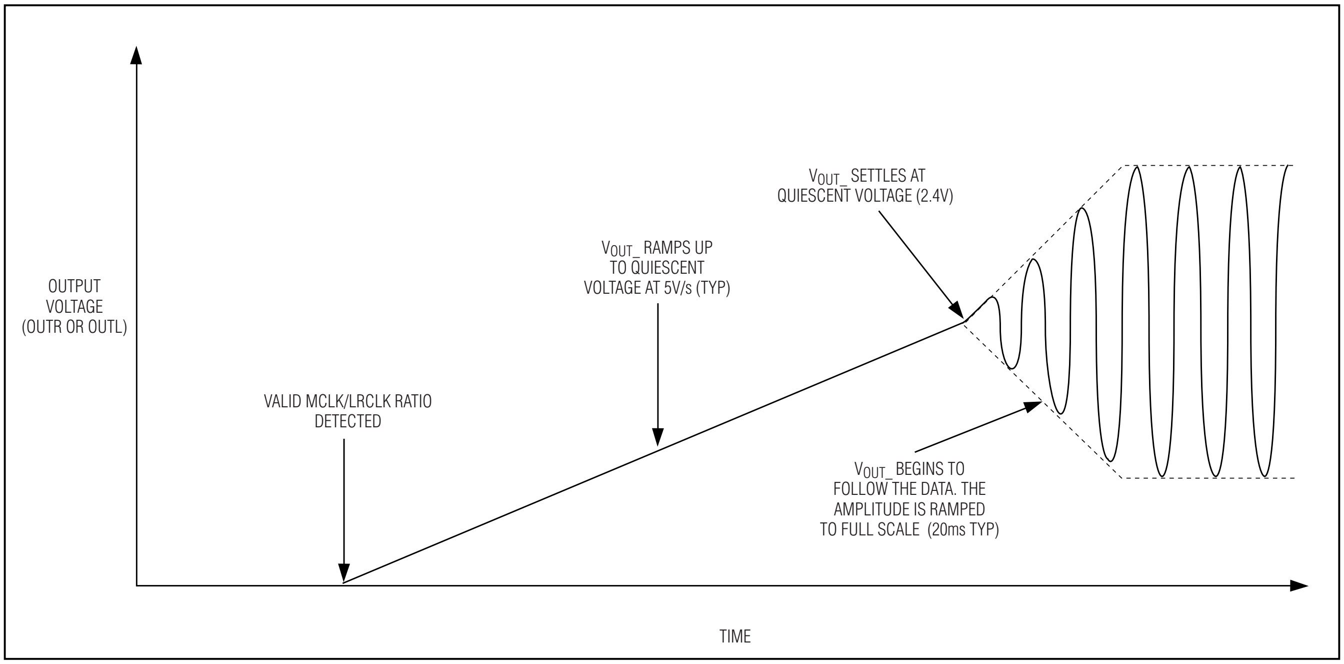


Figure 14. Power-Up Sequence

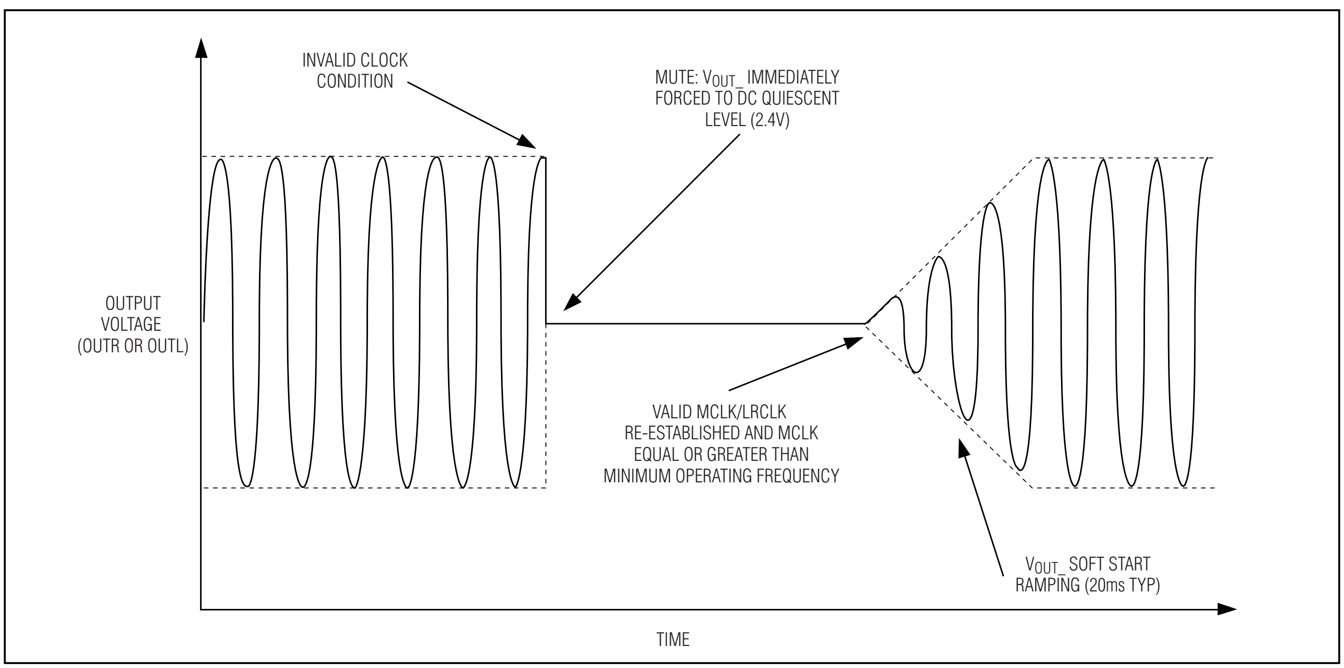


Figure 15. Invalid Clock Output Response

Power-Supply Connections and Ground Management

Proper layout and grounding are essential for optimum performance. Use large traces for the power-supply inputs and analog outputs to minimize losses due to parasitic trace resistance. Large traces also aid in moving heat away from the package. Proper grounding improves audio performance, minimizes crosstalk between channels, and prevents any switching noise from coupling into the audio signal. Route the analog paths (GND, V_{DD}, OUTL, and OUTR) away from the digital signals. Connect a 0.1µF capacitor in parallel with a 4.7µF capacitor as close to V_{DD} as possible. Low ESR-type capacitors are recommended for supply decoupling applications. A small value C0G-type bypass capacitor located as close to the device as possible is recommended in parallel with larger values.

Chip Information

PROCESS: BiCMOS

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

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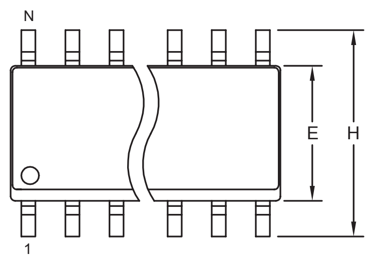
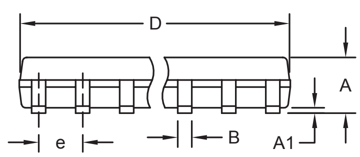


TOP VIEW

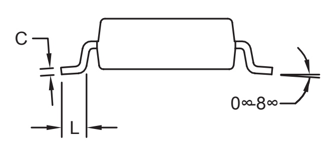
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050 BSC		1.27 BSC	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27

VARIATIONS:

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	N	MS012
D	0.189	0.197	4.80	5.00	8	AA
D	0.337	0.344	8.55	8.75	14	AB
D	0.386	0.394	9.80	10.00	16	AC



FRONT VIEW



SIDE VIEW

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. LEADS TO BE COPLANAR WITHIN 0.10mm (.004").
4. CONTROLLING DIMENSION: MILLIMETERS.
5. MEETS JEDEC MS012.
6. N = NUMBER OF PINS.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, .150" SOIC

APPROVAL | DOCUMENT CONTROL NO. 21-0041 | REV. B | 1/1