SONY

CXG7003FN

Power Amplifier/Antenna Switch + Low Noise Down Conversion Mixer for PHS

Description

The CXG7003FN is a MMIC consisting of the power amplifier, diversity antenna supported switch and low noise down conversion mixer.

This IC is designed using the Sony's GaAs J-FET process featuring a single positive power supply operation.

Features

- Operates at a single positive power supply: V_{DD} = 3V
- Diversity antenna supported switch
- Small mold package: 26-pin HSOF

<Power amplifier/antenna switch transmitter block >

- Low current consumption: I_{DD} = 150mA
  (P_{OUT} = 20.2dBm, f = 1.9GHz)
- High power gain: Gp = 40dB Typ.
  (P_{OUT} = 20.2dBm, f = 1.9GHz)

<Antenna switch receiver block/ low noise down conversion mixer>

- Low current consumption: I_{DD} = 5.5mA Typ.
  (When no signal)
- High conversion gain: Gc = 19.5dB Typ. (f = 1.9GHz)
- Low distortion: Input IP3 = –12dBm Typ. (f = 1.9GHz)
- High image suppression ratio: IMR = 40dBc Typ.
  (f = 1.9GHz)
- High 1/2 IF suppression ratio: 1/2IFR = 47dBc Typ.
  (f = 1.9GHz)

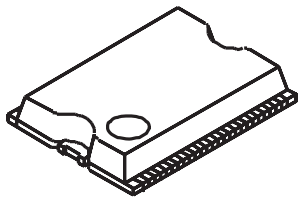
Applications

Digital cordless telephones (PHS)

Structure

GaAs J-FET MMIC

26 pin HSOF (Plastic)



Absolute Maximum Ratings

<Power amplifier block>

• Supply voltage	V_{DD}	6	V
• Voltage between gate and source	V_{GSO}	1.5	V
• Drain current	I_{DD}	550	mA
• Allowable power dissipation	P_D	3	W

<Switch block>

• Control voltage	V_{CTL}	6	V

<Front-end block>

• Supply voltage	V_{DD}	6	V
• Input power	P_{RF}	10	dBm

<Common to each block>

• Channel temperature	Tch	150	°C
• Operating temperature	Topr	–35 to +85	°C
• Storage temperature	Tstg	–65 to +150	°C

Recommended Operating Conditions

<Common to each block>

• Supply voltage	V_{DD}	2.7 to 3.3	V

<Switch block>

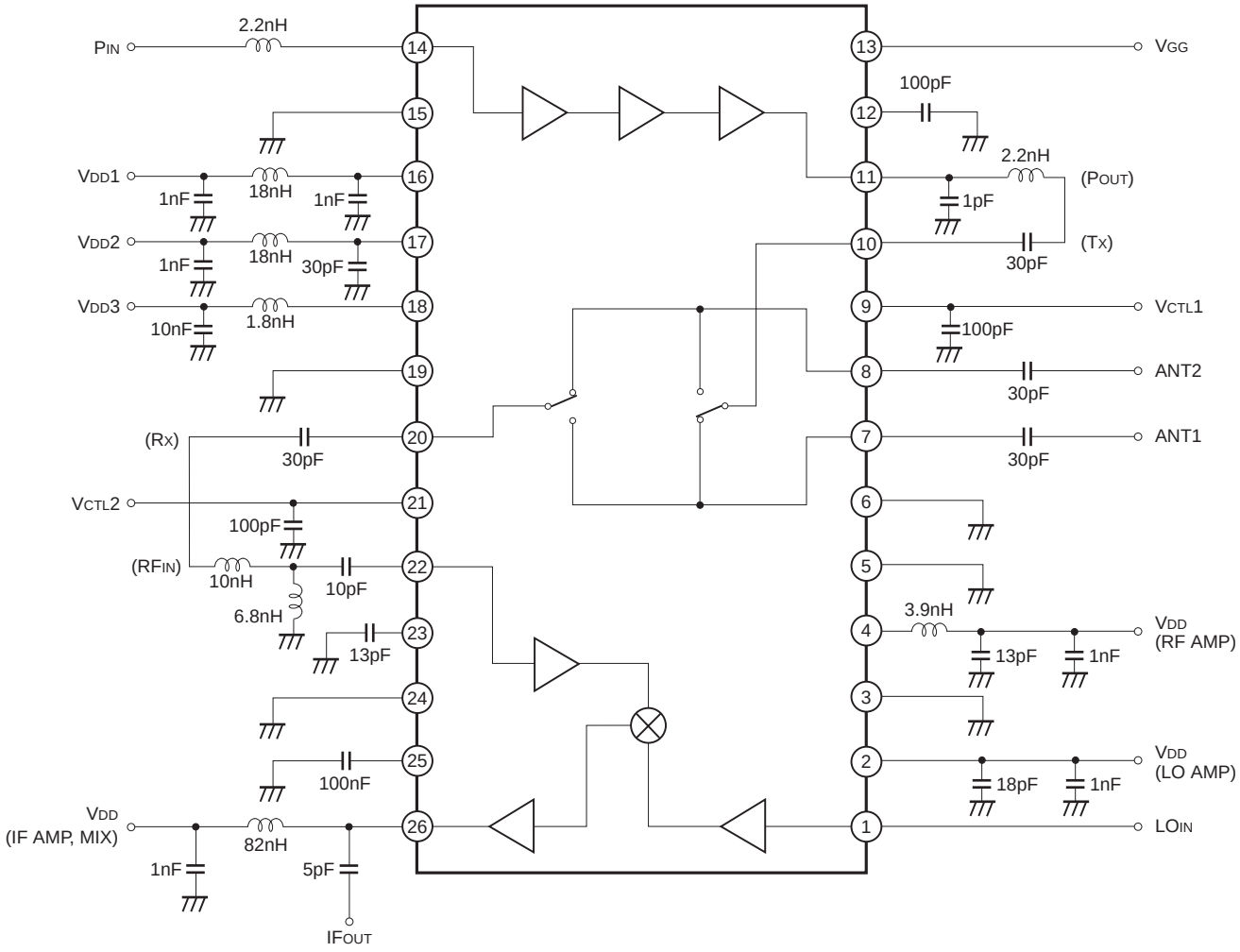
• Control voltage (H)	V_{CTL} (H)	2.9 to 3.3	V
• Control voltage (L)	V_{CTL} (L)	0 to 0.2	V

Notes on Handling

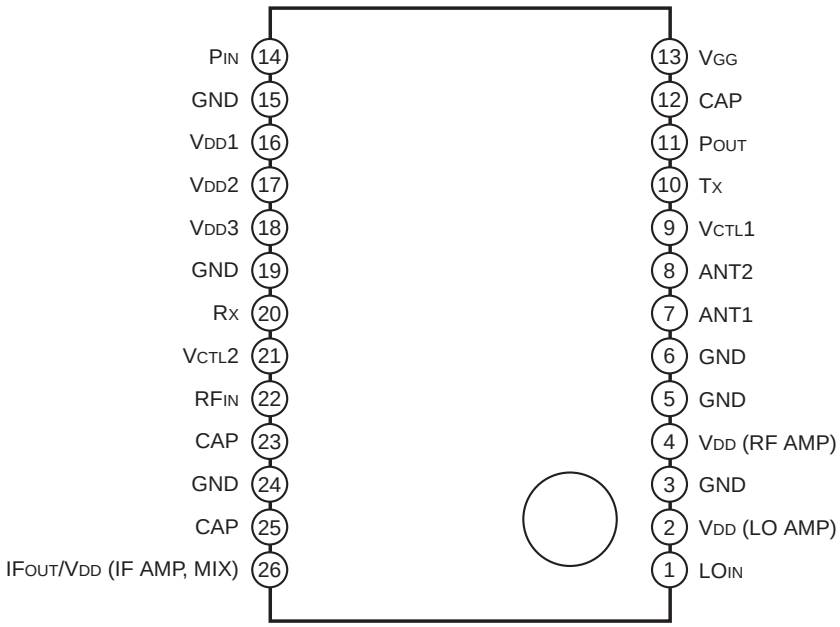
GaAs MMICs are ESD sensitive devices. Special handling precautions are required.

E04401-PS

Block Diagram and External Circuit



Pin Configuration



Pin Description

Pin No.	Symbol	Description
1	LO_{IN}	Local signal input pin
2	V_{DD} (LO AMP)	V_{DD} pin of local amplifier
3	GND	GND pin
4	V_{DD} (RF AMP)	V_{DD} pin of RF amplifier
5	GND	GND pin
6	GND	GND pin
7	ANT1	Antenna switch pin. This pin is ANT1-Tx or ANT1-Rx by setting of $V_{CTL}1$ and $V_{CTL}2$.
8	ANT2	Antenna switch pin. This pin is ANT2-Tx or ANT2-Rx by setting of $V_{CTL}1$ and $V_{CTL}2$.
9	$V_{CTL}1$	Antenna switch control 1 pin
10	T_X	Tx pin. Signal is input to antenna switch during ANT-Tx.
11	P_{OUT}	Power amplifier output pin
12	CAP	Connection pin of external capacitor (for noise elimination)
13	V_{GG}	Gate voltage adjustment pin of power amplifier (first stage, middle stage, rear-end FET)
14	P_{IN}	Signal input pin to power amplifier
15	GND	GND pin
16	$V_{DD}1$	$V_{DD}1$ pin of power amplifier (first stage FET)
17	$V_{DD}2$	$V_{DD}2$ pin of power amplifier (middle stage FET)
18	$V_{DD}3$	$V_{DD}3$ pin of power amplifier (rear-end FET)
19	GND	GND pin
20	R_X	Rx pin. ANT input signal is output to this pin during ANT1-Rx or ANT2-Rx.
21	$V_{CTL}2$	Antenna switch control 2 pin
22	RF_{IN}	RF signal input pin
23	CAP	External capacitor connection pin. This pin is connected to LNA FET source. RF amplifier characteristic is optimized during 1.9GHz by the capacitor of 13pF (Typ.).
24	GND	GND pin
25	CAP	External capacitor connection pin. IF amplifier distortion is improved by this capacitor.
26	IF_{OUT}/V_{DD} (IF AMP, MIX)	IF output and IF AMP, MIX V_{DD}

Electrical Characteristics

These specifications are when the Sony's recommended evaluation board shown on page 8 is used.

1. Control Pin Logic for Antenna Switch

Conditions of control pins	ANT1 – T_X ANT2 – R_X	ANT2 – T_X ANT1 – R_X
$V_{CTL}1$ = 3V, $V_{CTL}2$ = 0V	ON	OFF
$V_{CTL}1$ = 0V, $V_{CTL}2$ = 3V	OFF	ON

2. Power Amplifier Block + Antenna Switch Transmitter Block

These specifications are common to the ANT1 transmission and ANT2 transmission.

Unless otherwise specified: V_{DD} = 3V, I_{DD} = 150mA, P_{OUT} = 20.2dBm, f = 1.9GHz

When ANT1 transmission: $V_{CTL}1$ = 3V, $V_{CTL}2$ = 0V

When ANT2 transmission: $V_{CTL}1$ = 0V, $V_{CTL}2$ = 3V

(Ta = 25°C)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Current consumption	I_{DD}			150		mA
Gate voltage adjustment value	V_{GG}		0.04		0.6	V
Output power	P_{OUT}	Measured with the ANT pin	20.2			dBm
Power gain	G_P		36	40		dB
Adjacent channel leak power ratio (600 ± 100kHz)	ACPR600kHz	Measured with the ANT pin		–63	–55	dBc
Adjacent channel leak power ratio (900 ± 100kHz)	ACPR900kHz	Measured with the ANT pin		–70	–60	dBc
Occupied bandwidth	OBW	Measured with the ANT pin		250	275	kHz
2nd-order harmonic level	—	Measured with the ANT pin			–25	dBc
3rd-order harmonic level	—	Measured with the ANT pin			–25	dBc

3. Antenna Switch Receiver Block + Low Noise Down Conversion Mixer Block

These specifications are common to the ANT1 reception and ANT2 reception.

Unless otherwise specified: V_{DD} = 3V, RF1 = 1.90GHz/–35dBm, LO = 1.66GHz/–15dBm
When ANT1 reception: $V_{CTL}1$ = 0V, $V_{CTL}2$ = 3V
When ANT2 reception: $V_{CTL}1$ = 3V, $V_{CTL}2$ = 0V

(Ta = 25°C)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Current consumption	I_{DD}	When no signal		5.5	7.5	mA
Conversion gain	G_C	When a small signal	17	19.5		dB
Noise figure	NF	When a small signal		4.4	5.5	dB
Input IP3	IIP3	*1	–17	–12		dBm
Image suppression ratio	IMR	RF2 = 1.42GHz/–35dBm	25	40		dBc
1/2 IF suppression ratio	1/2IFR	RF2 = 1.78GHz/–35dBm	41	47		dBc
2 × LO–IF suppression ratio	—	RF2 = 3.08GHz/–35dBm	39	45		dBc
2 × LO+IF suppression ratio	—	RF2 = 3.56GHz/–35dBm	34	65		dBc
LO to ANT leak	P_{LK}			–50	–40	dBm

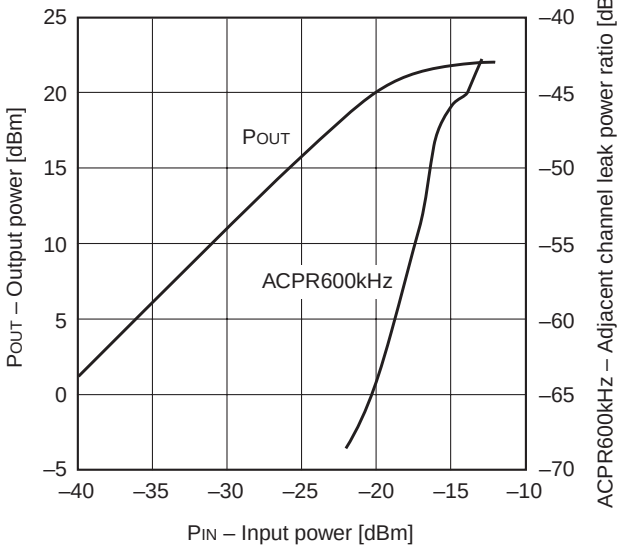
*1 Conversion from IM3 suppression ratio during RF1 = 1.9000GHz/–35dBm and RF2 = 1.9006GHz/–35dBm input.

Example of Representative Characteristics

1. Power Amplifier + Antenna Switch Transmitter Block (f = 1.9GHz, Ta = 25°C)

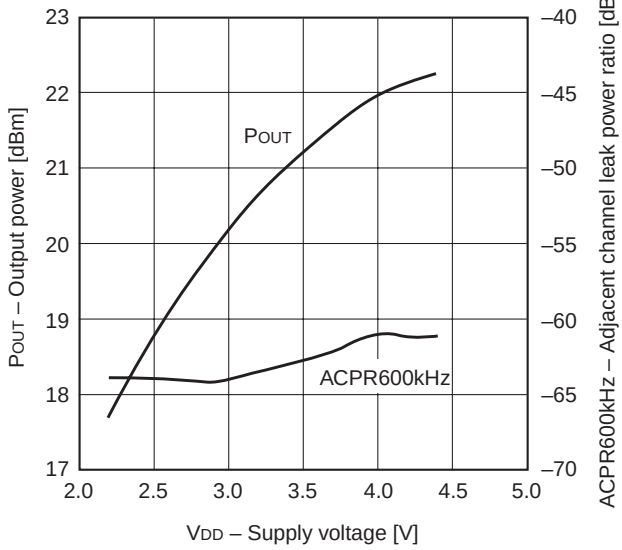
POUT, ACPR600kHz vs. PIN

V_{DD} = 3V, V_{GG} = const.,
I_{DD} = 150mA (@P_{OUT} = 20.2dBm),
P_{IN} = var.
When ANT1 transmission: $V_{CTL}1$ = 3V, $V_{CTL}2$ = 0V
When ANT2 transmission: $V_{CTL}1$ = 0V, $V_{CTL}2$ = 3V
The data shown below is common to ANT1 and ANT2.



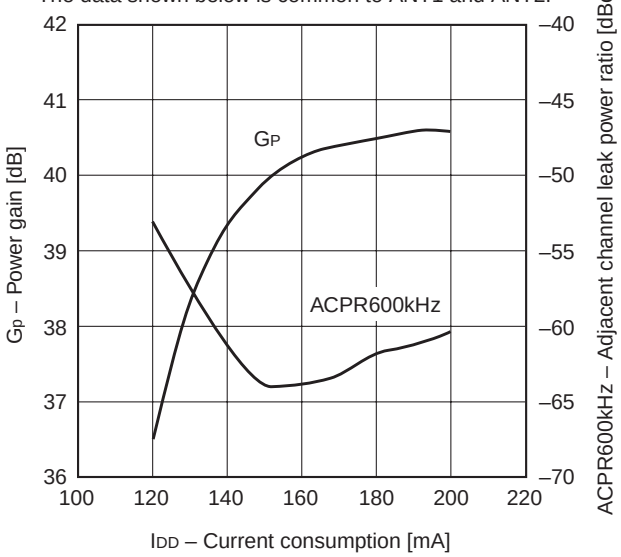
POUT, ACPR600kHz vs. VDD

V_{DD} = var., V_{GG} = const.,
I_{DD} = 150mA (@V_{DD} = 3V, P_{OUT} = 20.2dBm),
P_{IN} = –19.7dBm
When ANT1 transmission: $V_{CTL}1$ = 3V, $V_{CTL}2$ = 0V
When ANT2 transmission: $V_{CTL}1$ = 0V, $V_{CTL}2$ = 3V
The data shown below is common to ANT1 and ANT2.



Gp, ACPR600kHz vs. IDD

V_{DD} = 3V, V_{GG} = var., I_{DD} = var., P_{IN} = var.,
P_{OUT} = 20.2dBm
When ANT1 transmission: $V_{CTL}1$ = 3V, $V_{CTL}2$ = 0V
When ANT2 transmission: $V_{CTL}1$ = 0V, $V_{CTL}2$ = 3V
The data shown below is common to ANT1 and ANT2.

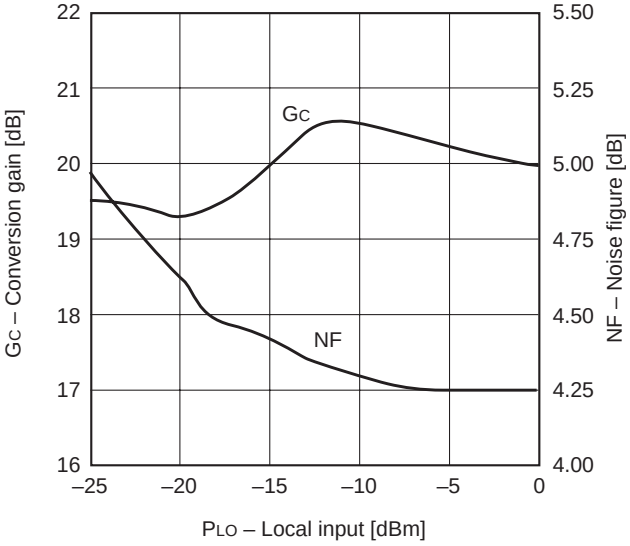


2. Antenna Switch Receiver Block + Low Noise Down Conversion Mixer (Ta = 25°C)

GC, NF vs. PLO

V_{DD} = 3V, RF1 = 1.90GHz/small signal,
LO = 1.66GHz
When ANT1 reception: $V_{CTL}1$ = 0V, $V_{CTL}2$ = 3V
When ANT2 reception: $V_{CTL}1$ = 3V, $V_{CTL}2$ = 0V

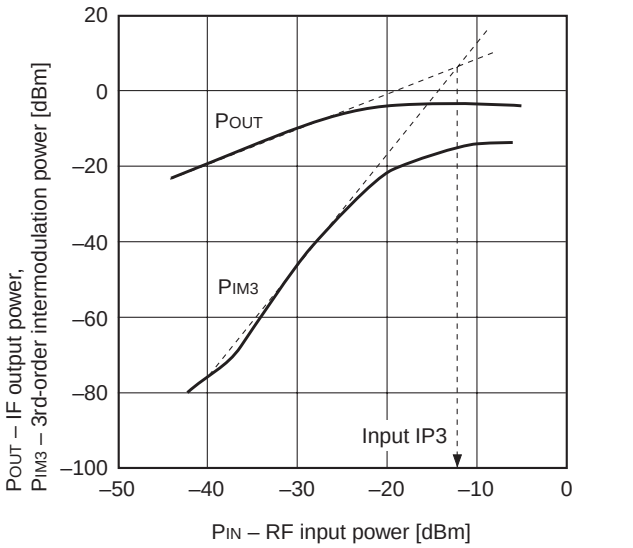
The data shown below is common to ANT1 and ANT2.



POUT, PIM3 vs. PIN

V_{DD} = 3V, RF1 = 1.9000GHz, RF2 = 1.9006GHz,
LO = 1.66GHz/–15dBm
When ANT1 reception: $V_{CTL}1$ = 0V, $V_{CTL}2$ = 3V
When ANT2 reception: $V_{CTL}1$ = 3V, $V_{CTL}2$ = 0V

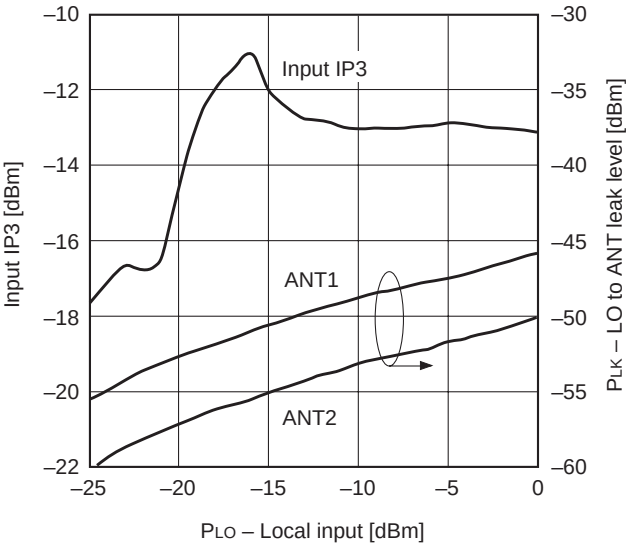
The data shown below is common to ANT1 and ANT2.



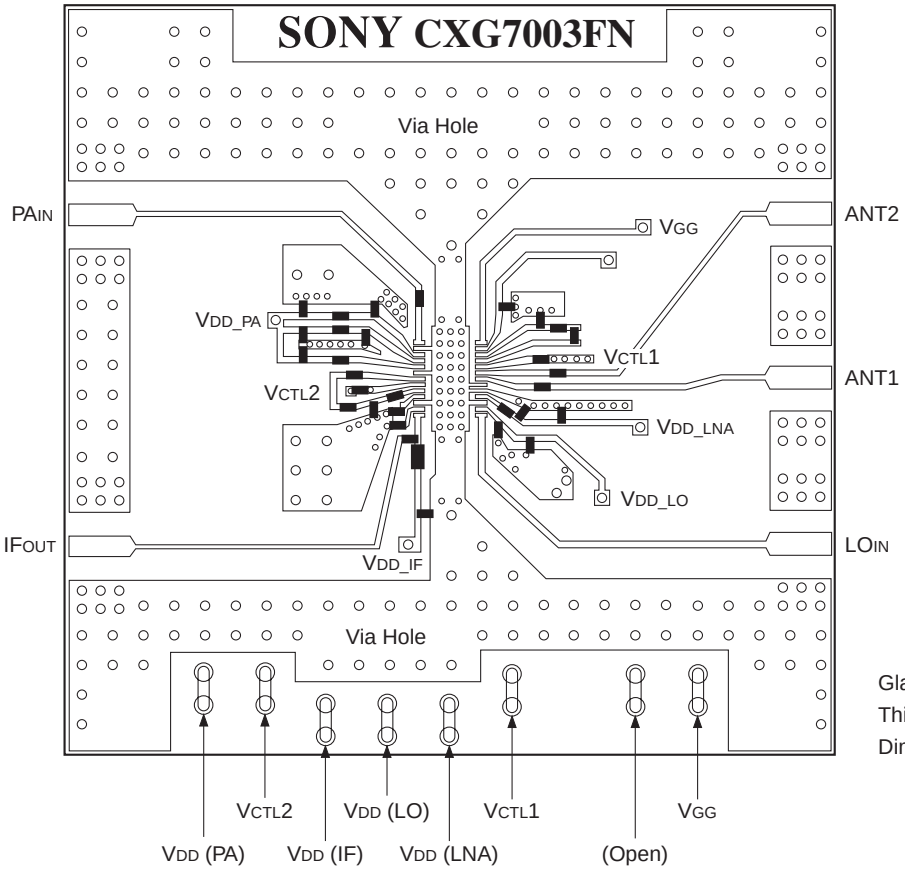
Input IP3, PLK vs. PLO

V_{DD} = 3V, RF = 1.90GHz/–35dBm,
LO = 1.66GHz
When ANT1 reception: $V_{CTL}1$ = 0V, $V_{CTL}2$ = 3V
When ANT2 reception: $V_{CTL}1$ = 3V, $V_{CTL}2$ = 0V

Input IP3 is common to ANT1 and ANT2.

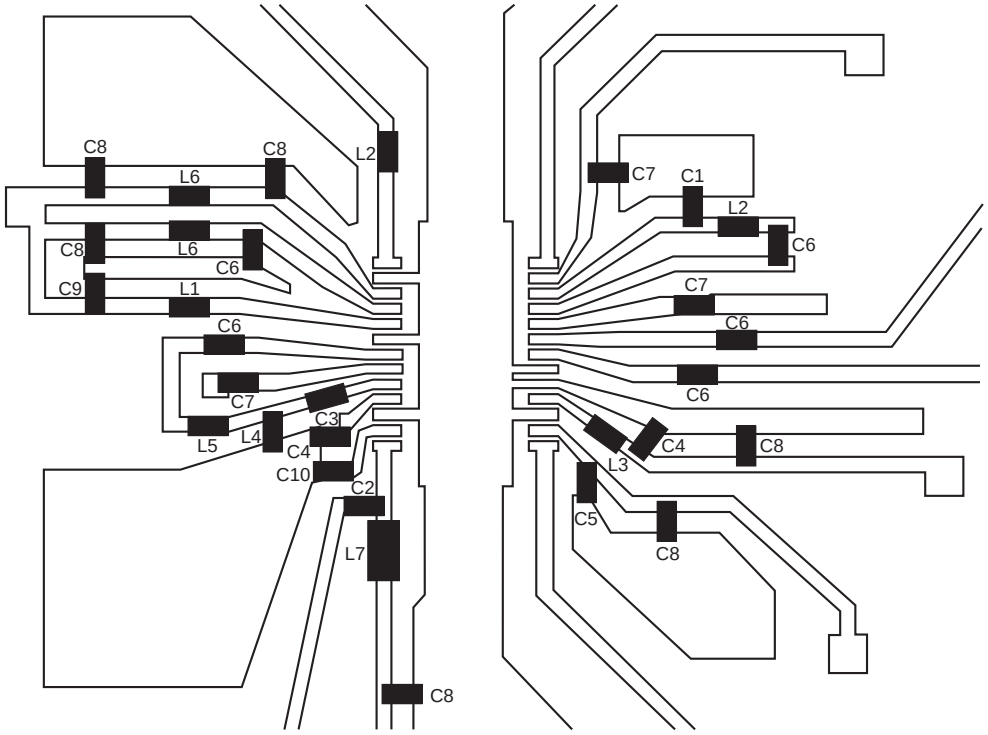


Recommended Evaluation Board



Glass fabric-base epoxy board (4 layers)
Thickness between layers 1 and 2: 0.2mm
Dimensions: 50mm × 50mm

Enlarged Diagram of External Circuit Block

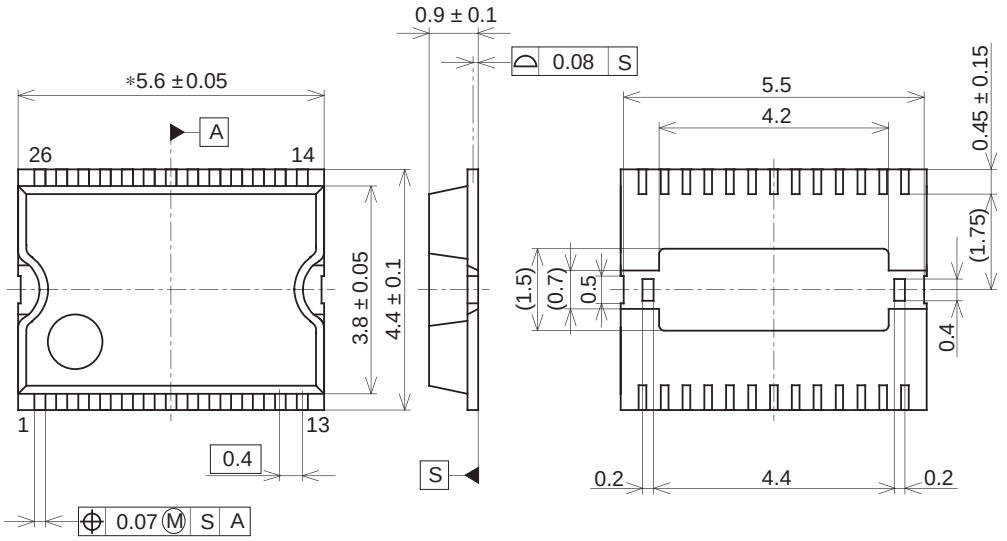


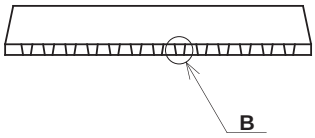
L1 = 1.8nH
L2 = 2.2nH
L3 = 3.9nH
L4 = 6.8nH
L5 = 10nH
L6 = 18nH
L7 = 82nH

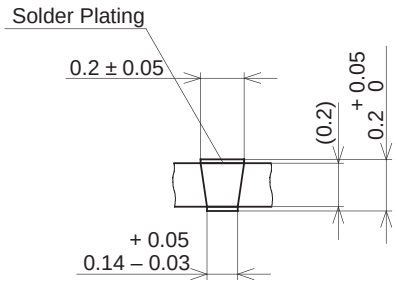
C1 = 1pF
C2 = 5pF
C3 = 10pF
C4 = 13pF
C5 = 18pF
C6 = 30pF
C7 = 100pF
C8 = 1nF
C9 = 10nF
C10 = 100nF

Package Outline Unit: mm

HSOF 26PIN (PLASTIC)







DETAIL **B**

NOTE: Dimension "∗" does not include mold protrusion.

SONY CODE	HSOF-26P-01
EIAJ CODE	————
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.06g

LEAD PLATING SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	COPPER ALLOY
SOLDER COMPOSITION	Sn-Bi Bi:1-4wt%
PLATING THICKNESS	5-18µm