1-/2-Channel 24-Bit µPower No Latency ΔΣ™ ADCs in MSOP-10

FEATURES

- **24-Bit ADCs in Tiny MSOP-10 Packages**
- **4ppm INL, No Missing Codes**
- **4ppm Full-Scale Error**
- **0.5ppm Offset**
- **0.6ppm Noise**
- **Single Conversion Settling Time for Multiplexed Applications**
- 1- or 2-Channel Inputs
- Automatic Channel Selection (Ping-Pong) (LTC2402)
- Zero Scale and Full Scale Set for Reference and Ground Sensing
- Internal Oscillator—No External Components Required
- 110dB Min, 50Hz/60Hz Notch Filter
- Reference Input Voltage: 0.1V to V_{CC}
- Live Zero—Extended Input Range Accommodates 12.5% Overrange and Underrange
- Single Supply 2.7V to 5.5V Operation
- Low Supply Current (200µA) and Auto Shutdown

APPLICATIONS

- Weight Scales
- Direct Temperature Measurement
- Gas Analyzers
- Strain Gauge Transducers
- Instrumentation
- Data Acquisition
- Industrial Process Control

DESCRIPTION

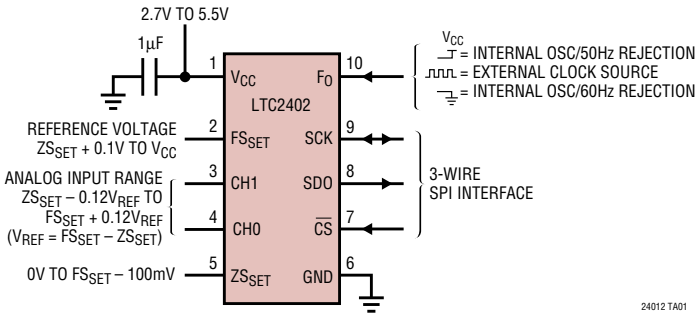
The LTC®2401/LTC2402 are 1- and 2-channel 2.7V to 5.5V micropower 24-bit analog-to-digital converters with an integrated oscillator, 4ppm INL and 0.6ppm RMS noise. These ultrasmall devices use delta-sigma technology and a new digital filter architecture that settles in a single cycle. This eliminates the latency found in conventional ΔΣ converters and simplifies multiplexed applications.

Through a single pin, the LTC2401/LTC2402 can be configured for better than 110dB rejection at 50Hz or 60Hz ±2%, or can be driven by an external oscillator for a user defined rejection frequency in the range 1Hz to 120Hz. The internal oscillator requires no external frequency setting components.

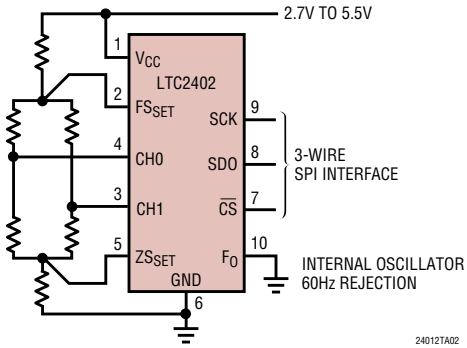
These converters accept an external reference voltage from 0.1V to V_{CC}. With an extended input conversion range of –12.5% V_{REF} to 112.5% V_{REF} (V_{REF} = FS_{SET} – ZS_{SET}), the LTC2401/LTC2402 smoothly resolve the offset and overrange problems of preceding sensors or signal conditioning circuits.

The LTC2401/LTC2402 communicate through a 2- or 3-wire digital interface that is compatible with SPI and MICROWIRE™ protocols.

TYPICAL APPLICATION



Pseudo Differential Bridge Digitizer

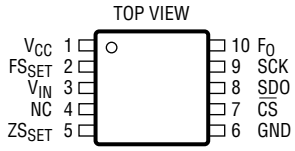


ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

Supply Voltage (V_{CC}) to GND ..... –0.3V to 7V
Analog Input Voltage to GND ..... –0.3V to (V_{CC} + 0.3V)
Reference Input Voltage to GND .. –0.3V to (V_{CC} + 0.3V)
Digital Input Voltage to GND ..... –0.3V to (V_{CC} + 0.3V)
Digital Output Voltage to GND ..... –0.3V to (V_{CC} + 0.3V)

Operating Temperature Range
LTC2401/LTC2402C ..... 0°C to 70°C
LTC2401/LTC2402I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

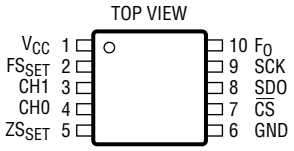
PACKAGE/ORDER INFORMATION



MS10 PACKAGE
10-LEAD PLASTIC MSOP

T_{JMAX} = 125°C, θ_{JA} = 130°C/W

ORDER PART NUMBER
LTC2401CMS LTC2401IMS
MS10 PART MARKING
LTMB LTMC



MS10 PACKAGE
10-LEAD PLASTIC MSOP

T_{JMAX} = 125°C, θ_{JA} = 130°C/W

ORDER PART NUMBER
LTC2402CMS LTC2402IMS
MS10 PART MARKING
LTMD LTME

Consult factory for Military grade parts.

CONVERTER CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{REF} = FS_{SET} – ZS_{SET}. (Notes 3, 4)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Resolution		●	24			Bits
No Missing Codes Resolution	0.1V ≤ FS_{SET} ≤ V_{CC}, ZS_{SET} = 0V (Note 5)	●	24			Bits
Integral Nonlinearity	FS_{SET} = 2.5V, ZS_{SET} = 0V (Note 6) FS_{SET} = 5V, ZS_{SET} = 0V (Note 6)	● ●		2 4	10 15	ppm of V_{REF} ppm of V_{REF}
Offset Error	2.5V ≤ FS_{SET} ≤ V_{CC}, ZS_{SET} = 0V	●		0.5	2	ppm of V_{REF}
Offset Error Drift	2.5V ≤ FS_{SET} ≤ V_{CC}, ZS_{SET} = 0V			0.01		ppm of V_{REF}/°C
Full-Scale Error	2.5V ≤ FS_{SET} ≤ V_{CC}, ZS_{SET} = 0V	●		4	10	ppm of V_{REF}
Full-Scale Error Drift	2.5V ≤ FS_{SET} ≤ V_{CC}, ZS_{SET} = 0V			0.04		ppm of V_{REF}/°C
Total Unadjusted Error	FS_{SET} = 2.5V, ZS_{SET} = 0V FS_{SET} = 5V, ZS_{SET} = 0V			5 10		ppm of V_{REF} ppm of V_{REF}
Output Noise	V_{IN} = 0V (Note 13)			3		μV_{RMS}
Normal Mode Rejection 60Hz ±2%	(Note 7)	●	110	130		dB
Normal Mode Rejection 50Hz ±2%	(Note 8)	●	110	130		dB
Power Supply Rejection, DC	FS_{SET} = 2.5V, ZS_{SET} = 0V, V_{IN} = 0V			100		dB
Power Supply Rejection, 60Hz ±2%	FS_{SET} = 2.5V, ZS_{SET} = 0V, V_{IN} = 0V, (Notes 7, 15)			110		dB
Power Supply Rejection, 50Hz ±2%	FS_{SET} = 2.5V, ZS_{SET} = 0V, V_{IN} = 0V, (Notes 8, 15)			110		dB

ANALOG INPUT AND REFERENCE

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{REF} = FS_{SET} – ZS_{SET}. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Input Voltage Range	(Note 14)	●	ZS_{SET} – 0.12V_{REF}		FS_{SET} + 0.12V_{REF}	V
FS_{SET}	Full-Scale Set Range		●	0.1 + ZS_{SET}		V_{CC}	V
ZS_{SET}	Zero-Scale Set Range		●	0		FS_{SET} – 0.1	V
$C_{S(IN)}$	Input Sampling Capacitance				10		pF
$C_{S(REF)}$	Reference Sampling Capacitance				15		pF
$I_{IN(LEAK)}$	Input Leakage Current	$\overline{CS}$ = V_{CC}	●	–10	1	10	nA
$I_{REF(LEAK)}$	Reference Leakage Current	V_{REF} = 2.5V, $\overline{CS}$ = V_{CC}	●	–12	1	12	nA

DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage $\overline{CS}$, F_O	2.7V ≤ V_{CC} ≤ 5.5V 2.7V ≤ V_{CC} ≤ 3.3V	●	2.5 2.0			V V
V_{IL}	Low Level Input Voltage $\overline{CS}$, F_O	4.5V ≤ V_{CC} ≤ 5.5V 2.7V ≤ V_{CC} ≤ 5.5V	●			0.8 0.6	V V
V_{IH}	High Level Input Voltage SCK	2.7V ≤ V_{CC} ≤ 5.5V (Note 9) 2.7V ≤ V_{CC} ≤ 3.3V (Note 9)	●	2.5 2.0			V V
V_{IL}	Low Level Input Voltage SCK	4.5V ≤ V_{CC} ≤ 5.5V (Note 9) 2.7V ≤ V_{CC} ≤ 5.5V (Note 9)	●			0.8 0.6	V V
I_{IN}	Digital Input Current $\overline{CS}$, F_O	0V ≤ V_{IN} ≤ V_{CC}	●	–10		10	µA
I_{IN}	Digital Input Current SCK	0V ≤ V_{IN} ≤ V_{CC} (Note 9)	●	–10		10	µA
C_{IN}	Digital Input Capacitance $\overline{CS}$, F_O				10		pF
C_{IN}	Digital Input Capacitance SCK	(Note 9)			10		pF
V_{OH}	High Level Output Voltage SDO	I_O = –800µA	●	V_{CC} – 0.5			V
V_{OL}	Low Level Output Voltage SDO	I_O = 1.6mA	●			0.4	V
V_{OH}	High Level Output Voltage SCK	I_O = –800µA (Note 10)	●	V_{CC} – 0.5			V
V_{OL}	Low Level Output Voltage SCK	I_O = 1.6mA (Note 10)	●			0.4	V
I_{OZ}	High-Z Output Leakage SDO		●	–10		10	µA

POWER REQUIREMENTS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	Supply Voltage		●	2.7		5.5	V
I_{CC}	Supply Current Conversion Mode Sleep Mode	 $\overline{CS}$ = 0V (Note 12) $\overline{CS}$ = V_{CC} (Note 12)	 ● ●		 200 20	 300 30	 µA µA

TIMING CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{EOSC}	External Oscillator Frequency Range		●	2.56		307.2	kHz
t_{HEO}	External Oscillator High Period		●	0.5		390	µs
t_{LEO}	External Oscillator Low Period		●	0.5		390	µs
t_{CONV}	Conversion Time	F_O = 0V F_O = V_{CC} External Oscillator (Note 11)	● ● ●	130.86 157.03 20510/f_{EOSC} (in kHz)	133.53 160.23	136.20 163.44	ms ms ms
f_{ISCK}	Internal SCK Frequency	Internal Oscillator (Note 10) External Oscillator (Notes 10, 11)		19.2 f_{EOSC}/8			kHz kHz
D_{ISCK}	Internal SCK Duty Cycle	(Note 10)		45		55	%
f_{ESCK}	External SCK Frequency Range	(Note 9)	●			2000	kHz
t_{LESCK}	External SCK Low Period	(Note 9)	●	250			ns
t_{HESCK}	External SCK High Period	(Note 9)	●	250			ns
t_{DOUT_ISCK}	Internal SCK 32-Bit Data Output Time	Internal Oscillator (Notes 10, 12) External Oscillator (Notes 10, 11)	● ●	1.64 256/f_{EOSC} (in kHz)	1.67	1.70	ms ms
t_{DOUT_ESCK}	External SCK 32-Bit Data Output Time	(Note 9)	●	32/f_{ESCK} (in kHz)			ms
t_1	$\overline{CS}$ ↓ to SDO Low Z		●	0		150	ns
t_2	$\overline{CS}$ ↑ to SDO High Z		●	0		150	ns
t_3	$\overline{CS}$ ↓ to SCK ↓	(Note 10)	●	0		150	ns
t_4	$\overline{CS}$ ↓ to SCK ↑	(Note 9)	●	50			ns
t_{KQMAX}	SCK ↓ to SDO Valid		●			200	ns
t_{KQMIN}	SDO Hold After SCK ↓	(Note 5)	●	15			ns
t_5	SCK Set-Up Before $\overline{CS}$ ↓		●	50			ns
t_6	SCK Hold After $\overline{CS}$ ↓		●			50	ns

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: All voltage values are with respect to GND.

Note 3: V_{CC} = 2.7 to 5.5V unless otherwise specified. Input source resistance = 0Ω.

Note 4: Internal Conversion Clock source with the F_O pin tied to GND or to V_{CC} or to external conversion clock source with f_{EOSC} = 153600Hz unless otherwise specified.

Note 5: Guaranteed by design, not subject to test.

Note 6: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 7: F_O = 0V (internal oscillator) or f_{EOSC} = 153600Hz ±2% (external oscillator).

Note 8: F_O = V_{CC} (internal oscillator) or f_{EOSC} = 128000Hz ±2% (external oscillator).

Note 9: The converter is in external SCK mode of operation such that the SCK pin is used as digital input. The frequency of the clock signal driving SCK during the data output is f_{ESCK} and is expressed in kHz.

Note 10: The converter is in internal SCK mode of operation such that the SCK pin is used as digital output. In this mode of operation, the SCK pin has a total equivalent load capacitance C_{LOAD} = 20pF.

Note 11: The external oscillator is connected to the F_O pin. The external oscillator frequency, f_{EOSC}, is expressed in kHz.

Note 12: The converter uses the internal oscillator. F_O = 0V or F_O = V_{CC}.

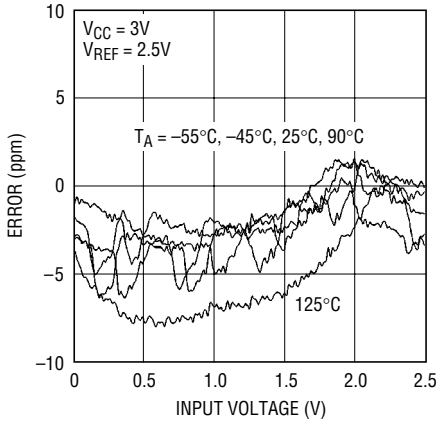
Note 13: The output noise includes the contribution of the internal calibration operations.

Note 14: V_{REF} = FS_{SET} – ZS_{SET}. The minimum input voltage is limited to –0.3V and the maximum to V_{CC} + 0.3V.

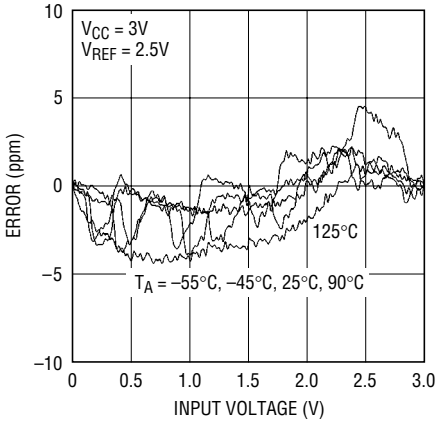
Note 15: V_{CC} (DC) = 4.1V, V_{CC} (AC) = 2.8V_{P-P}.

TYPICAL PERFORMANCE CHARACTERISTICS

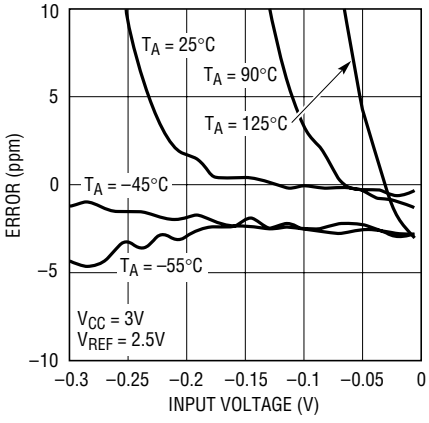
Total Unadjusted Error (3V Supply)



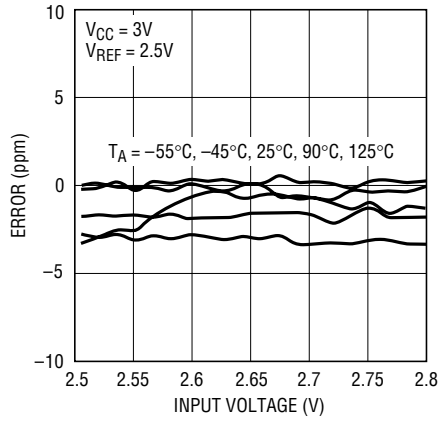
INL (3V Supply)



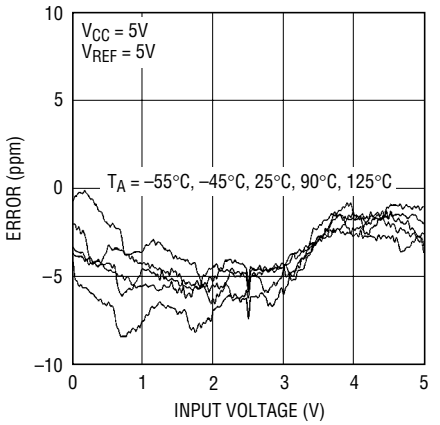
Negative Extended Input Range Total Unadjusted Error (3V Supply)



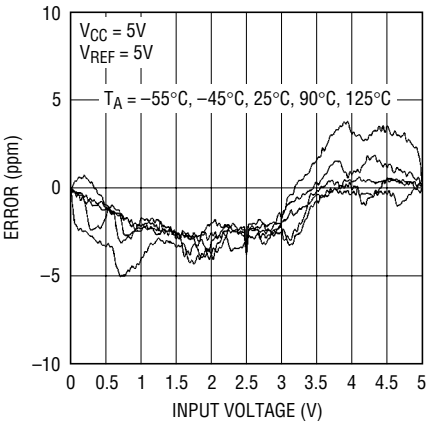
Positive Extended Input Range Total Unadjusted Error (3V Supply)



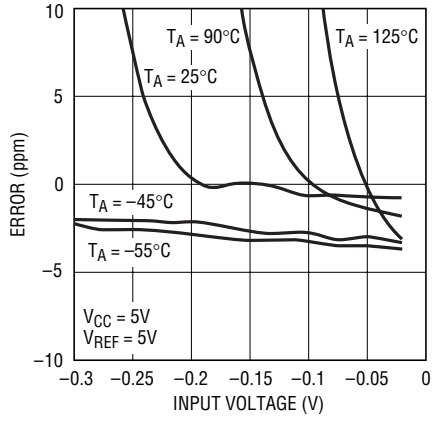
Total Unadjusted Error (5V Supply)



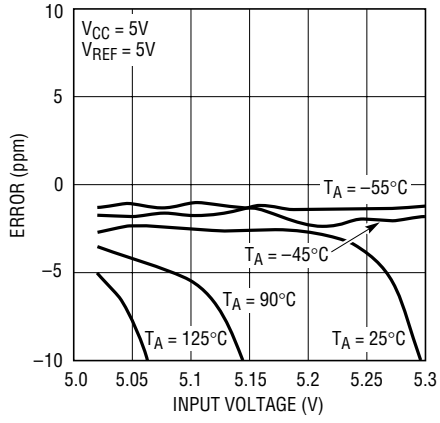
INL (5V Supply)



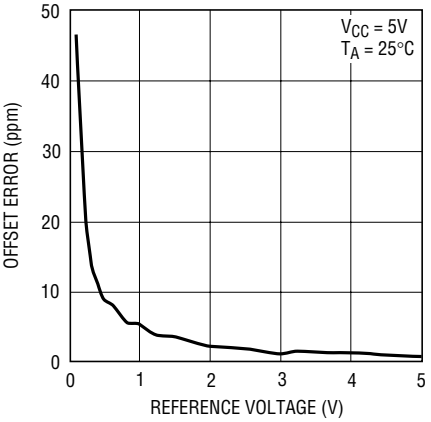
Negative Extended Input Range Total Unadjusted Error (5V Supply)



Positive Extended Input Range Total Unadjusted Error (5V Supply)

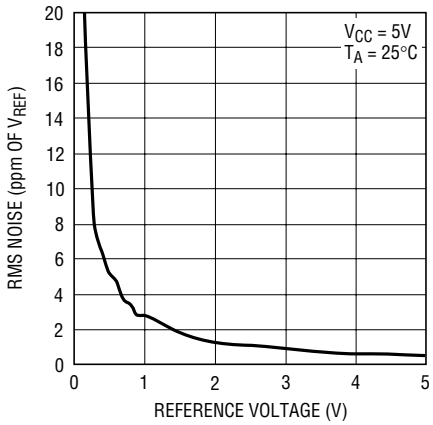


Offset Error vs Reference Voltage



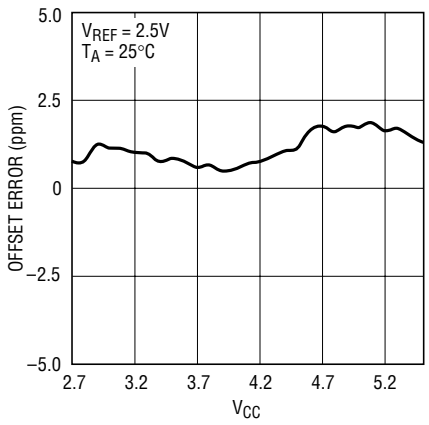
TYPICAL PERFORMANCE CHARACTERISTICS

RMS Noise vs Reference Voltage



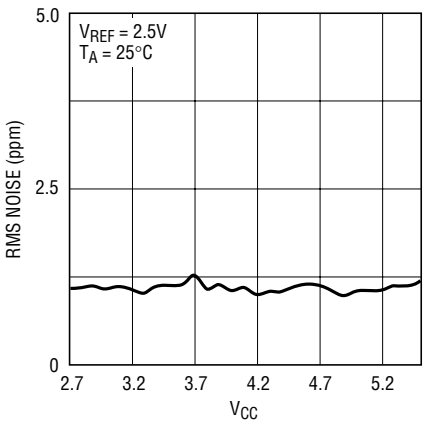
24012 G10

Offset Error vs V_{CC}



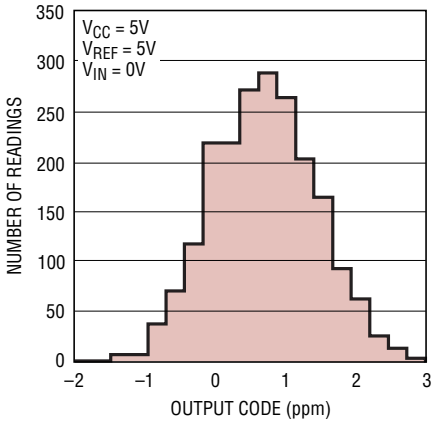
24012 G11

RMS Noise vs V_{CC}



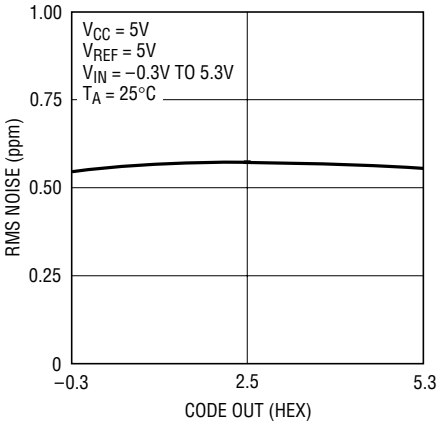
24012 G12

Noise Histogram



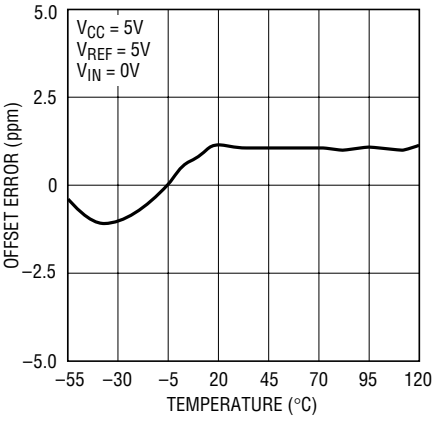
24012 G13

RMS Noise vs Code Out



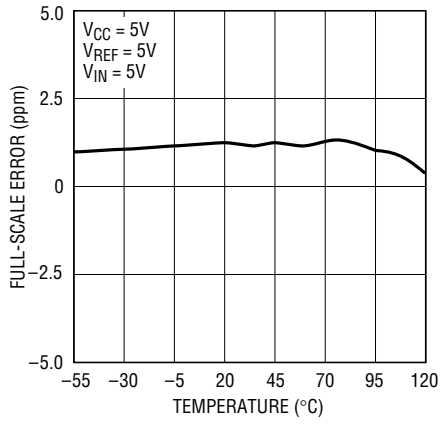
24012 G14

Offset Error vs Temperature



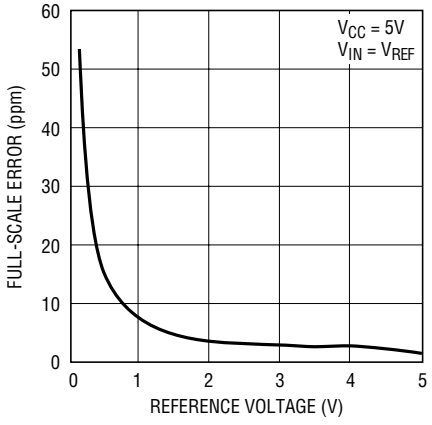
24012 G15

Full-Scale Error vs Temperature



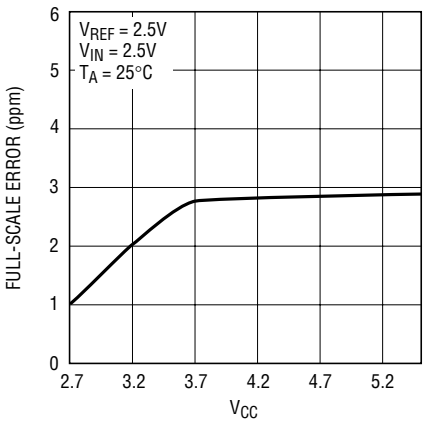
24012 G16

Full-Scale Error vs Reference Voltage



24012 G17

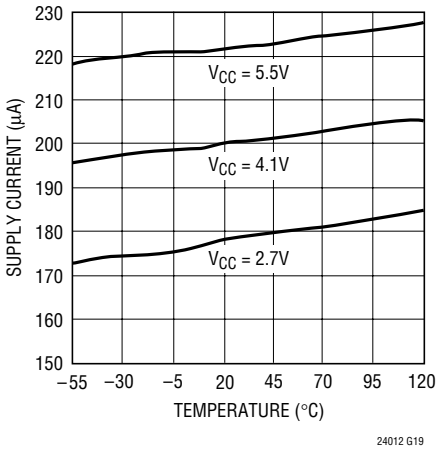
Full-Scale Error vs V_{CC}



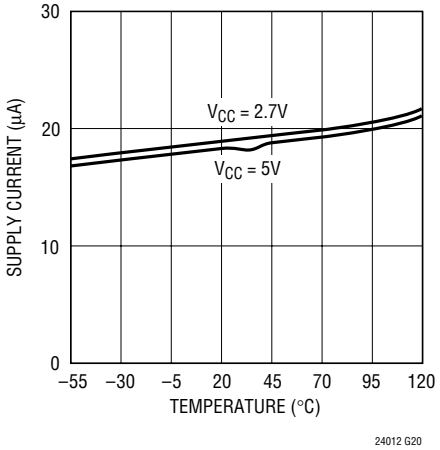
24012 G18

TYPICAL PERFORMANCE CHARACTERISTICS

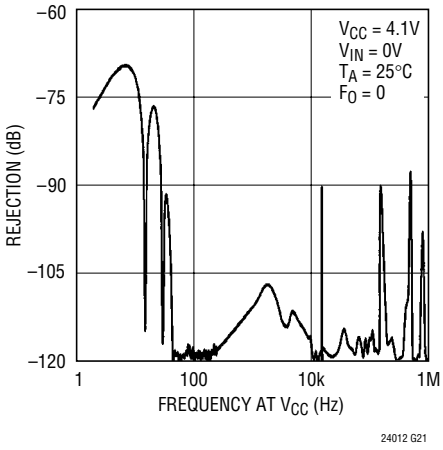
Conversion Current vs Temperature



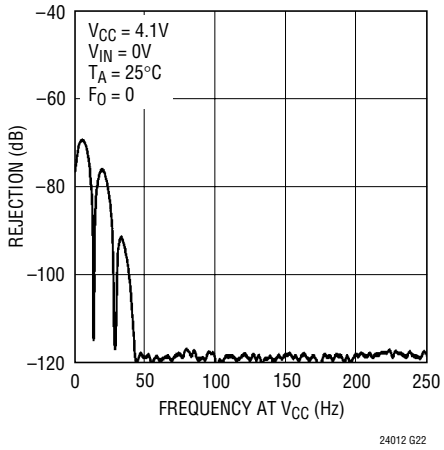
Sleep Current vs Temperature



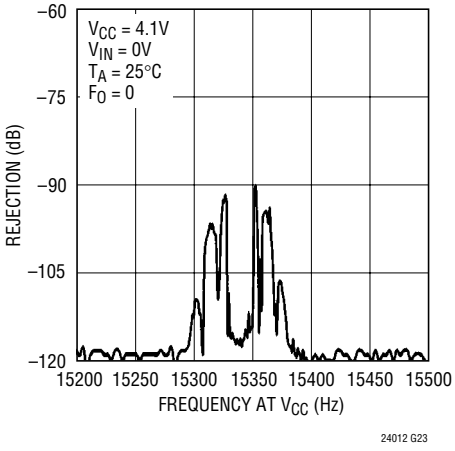
Rejection vs Frequency at V_{CC}



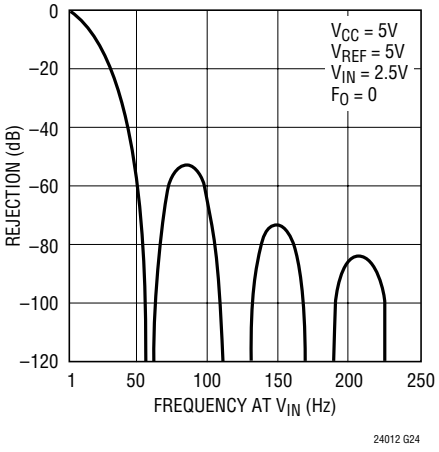
Rejection vs Frequency at V_{CC}



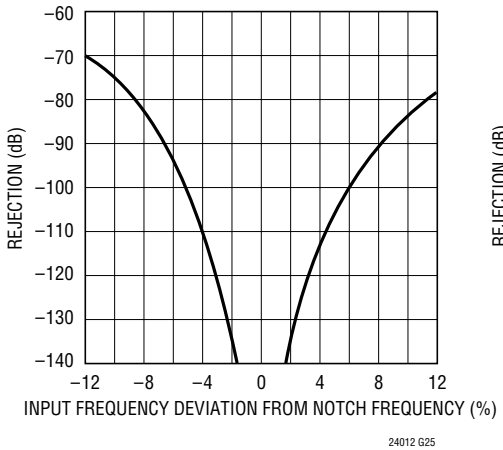
Rejection vs Frequency at V_{CC}



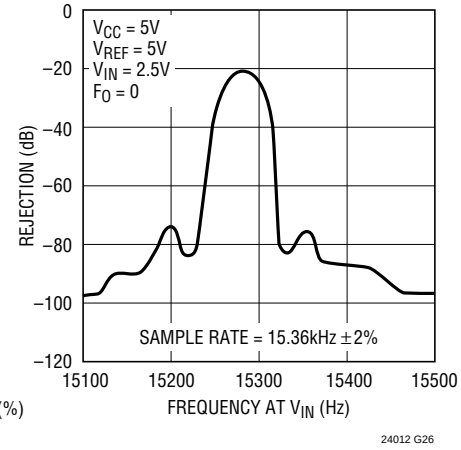
Rejection vs Frequency at V_{IN}



Rejection vs Frequency at V_{IN}



Rejection vs Frequency at V_{IN}



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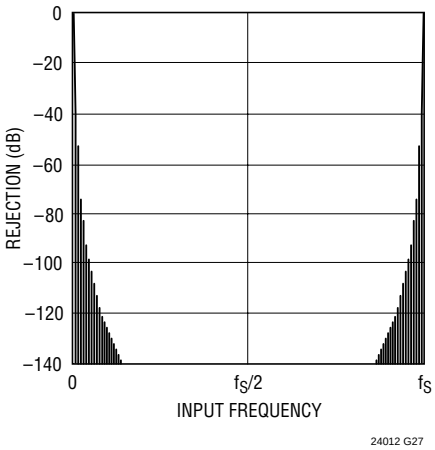
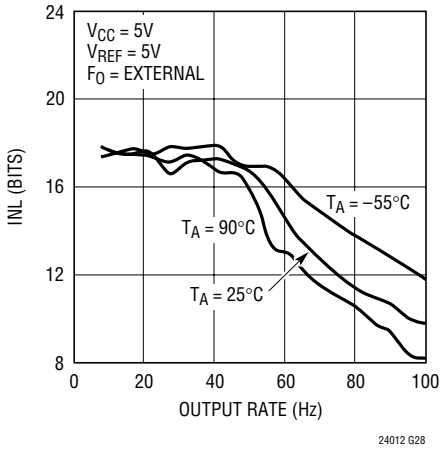
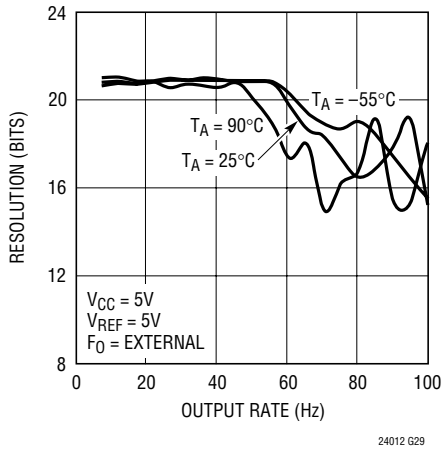


TYPICAL PERFORMANCE CHARACTERISTICS

INL vs Output Rate



Resolution vs Output Rate



PIN FUNCTIONS

V_{CC} (Pin 1): Positive Supply Voltage. Bypass to GND (Pin 6) with a 10µF tantalum capacitor in parallel with 0.1µF ceramic capacitor as close to the part as possible.

FS_{SET} (Pin 2): Full-Scale Set Input. This pin defines the full-scale input value. When $V_{IN} = FS_{SET}$, the ADC outputs full scale ($FFFFF_H$). The total reference voltage is $FS_{SET} – ZS_{SET}$.

CH0, CH1 (Pins 4, 3): Analog Input Channels. The input voltage range is $–0.125 • V_{REF}$ to $1.125 • V_{REF}$. For $V_{REF} > 2.5V$, the input voltage range may be limited by the absolute maximum rating of –0.3V to V_{CC} + 0.3V. Conversions are performed alternately between CH0 and CH1 for the LTC2402. Pin 4 is a No Connect (NC) on the LTC2401.

ZS_{SET} (Pin 5): Zero-Scale Set Input. This pin defines the zero-scale input value. When $V_{IN} = ZS_{SET}$, the ADC outputs zero scale (00000_H).

GND (Pin 6): Ground. Shared pin for analog ground, digital ground, reference ground and signal ground. Should be connected directly to a ground plane through a minimum length trace or it should be the single-point-ground in a single-point grounding system.

$\overline{CS}$ (Pin 7): Active LOW Digital Input. A LOW on this pin enables the SDO digital output and wakes up the ADC. Following each conversion, the ADC automatically enters the Sleep mode and remains in this low power state as long as $\overline{CS}$ is HIGH. A LOW on $\overline{CS}$ wakes up the ADC. A LOW-to-HIGH transition on this pin disables the SDO digital output. A LOW-to-HIGH transition on $\overline{CS}$ during the Data Output transfer aborts the data transfer and starts a new conversion.

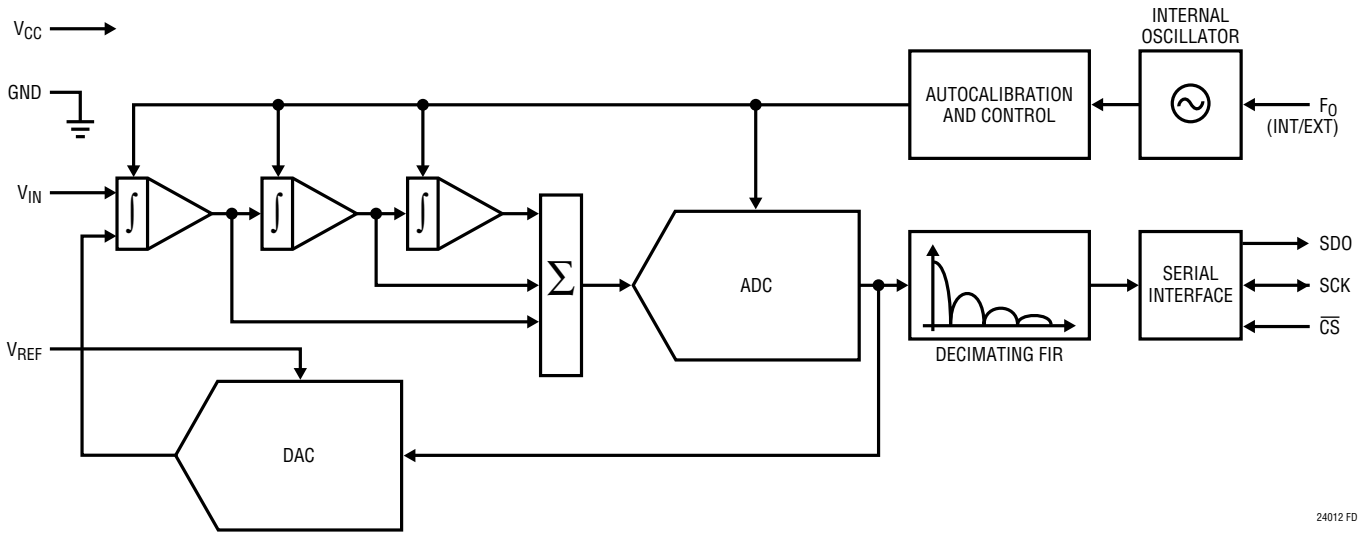
SDO (Pin 8): Three-State Digital Output. During the data output period, this pin is used for serial data output. When the chip select $\overline{CS}$ is HIGH ($\overline{CS} = V_{CC}$), the SDO pin is in a high impedance state. During the Conversion and Sleep periods, this pin can be used as a conversion status output. The conversion status can be observed by pulling $\overline{CS}$ LOW.

PIN FUNCTIONS

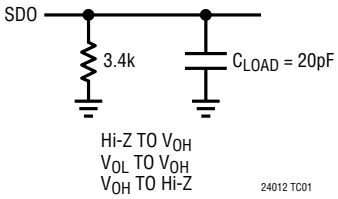
SCK (Pin 9): Bidirectional Digital Clock Pin. In the Internal Serial Clock Operation mode, SCK is used as digital output for the internal serial interface clock during the data output period. In the External Serial Clock Operation mode, SCK is used as digital input for the external serial interface. An internal pull-up current source is automatically activated in Internal Serial Clock Operation mode. The Serial Clock mode is determined by the level applied to SCK at power up and the falling edge of $\overline{CS}$.

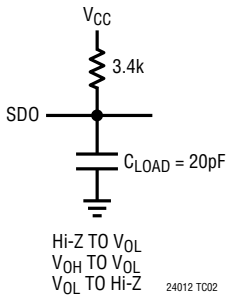
F_O (Pin 10): Frequency Control Pin. Digital input that controls the ADC's notch frequencies and conversion time. When the F_O pin is connected to V_{CC} ($F_O = V_{CC}$), the converter uses its internal oscillator and the digital filter's first null is located at 50Hz. When the F_O pin is connected to GND ($F_O = 0V$), the converter uses its internal oscillator and the digital filter's first null is located at 60Hz. When F_O is driven by an external clock signal with a frequency f_{EOSC}, the converter uses this signal as its clock and the digital filter first null is located at a frequency $f_{EOSC}/2560$.

FUNCTIONAL BLOCK DIAGRAM



TEST CIRCUITS





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Converter Operation Cycle

The LTC2401/LTC2402 are low power, delta-sigma analog-to-digital converters with an easy to use 3-wire serial interface. Their operation is simple and made up of three states. The converter operating cycle begins with the conversion, followed by a low power sleep state and concluded with the data output (see Figure 1). The 3-wire interface consists of serial data output (SDO), a serial clock (SCK) and a chip select ($\overline{CS}$).

Initially, the LTC2401/LTC2402 perform a conversion. Once the conversion is complete, the device enters the sleep state. While in this sleep state, power consumption is reduced by an order of magnitude. The part remains in the sleep state as long as $\overline{CS}$ is logic HIGH. The conversion result is held indefinitely in a static shift register while the converter is in the sleep state.

Once $\overline{CS}$ is pulled low, the device begins outputting the conversion result. There is no latency in the conversion result. The data output corresponds to the conversion just performed. This result is shifted out on the serial data out pin (SDO) under the control of the serial clock (SCK). Data is updated on the falling edge of SCK allowing the user to reliably latch data on the rising edge of SCK, see Figure 3. The data output state is concluded once 32 bits are read out of the ADC or when $\overline{CS}$ is brought HIGH. The device automatically initiates a new conversion cycle and the cycle repeats.

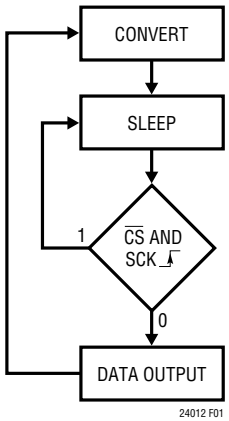

Figure 1. LTC2401/LTC2402 State Transition Diagram

Through timing control of the $\overline{CS}$ and SCK pins, the LTC2401/LTC2402 offer several flexible modes of operation (internal or external SCK and free-running conversion modes). These various modes do not require programming configuration registers; moreover, they do not disturb the cyclic operation described above. These modes of operation are described in detail in the Serial Interface Timing Modes section.

Conversion Clock

A major advantage delta-sigma converters offer over conventional type converters is an on-chip digital filter (commonly known as Sinc or Comb filter). For high resolution, low frequency applications, this filter is typically designed to reject line frequencies of 50Hz or 60Hz plus their harmonics. In order to reject these frequencies in excess of 110dB, a highly accurate conversion clock is required. The LTC2401/LTC2402 incorporate an on-chip highly accurate oscillator. This eliminates the need for external frequency setting components such as crystals or oscillators. Clocked by the on-chip oscillator, the LTC2401/LTC2402 reject line frequencies (50Hz or 60Hz ±2%) a minimum of 110dB.

Ease of Use

The LTC2401/LTC2402 data output has no latency, filter settling or redundant data associated with the conversion cycle. There is a one-to-one correspondence between the conversion and the output data. Therefore, multiplexing an analog input voltage is easy.

The LTC2401/LTC2402 perform offset and full-scale calibrations every conversion cycle. This calibration is transparent to the user and has no effect on the cyclic operation described above. The advantage of continuous calibration is extreme stability of offset and full-scale readings with respect to time, supply voltage change and temperature drift.

Power-Up Sequence

The LTC2401/LTC2402 automatically enter an internal reset state when the power supply voltage V_{CC} drops below approximately 2.2V. This feature guarantees the

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integrity of the conversion result and of the serial interface mode selection which is performed at the initial power-up. (See the 2-wire I/O sections in the Serial Interface Timing Modes section.)

When the V_{CC} voltage rises above this critical threshold, the converter creates an internal power-on-reset (POR) signal with duration of approximately 0.5ms. The POR signal clears all internal registers. Following the POR signal, the LTC2401/LTC2402 start a normal conversion cycle and follows the normal succession of states described above. The first conversion result following POR is accurate within the specifications of the device.

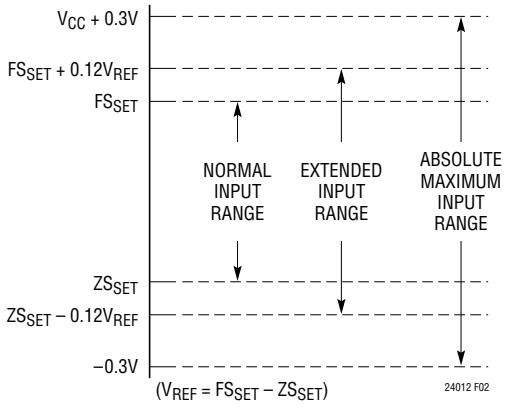

Figure 2. LTC2401/LTC2402 Input Range

Reference Voltage Range

The LTC2401/LTC2402 can accept a reference voltage (V_{REF} = FS_{SET} – ZS_{SET}) from 0V to V_{CC}. The converter output noise is determined by the thermal noise of the front-end circuits, and as such, its value in microvolts is nearly constant with reference voltage. A decrease in reference voltage will not significantly improve the converter's effective resolution. On the other hand, a reduced reference voltage will improve the overall converter INL performance. The recommended range for the LTC2401/LTC2402 voltage reference is 100mV to V_{CC}.

Input Voltage Range

The converter is able to accommodate system level offset and gain errors as well as system level overrange situations due to its extended input range, see Figure 2. The LTC2401/LTC2402 convert input signals within the extended input range of –0.125 • V_{REF} to 1.125 • V_{REF} (V_{REF} = FS_{SET} – ZS_{SET}).

For large values of V_{REF} (V_{REF} = FS_{SET} – ZS_{SET}), this range is limited by the absolute maximum voltage range of –0.3V to (V_{CC} + 0.3V). Beyond this range, the input ESD protection devices begin to turn on and the errors due to the input leakage current increase rapidly.

Input signals applied to V_{IN} may extend below ground by –300mV and above V_{CC} by 300mV. In order to limit any fault current, a resistor of up to 5k may be added in series with the V_{IN} pin without affecting the performance of the device. In the physical layout, it is important to maintain the parasitic capacitance of the connection between this series resistance and the V_{IN} pin as low as possible; therefore, the resistor should be located as close as practical to the V_{IN} pin. The effect of the series resistance on the converter accuracy can be evaluated from the curves presented in the Analog Input/Reference Current section. In addition, a series resistor will introduce a temperature dependent offset error due to the input leakage current. A 1nA input leakage current will develop a 1ppm offset error on a 5k resistor if V_{REF} = 5V. This error has a very strong temperature dependency.

Output Data Format

The LTC2401/LTC2402 serial output data stream is 32 bits long. The first 4 bits represent status information indicating the sign, selected channel, input range and conversion state. The next 24 bits are the conversion result, MSB first. The remaining 4 bits are sub LSBs beyond the 24-bit level that may be included in averaging or discarded without loss of resolution.

Bit 31 (first output bit) is the end of conversion ($\overline{EOC}$) indicator. This bit is available at the SDO pin during the conversion and sleep states whenever the $\overline{CS}$ pin is LOW. This bit is HIGH during the conversion and goes LOW when the conversion is complete.

Bit 30 (second output bit) for the LTC2402, this bit is LOW if the last conversion was performed on CH0 and HIGH for CH1. This bit is always low for the LTC2401.

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Bit 29 (third output bit) is the conversion result sign indicator (SIG). If V_{IN} is >0, this bit is HIGH. If V_{IN} is <0, this bit is LOW. The sign bit changes state during the zero code.

Bit 28 (forth output bit) is the extended input range (EXR) indicator. If the input is within the normal input range $0 \le V_{IN} \le V_{REF}$, this bit is LOW. If the input is outside the normal input range, $V_{IN} > V_{REF}$ or $V_{IN} < 0$, this bit is HIGH.

The function of these bits is summarized in Table 1.

Table 1. LTC2401/LTC2402 Status Bits

Input Range	Bit 31 $\overline{EOC}$	Bit 30 $\overline{CH0}$/CH1	Bit 29 SIG	Bit 28 EXR
$V_{IN} > V_{REF}$	0	0/1	1	1
$0 < V_{IN} \le V_{REF}$	0	0/1	1	0
$V_{IN} = 0^+/0^-$	0	0/1	1/0	0
$V_{IN} < 0$	0	0/1	0	1

Bit 27 (fifth output bit) is the most significant bit (MSB).

Bits 27-4 are the 24-bit conversion result MSB first.

Bit 4 is the least significant bit (LSB).

Bits 3-0 are sub LSBs below the 24-bit level. Bits 3-0 may be included in averaging or discarded without loss of resolution.

Data is shifted out of the SDO pin under control of the serial clock (SCK), see Figure 3. Whenever $\overline{CS}$ is HIGH, SDO remains high impedance and any SCK clock pulses are ignored by the internal data out shift register.

In order to shift the conversion result out of the device, $\overline{CS}$ must first be driven LOW. $\overline{EOC}$ is seen at the SDO pin of the device once $\overline{CS}$ is pulled LOW. $\overline{EOC}$ changes real time from HIGH to LOW at the completion of a conversion. This signal may be used as an interrupt for an external microcontroller. Bit 31 ($\overline{EOC}$) can be captured on the first rising edge of SCK. Bit 30 is shifted out of the device on the first falling edge of SCK. The final data bit (Bit 0) is shifted out on the falling edge of the 31st SCK and may be latched on the rising edge of the 32nd SCK pulse. On the falling edge of the 32nd SCK pulse, SDO goes HIGH indicating a new conversion cycle has been initiated. This bit serves as $\overline{EOC}$ (Bit 31) for the next conversion cycle. Table 2 summarizes the output data format.

As long as the voltage on the V_{IN} pin is maintained within the –0.3V to (V_{CC} + 0.3V) absolute maximum operating range, a conversion result is generated for any input value from $-0.125 \cdot V_{REF}$ to $1.125 \cdot V_{REF}$. For input voltages greater than $1.125 \cdot V_{REF}$, the conversion result is clamped to the value corresponding to $1.125 \cdot V_{REF}$. For input voltages below $-0.125 \cdot V_{REF}$, the conversion result is clamped to the value corresponding to $-0.125 \cdot V_{REF}$.

Frequency Rejection Selection (F_O Pin Connection)

The LTC2401/LTC2402 internal oscillator provides better than 110dB normal mode rejection at the line frequency and all its harmonics for 50Hz ±2% or 60Hz ±2%. For 60Hz rejection, F_O (Pin 10) should be connected to GND (Pin 6) while for 50Hz rejection the F_O pin should be connected to V_{CC} (Pin 1).

The selection of 50Hz or 60Hz rejection can also be made by driving F_O to an appropriate logic level. A selection change during the sleep or data output states will not

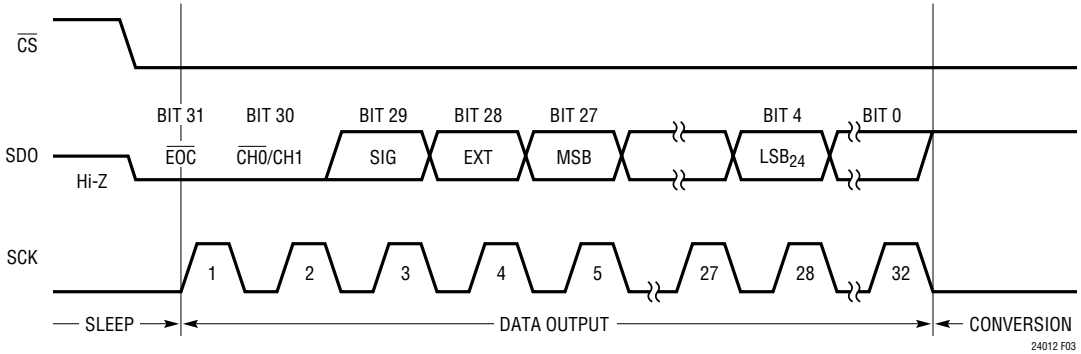

Figure 3. Output Data Timing

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Table 2. LTC2401/LTC2402 Output Data Format

Input Voltage	Bit 31 $\overline{EOC}$	Bit 30 CH SELECT	Bit 29 SIG	Bit 28 EXR	Bit 27 MSB	Bit 26	Bit 25	Bit 24	Bit 23	…	Bit 4 LSB	Bit 3-0 SUB LSBs*
$V_{IN} > 9/8 \cdot V_{REF}$	0	$\overline{CH0}$/CH1	1	1	0	0	0	1	1	...	1	X
$9/8 \cdot V_{REF}$	0	$\overline{CH0}$/CH1	1	1	0	0	0	1	1	...	1	X
$V_{REF} + 1LSB$	0	$\overline{CH0}$/CH1	1	1	0	0	0	0	0	...	0	X
V_{REF}	0	$\overline{CH0}$/CH1	1	0	1	1	1	1	1	...	1	X
$3/4V_{REF} + 1LSB$	0	$\overline{CH0}$/CH1	1	0	1	1	0	0	0	...	0	X
$3/4V_{REF}$	0	$\overline{CH0}$/CH1	1	0	1	0	1	1	1	...	1	X
$1/2V_{REF} + 1LSB$	0	$\overline{CH0}$/CH1	1	0	1	0	0	0	0	...	0	X
$1/2V_{REF}$	0	$\overline{CH0}$/CH1	1	0	0	1	1	1	1	...	1	X
$1/4V_{REF} + 1LSB$	0	$\overline{CH0}$/CH1	1	0	0	1	0	0	0	...	0	X
$1/4V_{REF}$	0	$\overline{CH0}$/CH1	1	0	0	0	1	1	1	...	1	X
$0^+/0^-$	0	$\overline{CH0}$/CH1	1/0**	0	0	0	0	0	0	...	0	X
–1LSB	0	$\overline{CH0}$/CH1	0	1	1	1	1	1	1	...	1	X
$-1/8 \cdot V_{REF}$	0	$\overline{CH0}$/CH1	0	1	1	1	1	0	0	...	0	X
$V_{IN} < -1/8 \cdot V_{REF}$	0	$\overline{CH0}$/CH1	0	1	1	1	1	0	0	...	0	X

*The sub LSBs are valid conversion results beyond the 24-bit level that may be included in averaging or discarded without loss of resolution.
**The sign bit changes state during the 0 code.

disturb the converter operation. If the selection is made during the conversion state, the result of the conversion in progress may be outside specifications but the following conversions will not be affected.

When a fundamental rejection frequency different from 50Hz or 60Hz is required or when the converter must be synchronized with an outside source, the LTC2401/LTC2402 can operate with an external conversion clock. The converter automatically detects the presence of an external clock signal at the F_O pin and turns off the internal oscillator. The frequency f_{EOSC} of the external signal must be at least 2560Hz (1Hz notch frequency) to be detected. The external clock signal duty cycle is not significant as long as the minimum and maximum specifications for the high and low periods t_{HEO} and t_{LEO} are observed.

While operating with an external conversion clock of a frequency f_{EOSC}, the LTC2401/LTC2402 provide better than 110dB normal mode rejection in a frequency range $f_{EOSC}/2560$ ±4% and its harmonics. The normal mode rejection as a function of the input frequency deviation from $f_{EOSC}/2560$ is shown in Figure 4.

Whenever an external clock is not present at the F_O pin, the converter automatically activates its internal oscillator and enters the Internal Conversion Clock mode. The LTC2401/LTC2402 operation will not be disturbed if the change of conversion clock source occurs during the sleep state or during the data output state while the converter uses an

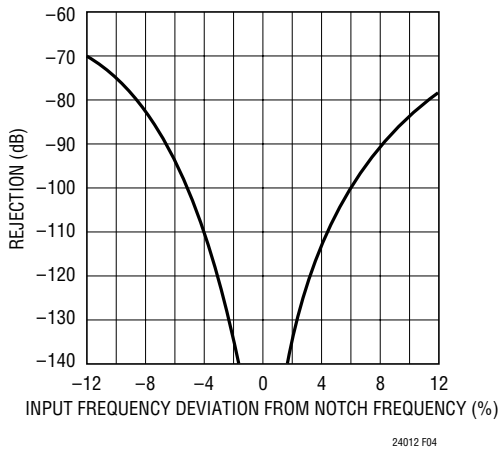

Figure 4. LTC2401/LTC2402 Normal Mode Rejection When Using an External Oscillator of Frequency f_{EOSC}

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external serial clock. If the change occurs during the conversion state, the result of the conversion in progress may be outside specifications but the following conversions will not be affected. If the change occurs during the data output state and the converter is in the Internal SCK mode, the serial clock duty cycle may be affected but the serial data stream will remain valid.

Table 3 summarizes the duration of each state as a function of F_O.

SERIAL INTERFACE

The LTC2401/LTC2402 transmit the conversion results and receives the start of conversion command through a synchronous 3-wire interface. During the conversion and sleep states, this interface can be used to assess the converter status and during the data output state it is used to read the conversion result.

Serial Clock Input/Output (SCK)

The serial clock signal present on SCK (Pin 9) is used to synchronize the data transfer. Each bit of data is shifted out the SDO pin on the falling edge of the serial clock.

In the Internal SCK mode of operation, the SCK pin is an output and the LTC2401/LTC2402 create their own serial clock by dividing the internal conversion clock by 8. In the External SCK mode of operation, the SCK pin is used as input. The internal or external SCK mode is selected on power-up and then reselected every time a HIGH-to-LOW transition is detected at the $\overline{CS}$ pin. If SCK is HIGH or floating at power-up or during this transition, the converter enters the internal SCK mode. If SCK is LOW at power-up or during this transition, the converter enters the external SCK mode.

Serial Data Output (SDO)

The serial data output pin, SDO (Pin 8), drives the serial data during the data output state. In addition, the SDO pin is used as an end of conversion indicator during the conversion and sleep states.

When $\overline{CS}$ (Pin 7) is HIGH, the SDO driver is switched to a high impedance state. This allows sharing the serial interface with other devices. If $\overline{CS}$ is LOW during the convert or sleep state, SDO will output $\overline{EOC}$. If $\overline{CS}$ is LOW during the conversion phase, the $\overline{EOC}$ bit appears HIGH on the SDO pin. Once the conversion is complete, $\overline{EOC}$ goes LOW. The device remains in the sleep state until the first rising edge of SCK occurs while $\overline{CS}$ = 0.

Chip Select Input ($\overline{CS}$)

The active LOW chip select, $\overline{CS}$ (Pin 7), is used to test the conversion status and to enable the data output transfer as described in the previous sections.

Table 3. LTC2401/LTC2402 State Duration

State	Operating Mode		Duration
CONVERT	Internal Oscillator	F_O = LOW (60Hz Rejection)	133ms
		F_O = HIGH (50Hz Rejection)	160ms
	External Oscillator	F_O = External Oscillator with Frequency f_{EOSC} kHz (f_{EOSC}/2560 Rejection)	20510/f_{EOSC}s
SLEEP			As Long As $\overline{CS}$ = HIGH Until $\overline{CS}$ = 0 and SCK ↓
DATA OUTPUT	Internal Serial Clock	F_O = LOW/HIGH (Internal Oscillator)	As Long As $\overline{CS}$ = LOW But Not Longer Than 1.67ms (32 SCK cycles)
		F_O = External Oscillator with Frequency f_{EOSC} kHz	As Long As $\overline{CS}$ = LOW But Not Longer Than 256/f_{EOSC}ms (32 SCK cycles)
	External Serial Clock with Frequency f_{SCK} kHz		As Long As $\overline{CS}$ = LOW But Not Longer Than 32/f_{SCK}ms (32 SCK cycles)

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In addition, the $\overline{CS}$ signal can be used to trigger a new conversion cycle before the entire serial data transfer has been completed. The LTC2401/LTC2402 will abort any serial data transfer in progress and start a new conversion cycle anytime a LOW-to-HIGH transition is detected at the $\overline{CS}$ pin after the converter has entered the data output state (i.e., after the first rising edge of SCK occurs with $\overline{CS}$ = 0).

Finally, $\overline{CS}$ can be used to control the free-running modes of operation, see Serial Interface Timing Modes section. Grounding $\overline{CS}$ will force the ADC to continuously convert at the maximum output rate selected by F_O. Tying a capacitor to $\overline{CS}$ will reduce the output rate and power dissipation by a factor proportional to the capacitor's value, see Figures 12 to 14.

SERIAL INTERFACE TIMING MODES

The LTC2401/LTC2402's 3-wire interface is SPI and MICROWIRE compatible. This interface offers several flexible modes of operation. These include internal/external serial clock, 2- or 3-wire I/O, single cycle conversion and autostart. The following sections describe each of these serial interface timing modes in detail. In all these cases, the converter can use the internal oscillator (F_O = LOW or F_O = HIGH) or an external oscillator connected to the F_O pin. Refer to Table 4 for a summary.

External Serial Clock, Single Cycle Operation (SPI/MICROWIRE Compatible)

This timing mode uses an external serial clock to shift out the conversion result and a $\overline{CS}$ signal to monitor and control the state of the conversion cycle, see Figure 5.

The serial clock mode is selected on the falling edge of $\overline{CS}$. To select the external serial clock mode, the serial clock pin (SCK) must be LOW during each $\overline{CS}$ falling edge.

The serial data output pin (SDO) is Hi-Z as long as $\overline{CS}$ is HIGH. At any time during the conversion cycle, $\overline{CS}$ may be pulled LOW in order to monitor the state of the converter. While $\overline{CS}$ is pulled LOW, $\overline{EOC}$ is output to the SDO pin. $\overline{EOC}$ = 1 while a conversion is in progress and $\overline{EOC}$ = 0 if the device is in the sleep state. Independent of $\overline{CS}$, the device automatically enters the low power sleep state once the conversion is complete.

When the device is in the sleep state ($\overline{EOC}$ = 0), its conversion result is held in an internal static shift register. The device remains in the sleep state until the first rising edge of SCK is seen while $\overline{CS}$ is LOW. Data is shifted out the SDO pin on each falling edge of SCK. This enables external circuitry to latch the output on the rising edge of SCK. $\overline{EOC}$ can be latched on the first rising edge of SCK and the last bit of the conversion result can be latched on the 32nd rising edge of SCK. On the 32nd falling edge of SCK, the device begins a new conversion. SDO goes HIGH ($\overline{EOC}$ = 1) indicating a conversion is in progress.

At the conclusion of the data cycle, $\overline{CS}$ may remain LOW and $\overline{EOC}$ monitored as an end-of-conversion interrupt. Alternatively, $\overline{CS}$ may be driven HIGH setting SDO to Hi-Z. As described above, $\overline{CS}$ may be pulled LOW at any time in order to monitor the conversion status.

Typically, $\overline{CS}$ remains LOW during the data output state. However, the data output state may be aborted by pulling $\overline{CS}$ HIGH anytime between the first rising edge and the 32nd falling edge of SCK, see Figure 6. On the rising edge

Table 4. LTC2401/LTC2402 Interface Timing Modes

Configuration	SCK Source	Conversion Cycle Control	Data Output Control	Connection and Waveforms
External SCK, Single Cycle Conversion	External	$\overline{CS}$ and SCK	$\overline{CS}$ and SCK	Figures 5, 6
External SCK, 2-Wire I/O	External	SCK	SCK	Figure 7
Internal SCK, Single Cycle Conversion	Internal	$\overline{CS}\downarrow$	$\overline{CS}\downarrow$	Figures 8, 9
Internal SCK, 2-Wire I/O, Continuous Conversion	Internal	Continuous	Internal	Figure 10
Internal SCK, Autostart Conversion	Internal	C_{EXT}	Internal	Figure 11

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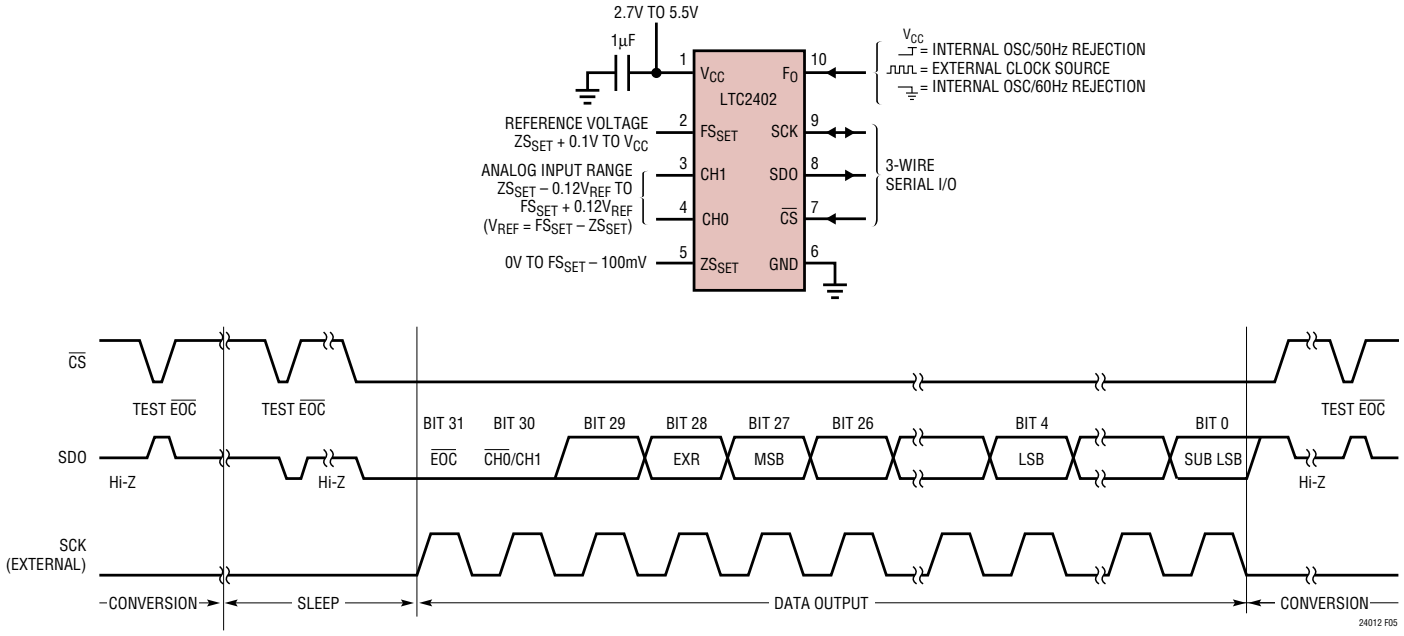

Figure 5. External Serial Clock, Single Cycle Operation

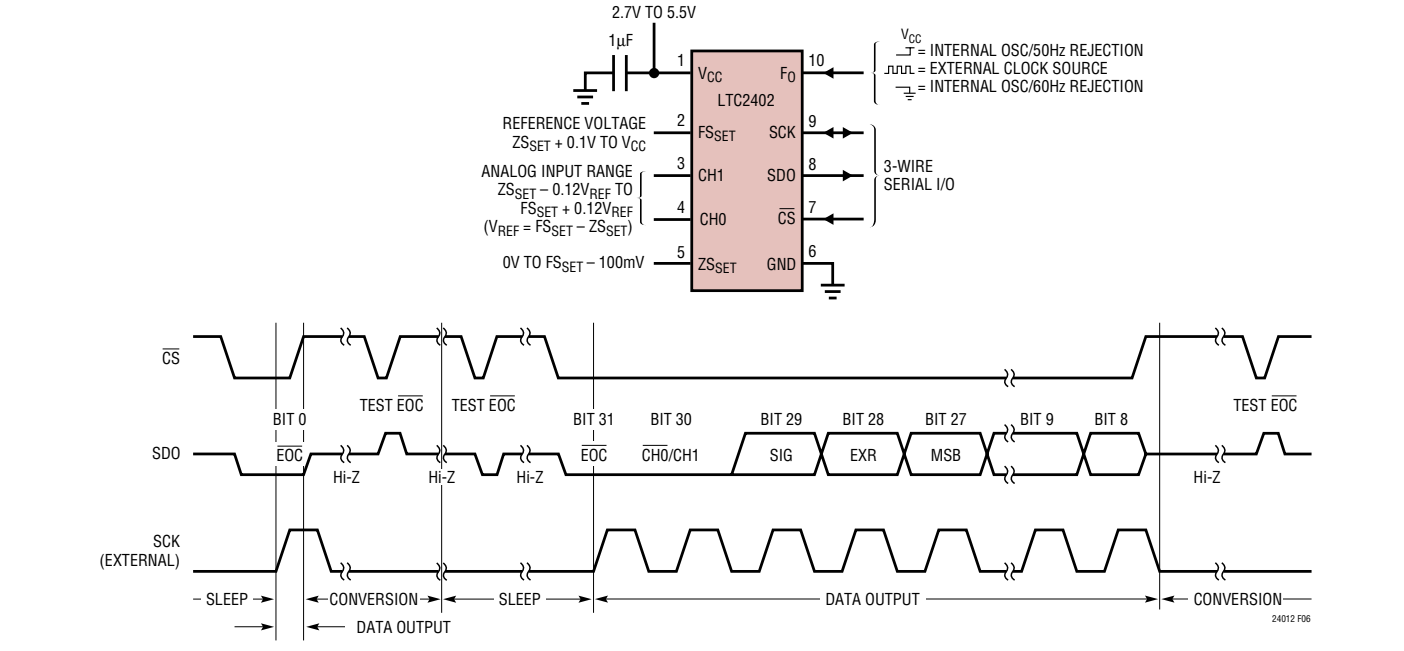

Figure 6. External Serial Clock, Reduced Data Output Length

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of $\overline{CS}$, the device aborts the data output state and immediately initiates a new conversion. This is useful for systems not requiring all 32 bits of output data, aborting an invalid conversion cycle or synchronizing the start of a conversion.

External Serial Clock, 2-Wire I/O

This timing mode utilizes a 2-wire serial I/O interface. The conversion result is shifted out of the device by an externally generated serial clock (SCK) signal, see Figure 7. $\overline{CS}$ may be permanently tied to ground (Pin 6), simplifying the user interface or isolation barrier.

The external serial clock mode is selected at the end of the power-on reset (POR) cycle. The POR cycle is concluded approximately 0.5ms after V_{CC} exceeds 2.2V. The level applied to SCK at this time determines if SCK is internal or external. SCK must be driven LOW prior to the end of POR in order to enter the external serial clock timing mode.

Since $\overline{CS}$ is tied LOW, the end-of-conversion ($\overline{EOC}$) can be continuously monitored at the SDO pin during the convert and sleep states. $\overline{EOC}$ may be used as an interrupt to an external controller indicating the conversion result is ready. $\overline{EOC}$ = 1 while the conversion is in progress and $\overline{EOC}$ = 0 once the conversion enters the low power sleep state. On the falling edge of $\overline{EOC}$, the conversion result is loaded into an internal static shift register. The device remains in the sleep state until the first rising edge of SCK. Data is shifted out the SDO pin on each falling edge of SCK enabling external circuitry to latch data on the rising edge of SCK. $\overline{EOC}$ can be latched on the first rising edge of SCK. On the 32nd falling edge of SCK, SDO goes HIGH ($\overline{EOC}$ = 1) indicating a new conversion has begun.

Internal Serial Clock, Single Cycle Operation

This timing mode uses an internal serial clock to shift out the conversion result and a $\overline{CS}$ signal to monitor and control the state of the conversion cycle, see Figure 8.

In order to select the internal serial clock timing mode, the serial clock pin (SCK) must be floating (Hi-Z) or pulled HIGH prior to the falling edge of $\overline{CS}$. The device will not enter the internal serial clock mode if SCK is driven LOW on the falling edge of $\overline{CS}$. An internal weak pull-up resistor is active on the SCK pin during the falling edge of $\overline{CS}$; therefore, the internal serial clock timing mode is automatically selected if SCK is not externally driven.

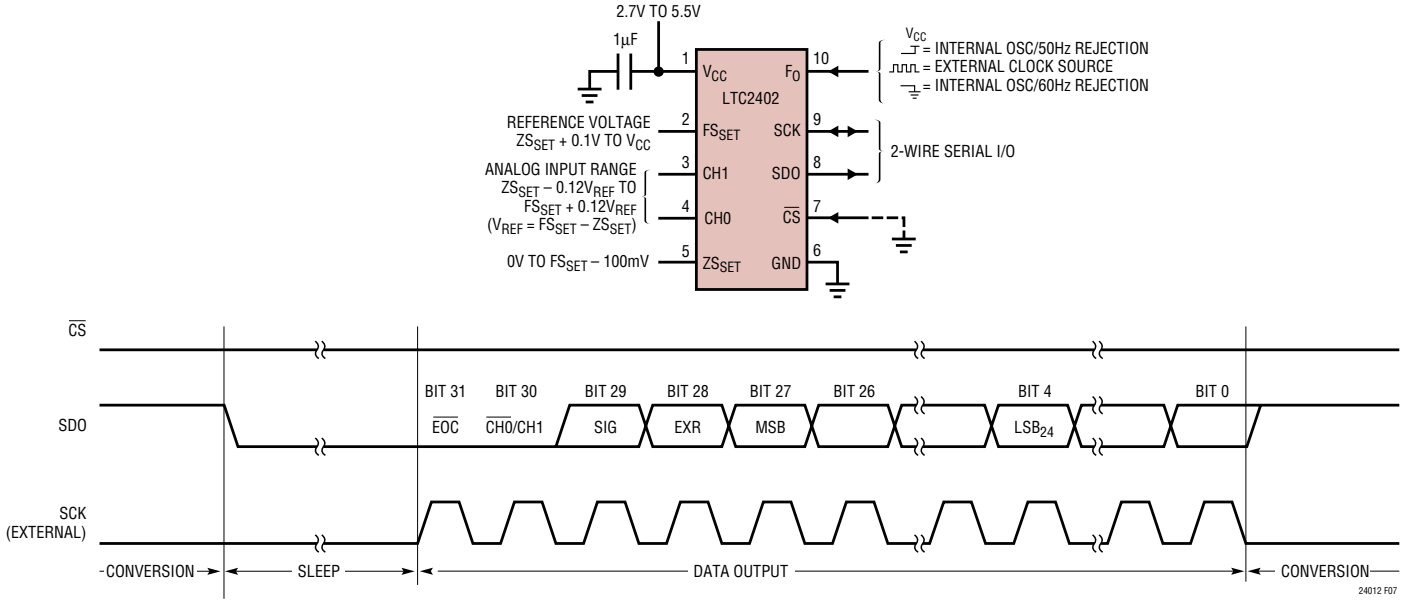

Figure 7. External Serial Clock, $\overline{CS}$ = 0 Operation

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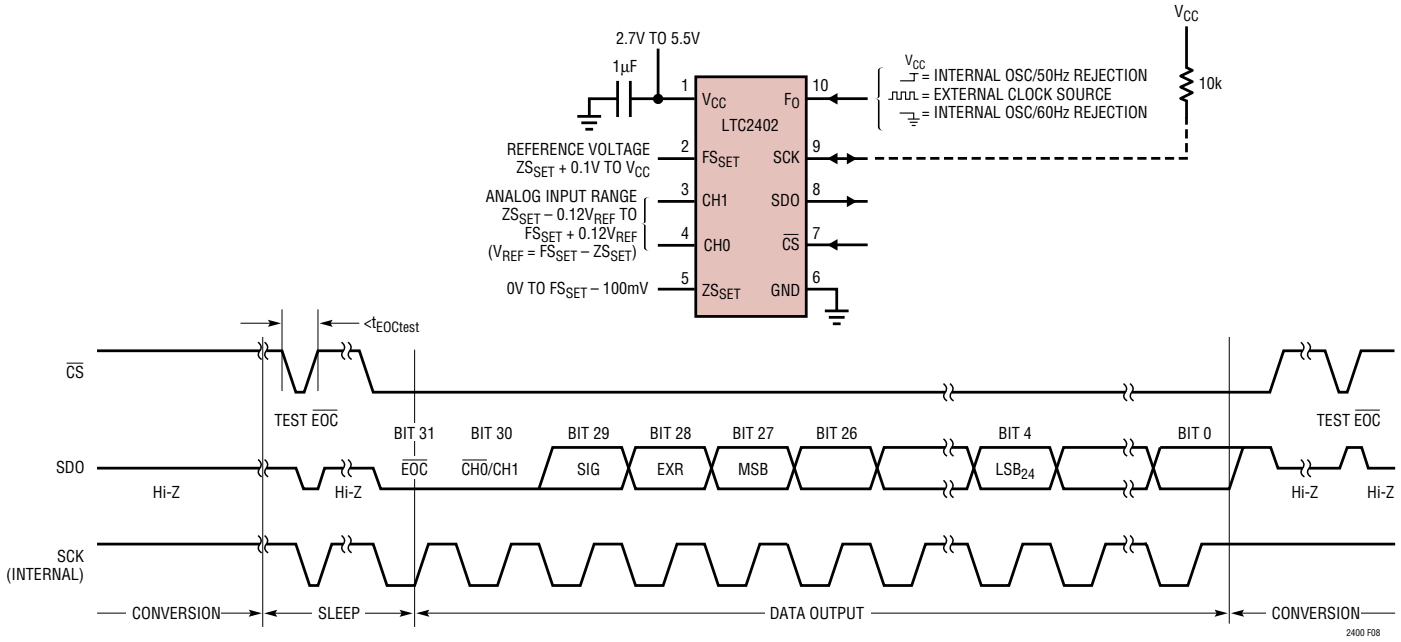

Figure 8. Internal Serial Clock, Single Cycle Operation

The serial data output pin (SDO) is Hi-Z as long as $\overline{CS}$ is HIGH. At any time during the conversion cycle, $\overline{CS}$ may be pulled LOW in order to monitor the state of the converter. Once $\overline{CS}$ is pulled LOW, SCK goes LOW and $\overline{EOC}$ is output to the SDO pin. $\overline{EOC}$ = 1 while a conversion is in progress and $\overline{EOC}$ = 0 if the device is in the sleep state.

When testing $\overline{EOC}$, if the conversion is complete ($\overline{EOC}$ = 0), the device will exit the sleep state and enter the data output state if $\overline{CS}$ remains LOW. In order to prevent the device from exiting the low power sleep state, $\overline{CS}$ must be pulled HIGH before the first rising edge of SCK. In the internal SCK timing mode, SCK goes HIGH and the device begins outputting data at time $t_{EOCtest}$ after the falling edge of $\overline{CS}$ (if $\overline{EOC}$ = 0) or $t_{EOCtest}$ after $\overline{EOC}$ goes LOW (if $\overline{CS}$ is LOW during the falling edge of $\overline{EOC}$). The value of $t_{EOCtest}$ is 23µs if the device is using its internal oscillator (F_O = logic LOW or HIGH). If F_O is driven by an external oscillator of frequency f_{EOSC}, then $t_{EOCtest}$ is $3.6/f_{EOSC}$. If $\overline{CS}$ is pulled HIGH before time $t_{EOCtest}$, the device remains in the sleep state. The conversion result is held in the internal static shift register.

If $\overline{CS}$ remains LOW longer than $t_{EOCtest}$, the first rising edge of SCK will occur and the conversion result is serially shifted out of the SDO pin. The data output cycle begins on this first rising edge of SCK and concludes after the 32nd rising edge. Data is shifted out the SDO pin on each falling edge of SCK. The internally generated serial clock is output to the SCK pin. This signal may be used to shift the conversion result into external circuitry. $\overline{EOC}$ can be latched on the first rising edge of SCK and the last bit of the conversion result on the 32nd rising edge of SCK. After the 32nd rising edge, SDO goes HIGH ($\overline{EOC}$ = 1), SCK stays HIGH, and a new conversion starts.

Typically, $\overline{CS}$ remains LOW during the data output state. However, the data output state may be aborted by pulling $\overline{CS}$ HIGH anytime between the first and 32nd rising edge of SCK, see Figure 9. On the rising edge of $\overline{CS}$, the device aborts the data output state and immediately initiates a new conversion. This is useful for systems not requiring all 32 bits of output data, aborting an invalid conversion cycle, or synchronizing the start of a conversion. If $\overline{CS}$ is pulled HIGH while the converter is driving SCK LOW, the

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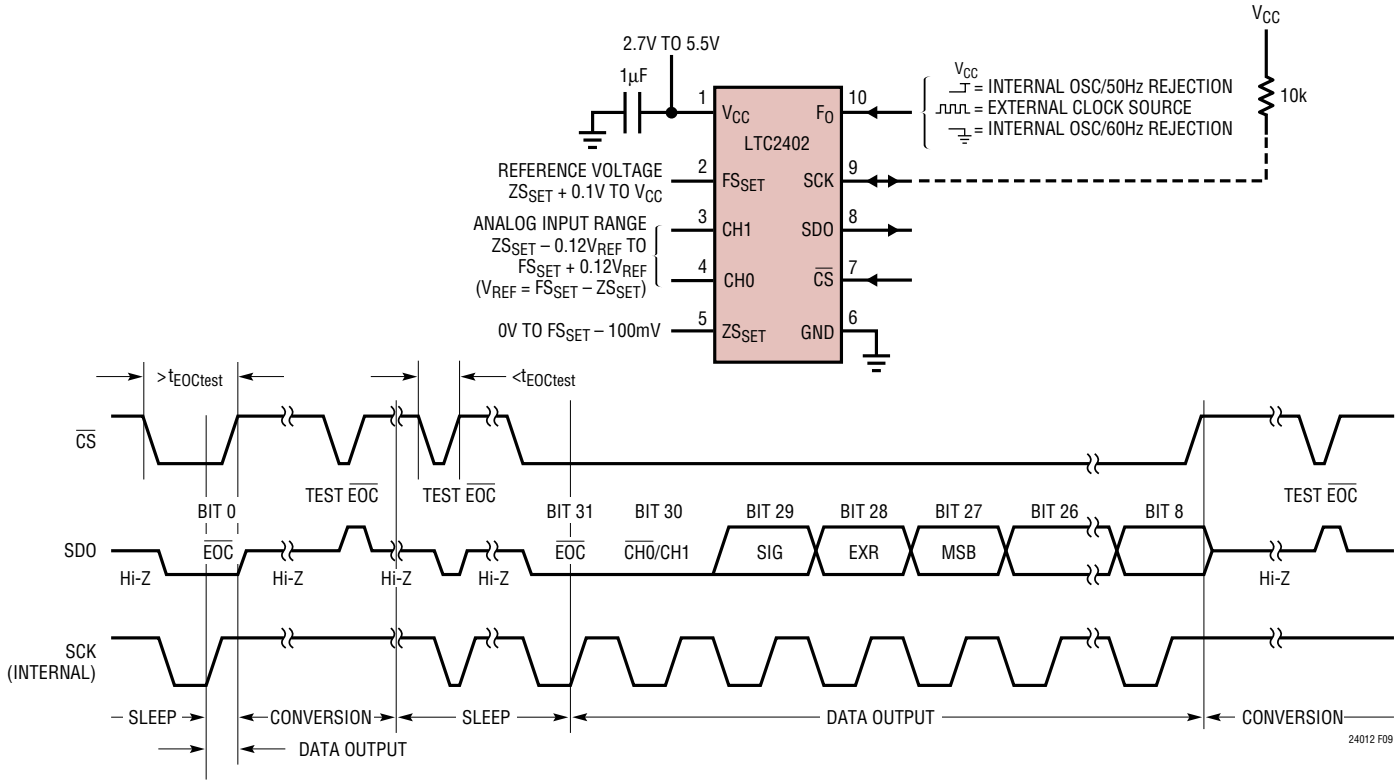

Figure 9. Internal Serial Clock, Reduced Data Output Length

internal pull-up is not available to restore SCK to a logic HIGH state. This will cause the device to exit the internal serial clock mode on the next falling edge of $\overline{CS}$. This can be avoided by adding an external 10k pull-up resistor to the SCK pin or by never pulling $\overline{CS}$ HIGH when SCK is LOW.

Whenever SCK is LOW, the LTC2401/LTC2402's internal pull-up at pin SCK is disabled. Normally, SCK is not externally driven if the device is in the internal SCK timing mode. However, certain applications may require an external driver on SCK. If this driver goes Hi-Z after outputting a LOW signal, the LTC2401/LTC2402's internal pull-up remains disabled. Hence, SCK remains LOW. On the next falling edge of $\overline{CS}$, the device is switched to the external SCK timing mode. By adding an external 10k pull-up resistor to SCK, this pin goes HIGH once the external driver goes Hi-Z. On the next $\overline{CS}$ falling edge, the device will remain in the internal SCK timing mode.

A similar situation may occur during the sleep state when $\overline{CS}$ is pulsed HIGH-LOW-HIGH in order to test the conversion status. If the device is in the sleep state ($\overline{EOC}$ = 0), SCK will go LOW. Once $\overline{CS}$ goes HIGH (within the time period defined above as $t_{EOCtest}$), the internal pull-up is activated. For a heavy capacitive load on the SCK pin, the internal pull-up may not be adequate to return SCK to a HIGH level before $\overline{CS}$ goes low again. This is not a concern under normal conditions where $\overline{CS}$ remains LOW after detecting $\overline{EOC}$ = 0. This situation is easily overcome by adding an external 10k pull-up resistor to the SCK pin.

Internal Serial Clock, 2-Wire I/O, Continuous Conversion

This timing mode uses a 2-wire, all output (SCK and SDO) interface. The conversion result is shifted out of the device by an internally generated serial clock (SCK) signal, see Figure 10. $\overline{CS}$ may be permanently tied to ground (Pin 6), simplifying the user interface or isolation barrier.

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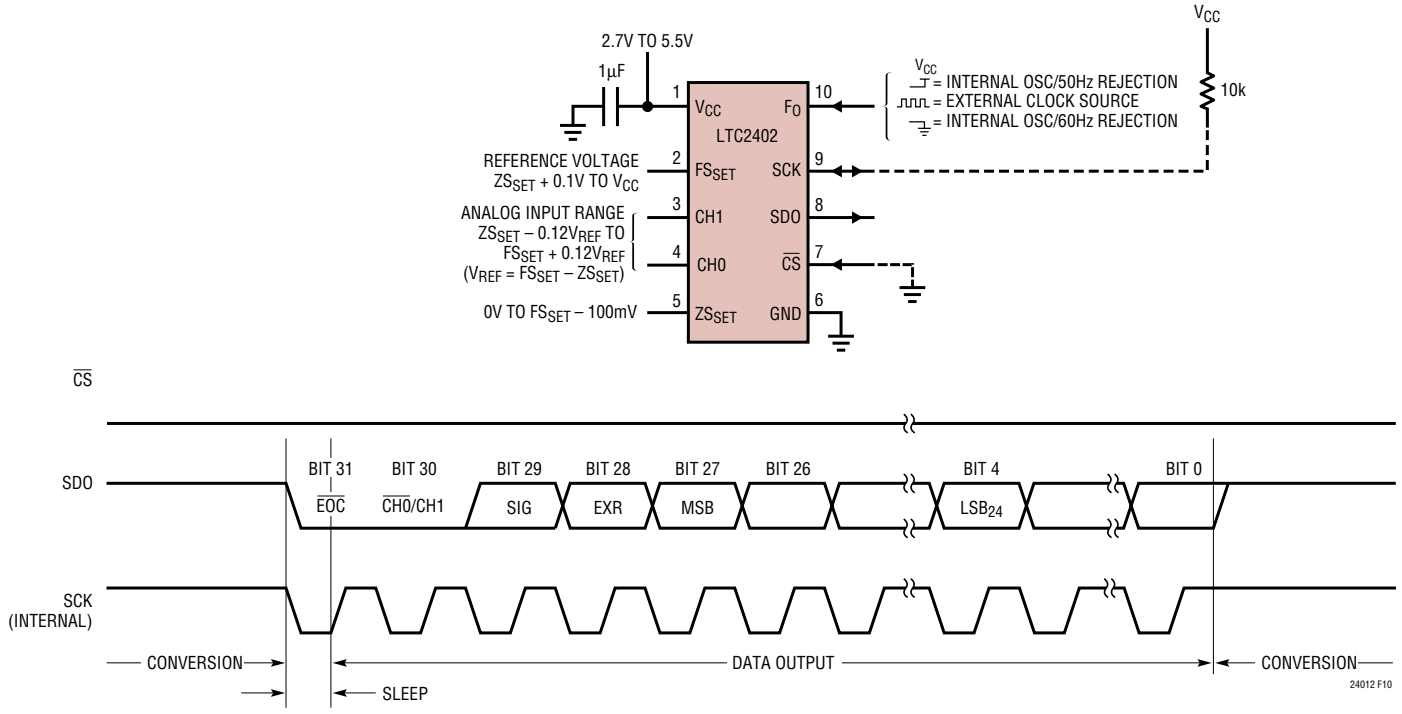

Figure 10. Internal Serial Clock, Continuous Operation

The internal serial clock mode is selected at the end of the power-on reset (POR) cycle. The POR cycle is concluded approximately 0.5ms after V_{CC} exceeds 2.2V. An internal weak pull-up is active during the POR cycle; therefore, the internal serial clock timing mode is automatically selected if SCK is not externally driven LOW (if SCK is loaded such that the internal pull-up cannot pull the pin HIGH, the external SCK mode will be selected).

During the conversion, the SCK and the serial data output pin (SDO) are HIGH ($\overline{EOC}$ = 1). Once the conversion is complete, SCK and SDO go LOW ($\overline{EOC}$ = 0) indicating the conversion has finished and the device has entered the low power sleep state. The part remains in the sleep state a minimum amount of time (1/2 the internal SCK period) then immediately begins outputting data. The data output cycle begins on the first rising edge of SCK and ends after the 32nd rising edge. Data is shifted out the SDO pin on each falling edge of SCK. The internally generated serial clock is output to the SCK pin. This signal may be used to shift the conversion result into external circuitry. $\overline{EOC}$ can be latched on the first rising edge of SCK and the last bit of the conversion result can be latched on the 32nd rising edge of SCK. After the 32nd rising edge, SDO goes HIGH ($\overline{EOC}$ = 1) indicating a new conversion is in progress. SCK remains HIGH during the conversion.

Internal Serial Clock, Autostart Conversion

This timing mode is identical to the internal serial clock, 2-wire I/O described above with one additional feature. Instead of grounding $\overline{CS}$, an external timing capacitor is tied to $\overline{CS}$.

While the conversion is in progress, the $\overline{CS}$ pin is held HIGH by an internal weak pull-up. Once the conversion is complete, the device enters the low power sleep state and an internal 25nA current source begins discharging the capacitor tied to $\overline{CS}$, see Figure 11. The time the converter spends in the sleep state is determined by the value of the external timing capacitor, see Figures 12 and 13. Once the voltage at $\overline{CS}$ falls below an internal threshold (≈1.4V), the device automatically begins outputting data. The data output cycle begins on the first rising edge of SCK and ends on the 32nd rising edge. Data is shifted out the SDO pin on each falling edge of SCK. The internally generated serial clock is output to the SCK pin. This signal may be

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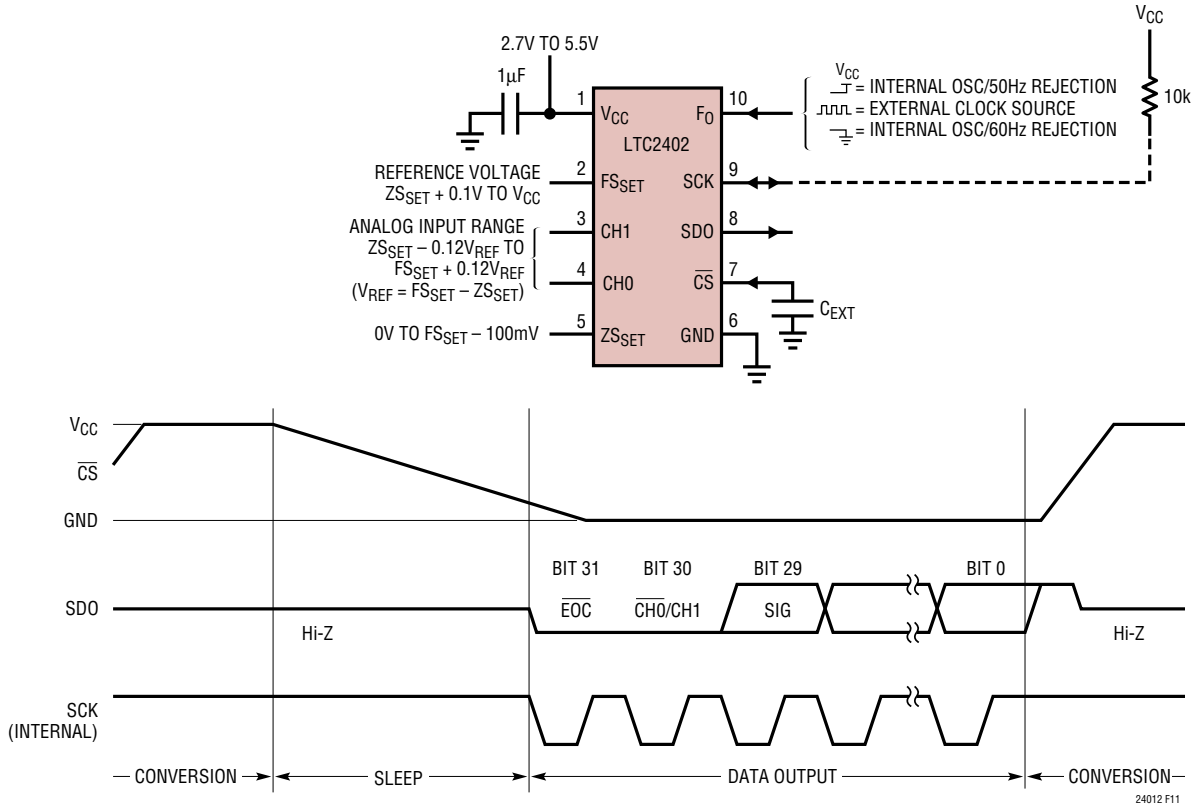

Figure 11. Internal Serial Clock, Autostart Operation

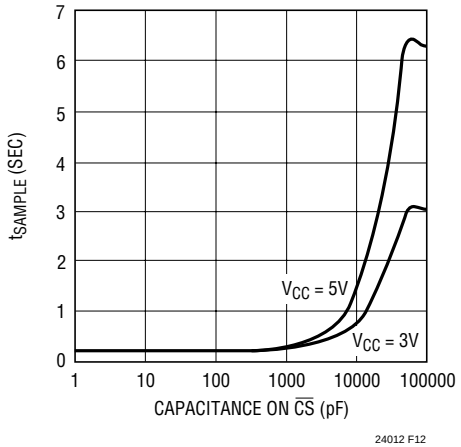

Figure 12. $\overline{CS}$ Capacitance vs t_{SAMPLE}

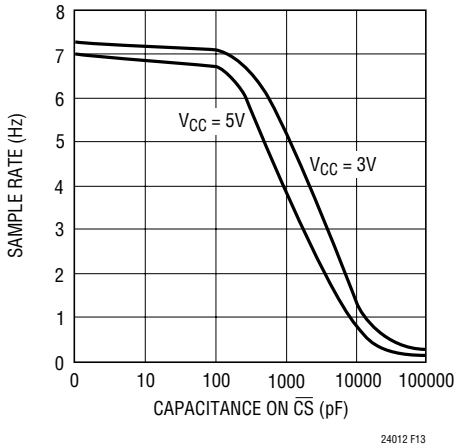

Figure 13. $\overline{CS}$ Capacitance vs Output Rate

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used to shift the conversion result into external circuitry. After the 32nd rising edge, $\overline{CS}$ is pulled HIGH and a new conversion is immediately started. This is useful in applications requiring periodic monitoring and ultralow power. Figure 14 shows the average supply current as a function of capacitance on $\overline{CS}$.

It should be noticed that the external capacitor discharge current is kept very small in order to decrease the converter power dissipation in the sleep state. In the autostart mode the analog voltage on the $\overline{CS}$ pin cannot be observed without disturbing the converter operation using a regular oscilloscope probe. When using this configuration, it is important to minimize the external leakage current at the $\overline{CS}$ pin by using a low leakage external capacitor and properly cleaning the PCB surface.

The internal serial clock mode is selected every time the voltage on the $\overline{CS}$ pin crosses an internal threshold voltage. An internal weak pull-up at the SCK pin is active while $\overline{CS}$ is discharging; therefore, the internal serial clock timing mode is automatically selected if SCK is floating. It is important to ensure there are no external drivers pulling SCK LOW while $\overline{CS}$ is discharging.

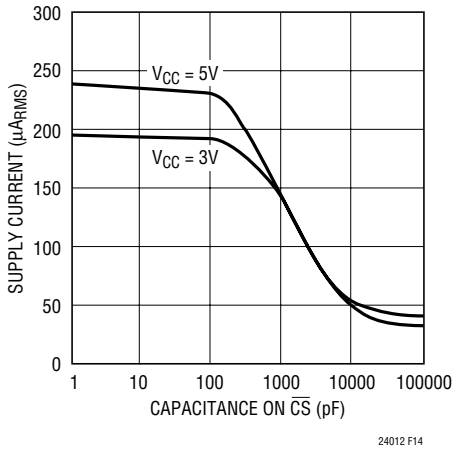

Figure 14. $\overline{CS}$ Capacitance vs Supply Current

DIGITAL SIGNAL LEVELS

The LTC2401/LTC2402's digital interface is easy to use. Its digital inputs (F_O, $\overline{CS}$ and SCK in External SCK mode of operation) accept standard TTL/CMOS logic levels and the internal hysteresis receivers can tolerate edge rates as slow as 100μs. However, some considerations are required to take advantage of exceptional accuracy and low supply current.

The digital output signals (SDO and SCK in Internal SCK mode of operation) are less of a concern because they are not generally active during the conversion state.

In order to preserve the LTC2401/LTC2402's accuracy, it is very important to minimize the ground path impedance which may appear in series with the input and/or reference signal and to reduce the current which may flow through this path. The GND pin should be connected to a low resistance ground plane through a minimum length trace. The use of multiple via holes is recommended to further reduce the connection resistance.

In an alternative configuration, the GND pin of the converter can be the single-point-ground in a single point grounding system. The input signal ground, the reference signal ground, the digital drivers ground (usually the digital ground) and the power supply ground (the analog ground) should be connected in a star configuration with the common point located as close to the GND pin as possible.

The power supply current during the conversion state should be kept to a minimum. This is achieved by restricting the number of digital signal transitions occurring during this period.

While a digital input signal is in the range 0.5V to (V_{CC} – 0.5V), the CMOS input receiver draws additional current from the power supply. It should be noted that, when any one of the digital input signals (F_O, $\overline{CS}$ and SCK in External SCK mode of operation) is within this range, the LTC2401/LTC2402 power supply current may increase even if the signal in question is at a valid logic level. For micropower operation and in order to minimize the potential errors due to additional ground pin current, it is recommended to drive all digital input signals to full CMOS levels [V_{IL} < 0.4V and V_{OH} > (V_{CC} – 0.4V)].

Severe ground pin current disturbances can also occur due to the undershoot of fast digital input signals. Undershoot and overshoot can occur because of the impedance mismatch at the converter pin when the transition time of an external control signal is less than twice the propagation delay from the driver to LTC2401/LTC2402. For

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reference, on a regular FR-4 board, signal propagation velocity is approximately 183ps/inch for internal traces and 170ps/inch for surface traces. Thus, a driver generating a control signal with a minimum transition time of 1ns must be connected to the converter pin through a trace shorter than 2.5 inches. This problem becomes particularly difficult when shared control lines are used and multiple reflections may occur. The solution is to carefully terminate all transmission lines close to their characteristic impedance.

Parallel termination near the LTC2401/LTC2402 pin will eliminate this problem but will increase the driver power dissipation. A series resistor between 27Ω and 56Ω placed near the driver or near the LTC2401/LTC2402 pin will also eliminate this problem without additional power dissipation. The actual resistor value depends upon the trace impedance and connection topology.

Driving the Input and Reference

The analog input and reference of the typical delta-sigma analog-to-digital converter are applied to a switched capacitor network. This network consists of capacitors switching between the analog input (V_{IN}), ZS_{SET} (Pin 5) and FS_{SET} (Pin 2). The result is small current spikes seen at both V_{IN} and V_{REF}. A simplified input equivalent circuit is shown in Figure 15.

The key to understanding the effects of this dynamic input current is based on a simple first order RC time constant model. Using the internal oscillator, the

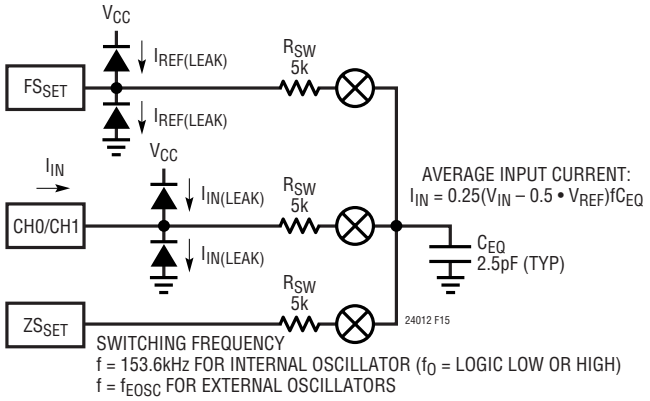

Figure 15. LTC2401/LTC2402 Equivalent Analog Input Circuit

LTC2401/LTC2402's internal switched capacitor network is clocked at 153,600Hz corresponding to a 6.5μs sampling period. Fourteen time constants are required each time a capacitor is switched in order to achieve 1ppm settling accuracy.

Therefore, the equivalent time constant at V_{IN} and V_{REF} should be less than 6.5μs/14 = 460ns in order to achieve 1ppm accuracy.

Input Current (V_{IN})

If complete settling occurs on the input, conversion results will be uneffected by the dynamic input current. If the settling is incomplete, it does not degrade the linearity performance of the device. It simply results in an offset/full-scale shift, see Figure 16. To simplify the analysis of input dynamic current, two separate cases are assumed: large capacitance at V_{IN} (C_{IN} > 0.01μF) and small capacitance at V_{IN} (C_{IN} < 0.01μF).

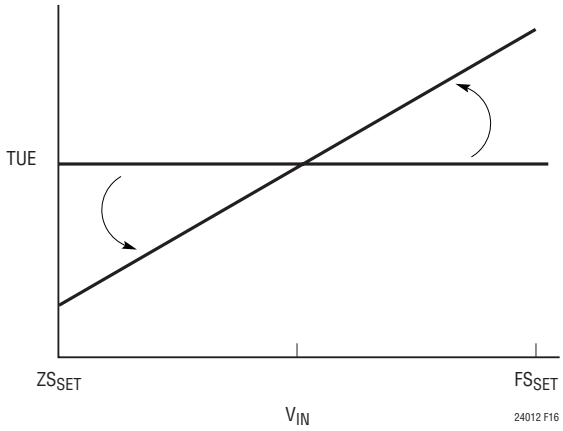

Figure 16. Offset/Full-Scale Shift

If the total capacitance at V_{IN} (see Figure 17) is small (<0.01μF), relatively large external source resistances (up to 20k for 20pF parasitic capacitance) can be tolerated without any offset/full-scale error. Figures 18 and 19 show a family of offset and full-scale error curves for various small valued input capacitors (C_{IN} < 0.01μF) as a function of input source resistance.

For large input capacitor values (C_{IN} > 0.01μF), the input spikes are averaged by the capacitor into a DC current. The gain shift becomes a linear function of input source

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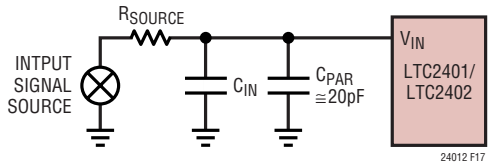

Figure 17. An RC Network at V_{IN}

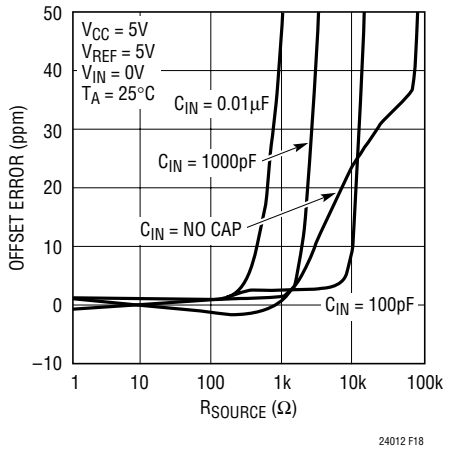

Figure 18. Offset vs R_{SOURCE} (Small C)

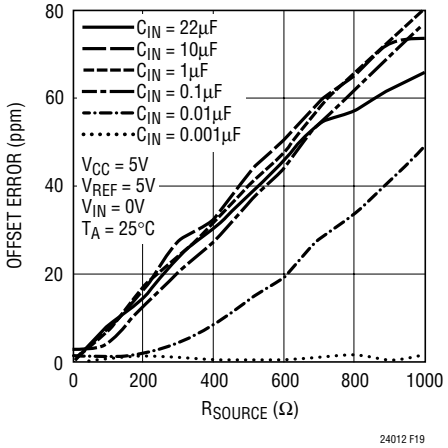

Figure 19. Offset vs R_{SOURCE} (Large C)

resistance independent of input capacitance, see Figures 20 and 21. The equivalent input impedance is 6.25MΩ. This results in ±400µA of input dynamic current at the extreme values of V_{IN} (V_{IN} = 0V and V_{IN} = V_{REF}, when V_{REF} = 5V). This corresponds to a 0.8ppm shift in offset and full-scale readings for every 10Ω of input source resistance.

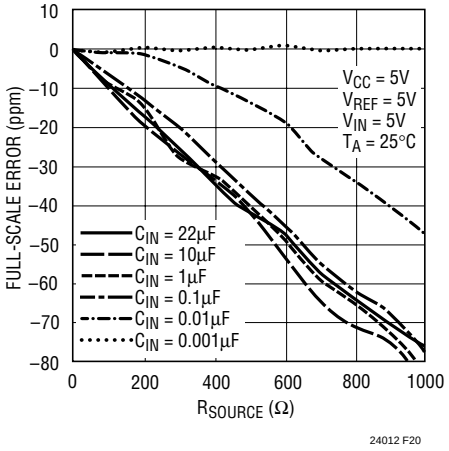

Figure 20. Full-Scale Error vs R_{SOURCE} (Large C)

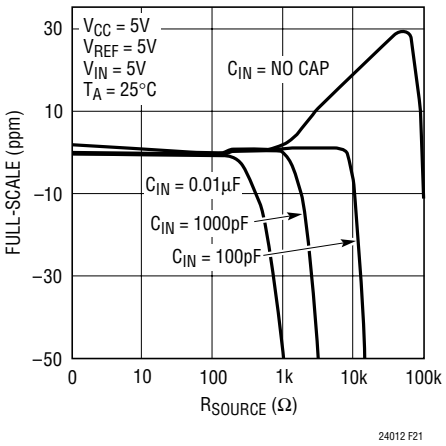

Figure 21. Full-Scale Error vs R_{SOURCE} (Small C)

In addition to the input current spikes, the input ESD protection diodes have a temperature dependent leakage current. This leakage current, nominally 1nA (±10nA max), results in a fixed offset shift of 10µV for a 10k source resistance.

The effect of input leakage current is evident for C_{IN} = 0 in Figures 18 and 21. A leakage current of 3nA results in a 150µV (30ppm) error for a 50k source resistance. As R_{SOURCE} gets larger, the switched capacitor input current begins to dominate.

Reference Current (V_{REF})

Similar to the analog input, the reference input has a dynamic input current. This current has negligible effect

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on the offset. However, the reference current at $V_{IN} = V_{REF}$ is similar to the input current at full-scale. For large values of reference capacitance ($C_{VREF} > 0.01\mu F$), the full-scale error shift is 0.08ppm/Ω of external reference resistance independent of the capacitance at V_{REF}, see Figure 22. If the capacitance tied to V_{REF} is small ($C_{VREF} < 0.01\mu F$), an input resistance of up to 20k (20pF parasitic capacitance at V_{REF}) may be tolerated, see Figure 23.

Unlike the analog input, the integral nonlinearity of the device can be degraded with excessive external RC time constants tied to the reference input. If the capacitance at node V_{REF} is small ($C_{VREF} < 0.01\mu F$), the reference input can tolerate large external resistances without reduction in INL, see Figure 24. If the external capacitance is large ($C_{VREF} > 0.01\mu F$), the linearity will be degraded by 0.04ppm/Ω independent of capacitance at V_{REF}, see Figure 25.

In addition to the dynamic reference current, the V_{REF} ESD protection diodes have a temperature dependent leakage current. This leakage current, nominally 1nA (±10nA max), results in a fixed full-scale shift of 10μV for a 10k source resistance.

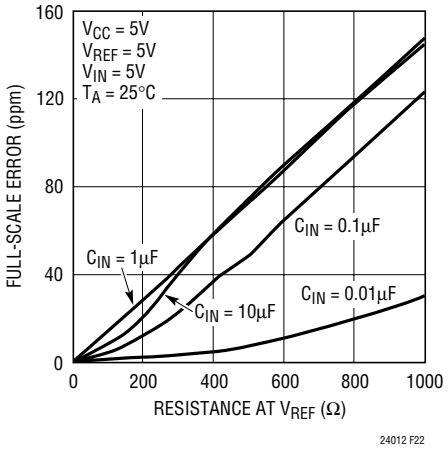

Figure 22. Full-Scale Error vs R_{VREF} (Large C)

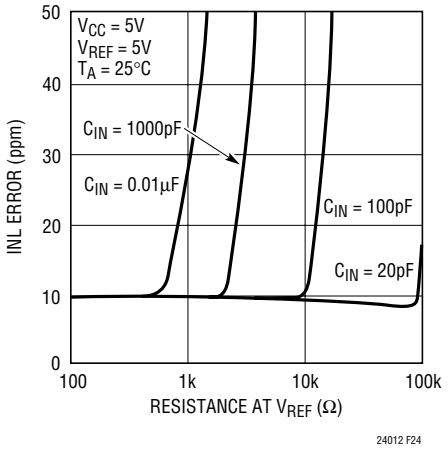

Figure 24. INL Error vs R_{VREF} (Small C)

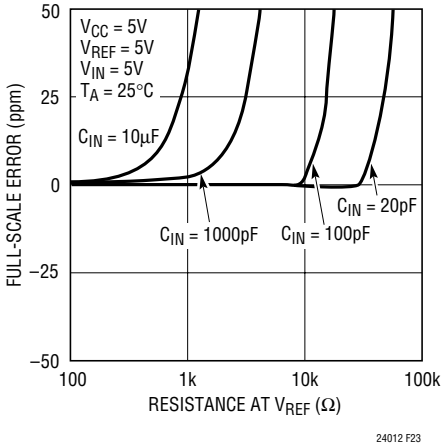

Figure 23. Full-Scale Error vs R_{VFEF} (Small C)

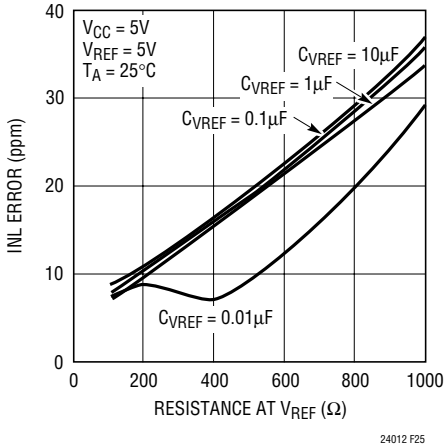

Figure 25. INL Error vs R_{VREF} (Large C)

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ANTIALIASING

One of the advantages delta-sigma ADCs offer over conventional ADCs is on-chip digital filtering. Combined with a large oversampling ratio, the LTC2401/LTC2402 significantly simplify antialiasing filter requirements.

The digital filter provides very high rejection except at integer multiples of the modulator sampling frequency (f_S), see Figure 26. The modulator sampling frequency is 256 • F_O, where F_O is the notch frequency (typically 50Hz or 60Hz). The bandwidth of signals not rejected by the digital filter is narrow (≈0.2%) compared to the bandwidth of the frequencies rejected.

As a result of the oversampling ratio (256) and the digital filter, minimal (if any) antialias filtering is required in front of the LTC2401/LTC2402. If passive RC components are placed in front of the LTC2401/LTC2402, the input dynamic current should be considered (see Input Current section). In cases where large effective RC time constants are used, an external buffer amplifier may be required to minimize the effects of input dynamic current.

The modulator contained within the LTC2401/LTC2402 can handle large-signal level perturbations without saturating. Signal levels up to 40% of V_{REF} do not saturate the analog modulator. These signals are limited by the input ESD protection to 300mV below ground and 300mV above V_{CC}.

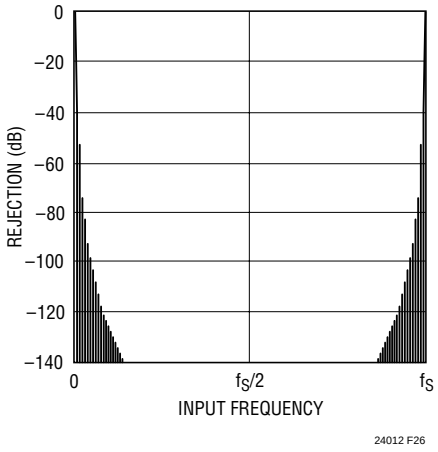

Figure 26. Sinc^4 Filter Rejection

Single Ended Half-Bridge Digitizer with Reference and Ground Sensing

Sensors convert real world phenomena (temperature, pressure, gas levels, etc.) into a voltage. Typically, this voltage is generated by passing an excitation current through the sensor. The wires connecting the sensor to the ADC form parasitic resistors R_{P1} and R_{P2}. The excitation current also flows through parasitic resistors R_{P1} and R_{P2}, as shown in Figure 27. The voltage drop across these parasitic resistors leads to systematic offset and full-scale errors.

In order to eliminate the errors associated with these parasitic resistors, the LTC2401/LTC2402 include a full-scale set input (FS_{SET}) and a zero-scale set input (ZS_{SET}). As shown in Figure 28, the FS_{SET} pin acts as a zero current full-scale sense input. Errors due to parasitic resistance R_{P1} in series with the half-bridge sensor are removed by the FS_{SET} input to the ADC. The absolute full-scale output of the ADC (data out = $FFFFFF_{HEX}$) will occur

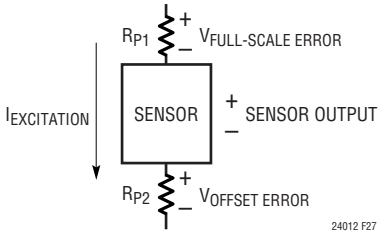

Figure 27. Errors Due to Excitation Currents

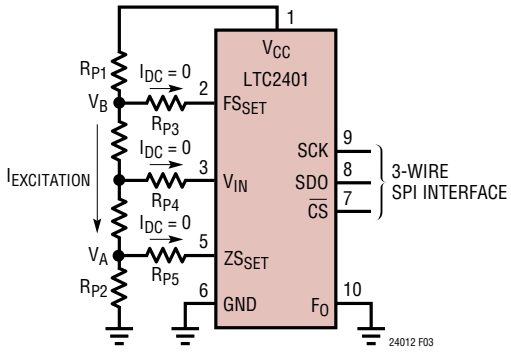

Figure 28. Half-Bridge Digitizer with Zero-Scale and Full-Scale Sense

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at $V_{IN} = V_B = FS_{SET}$, see Figure 29. Similarly, the offset errors due to R_{P2} are removed by the ground sense input ZS_{SET}. The absolute zero output of the ADC (data out = 000000_{HEX}) occurs at $V_{IN} = V_A = ZS_{SET}$. Parasitic resistors R_{P3} to R_{P5} have negligible errors due to the 1nA (typ) leakage current at pins FS_{SET}, ZS_{SET} and V_{IN}. The wide dynamic input range (–300mV to 5.3V) and low noise (0.6ppm RMS) enable the LTC2401 or the LTC2402 to directly digitize the output of the bridge sensor.

The LTC2402 is ideal for applications requiring continuous monitoring of two input sensors. As shown in Figure 30, the LTC2402 can monitor both a thermocouple temperature probe and a cold junction temperature sensor. Absolute temperature measurements can be performed with a variety of thermocouples using digital cold junction compensation.

The selection between CH0 and CH1 is automatic. Initially, after power-up, a conversion is performed on CH0. For each subsequent conversion, the input channel selection is alternated. Embedded within the serial data output is a status bit indicating which channel corresponds to the conversion result. If the conversion was performed on CH0, this bit (Bit 30) is LOW and is HIGH if the conversion was performed on CH1 (see Figure 31).

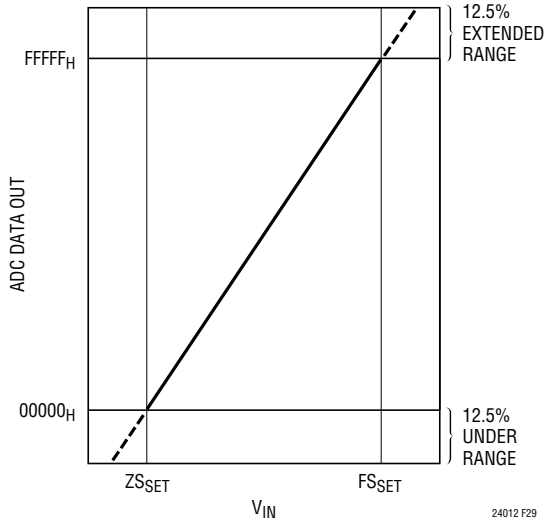

Figure 29. Transfer Curve with Zero-Scale and Full-Scale Set

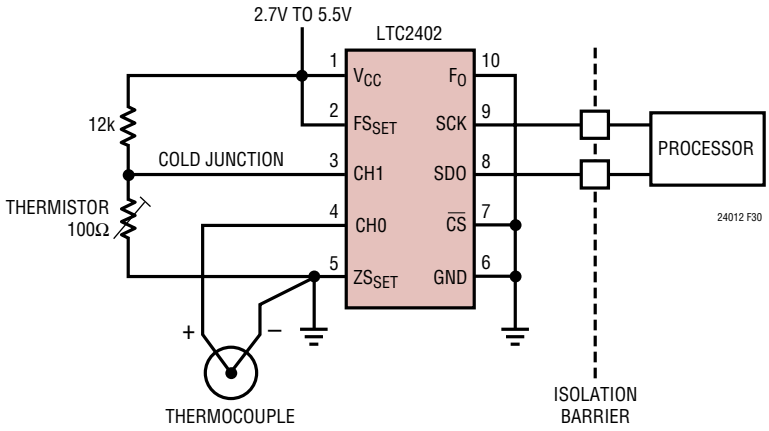

Figure 30. Isolated Temperature Measurement

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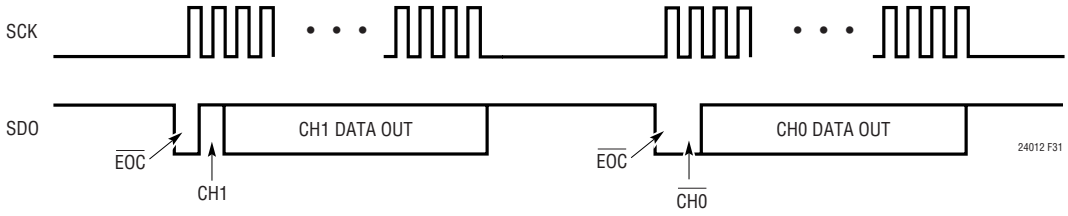

Figure 31. Embedded Selected Channel Indicator

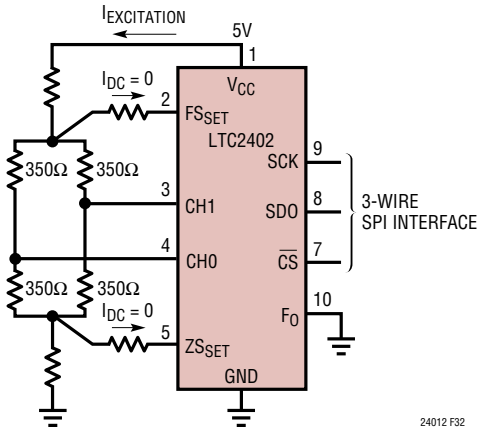

Figure 32. Pseudo Differential Strain Guage Application

There are no extra control or status pins required to perform the alternating 2-channel measurements. The LTC2402 only requires two digital signals (SCK and SDO). This simplification is ideal for isolated temperature measurements or systems where minimal control signals are available.

Pseudo Differential Applications

Generally, designers choose fully differential topologies for several reasons. First, the interface to a 4- or 6-wire bridge is simple (it is a differential output). Second, they require good rejection of line frequency noise. Third, they typically look at a small differential signal sitting on a large common mode voltage; they need accurate measurements of the differential signal independent of the common mode input voltage. Many applications currently using fully differential analog-to-digital converters for any of the above reasons may migrate to a pseudo differential conversion using the LTC2402.

Direct Connection to a Full Bridge

The LTC2402 interfaces directly to a 4- or 6-wire bridge, as shown in Figure 32. The LTC2402 includes a FS_{SET} and a ZS_{SET} for sensing the excitation voltage directly across the bridge. This eliminates errors due to excitation currents flowing through parasitic resistors. The LTC2402 also includes two single ended input channels which can tie directly to the differential output of the bridge. The two conversion results may be digitally subtracted yielding the differential result.

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The LTC2402's single ended rejection of line frequencies (±2%) and harmonics is better than 110dB. Since the device performs two independent single ended conversions each with >110dB rejection, the overall common mode and differential rejection is much better than the 80dB rejection typically found in other differential input delta-sigma converters.

In addition to excellent rejection of line frequency noise, the LTC2402 also exhibits excellent single ended noise rejection over a wide range of frequencies due to its 4th order sinc filter. Each single ended conversion independently rejects high frequency noise (>60Hz). Care must be taken to insure noise at frequencies below 15Hz and at multiples of the ADC sample rate (15,360Hz) are not present. For this application, it is recommended the LTC2402 is placed in close proximity to the bridge sensor in order to reduce the noise injected into the ADC input. By performing three successive conversions (CH0-CH1-CH0), the drift and low frequency noise can be measured and compensated for digitally.

The absolute accuracy (less than 10 ppm total error) of the LTC2402 enables extremely accurate measurement of small signals sitting on large voltages. Each of the two pseudo differential measurements performed by the LTC2402 is absolutely accurate independent of the common mode voltage output from the bridge. The pseudo differential result obtained from digitally subtracting the two single ended conversion results is accurate to within the noise level of the device ($3\mu V_{RMS}$) times the square root of 2, independent of the common mode input voltage.

Typically, a bridge sensor outputs 2mV/V full scale. With a 5V excitation, this translates to a full-scale output of 10mV. Divided by the RMS noise of 4.2μV(=3μV • 1.414), this circuit yields 2,300 counts with no averaging or amplification. If more counts are required, several conversions may be averaged (the number of effective counts is increased by a factor of square root of 2 for each doubling of averages).

An RTD Temperature Digitizer

RTDs used in remote temperature measurements often have long lead lengths between the ADC and RTD sensor. These long lead lengths lead to voltage drops due to excitation current in the interconnect to the RTD. This voltage drop can be measured and digitally removed using the LTC2402 (see Figure 33).

The excitation current (typically 200μA) flows from the ADC through a long lead length to the remote temperature sensor (RTD). This current is applied to the RTD, whose resistance changes as a function of temperature (100Ω to 400Ω for 0°C to 800°C). The same excitation current flows back to the ADC ground and generates another voltage drop across the return leads. In order to get an accurate measurement of the temperature, these voltage drops must be measured and removed from the conversion result. Assuming the resistance is approximately the same

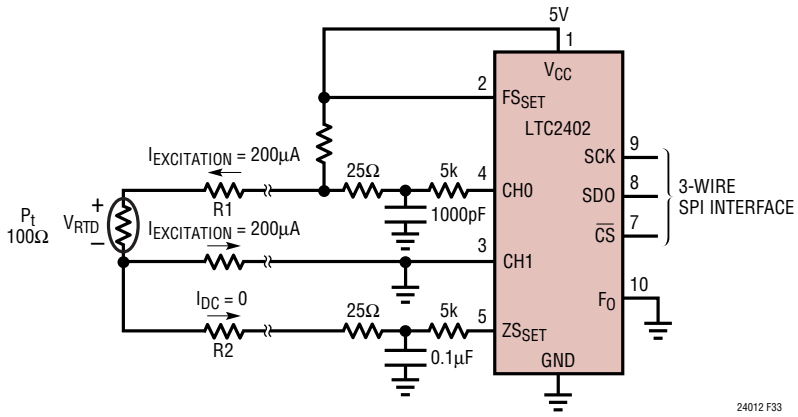

Figure 33. RTD Remote Temperature Measurement

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for the forward and return paths (R1 = R2), the auxiliary channel on the LTC2402 can measure this drop. These errors are then removed with simple digital correction.

The result of the first conversion on CH0 corresponds to an input voltage of $V_{RTD} + R1 \bullet I_{EXCITATION}$. The result of the second conversion (CH1) is $-R1 \bullet I_{EXCITATION}$. Note, the LTC2402's input range is not limited to the supply rails, it has underrange capabilities. The device's input range is –300mV to V_{REF} + 300mV. Adding the two conversion results together, the voltage drop across the RTD's leads are cancelled and the final result is V_{RTD}.

An Isolated, 24-Bit Data Acquisition System

The LTC1535 is useful for signal isolation. Figure 34 shows a fully isolated, 24-bit differential input A/D converter implemented with the LTC1535 and LTC2402. Power on the isolated side is regulated by an LT1761-5.0 low noise, low dropout micropower regulator. Its output is suitable for driving bridge circuits and for ratiometric applications.

During power-up, the LTC2402 becomes active at V_{CC} = 2.3V, while the isolated side of the LTC1535 must wait for V_{CC2} to reach its undervoltage lockout threshold of 4.2V. Below 4.2V, the LTC1535's driver outputs Y and Z are in a high impedance state, allowing the 1kΩ pull-down to define the logic state at SCK. When the LTC2402 first becomes active, it samples SCK; a logic "0" provided by the 1kΩ pull-down invokes the external serial clock mode. In this mode, the LTC2402 is controlled by a single clock line from the nonisolated side of the barrier, through the LTC1535's driver output Y. The entire power-up sequence, from the time power is applied to V_{CC1} until the LT1761's output has reached 5V, is approximately 1ms.

Data returns to the nonisolated side through the LTC1535's receiver at RO. An internal divider on receiver input B sets a logic threshold of approximately 3.4V at input A, facilitating communications with the LTC2402's SDO output without the need for any external components.

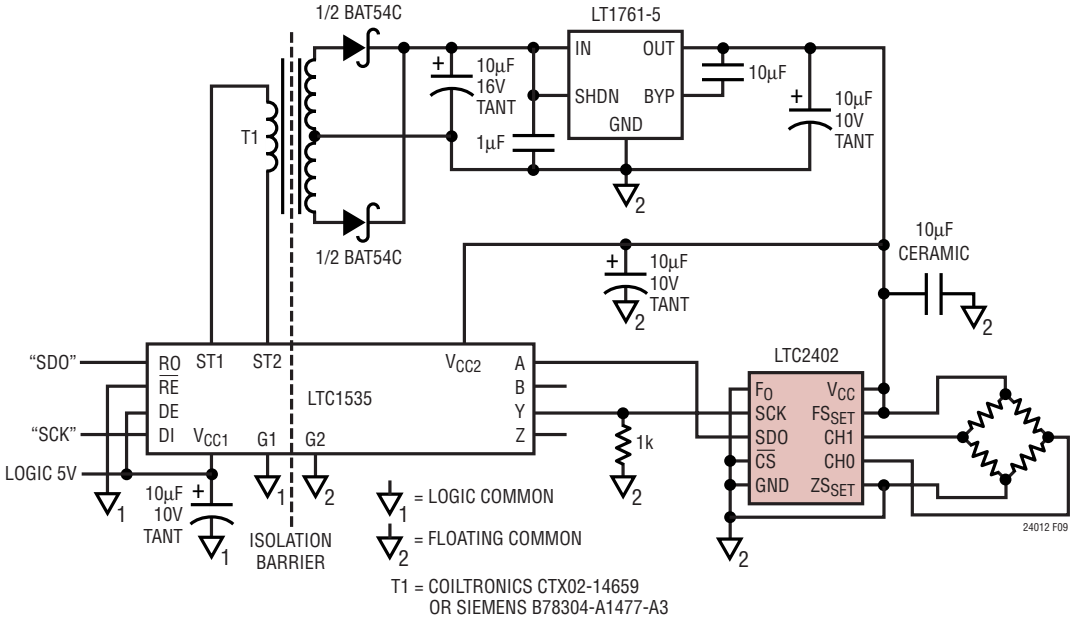
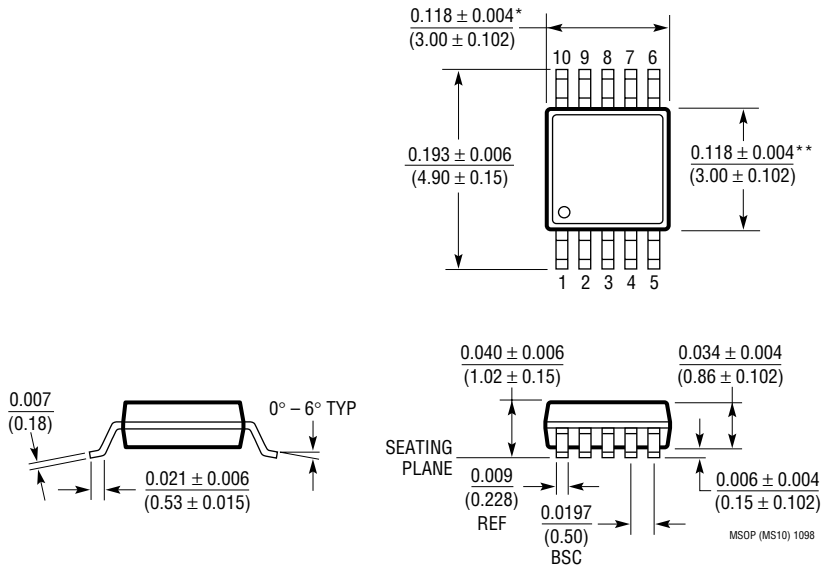


Figure 34. Complete, Isolated 24-Bit Data Acquisition System

PACKAGE INFORMATION

Dimensions in inches (millimeters) unless otherwise noted.

MS10 Package
10-Lead Plastic MSOP
(LTC DWG # 05-08-1661)



* DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

** DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

TYPICAL APPLICATION

Figure 35 shows the block diagram of a demo circuit (contact LTC for a demonstration) of a multichannel isolated temperature measurement system. This circuit decodes an address to select which LTC2402 receives a 32-bit burst of SCK signal. All devices independently convert either the thermal couple output or the thermistor cold juntion output. After each conversion, the devices enter their sleep state and wait for the SCK signal before clocking out data and beginning the next conversion.

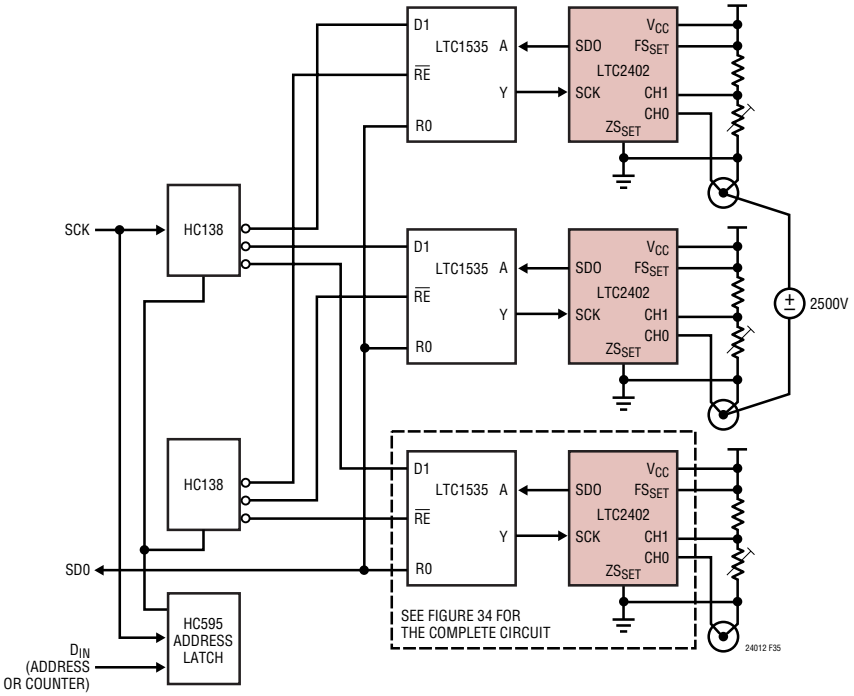


Figure 35. Mulitchannel Isolated Temperature Measurement System

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1019	Precision Bandgap Reference, 2.5V, 5V	3ppm/°C Drift, 0.05% Max
LTC1050	Precision Chopper Stabilized Op Amp	No External Components 5µV Offset, 1.6µV_{P-P} Noise
LT1236A-5	Precision Bandgap Reference, 5V	0.05% Max, 5ppm/°C Drift
LTC1391	8-Channel Multiplexer	Low R_{ON}: 45Ω, Low Charge Injection Serial Interface
LT1460	Micropower Series Reference	0.075% Max, 10ppm/°C Max Drift, 2.5V, 5V and 10V Versions
LT1461-2.5	Precision Micropower Voltage Reference	50µA Supply Current, 3ppm/°C Drift
LTC1535	Isolated RS485 Transceiver	2500V_{RMS} Isolation
LTC2400	24-Bit, No Latency ΔΣ ADC in SO-8	4ppm INL, 10ppm Total Unadjusted Error, 200µA
LTC2404/LTC2408	4-/8-Channel, 24-Bit, No Latency ΔΣ ADC	4ppm INL, 10ppm Total Unadjusted Error, 200µA
LTC2410	24-Bit, Fully Differential, No Latency ΔΣ ADC in SSOP-16	0.16ppm Noise, 2ppm INL, 10ppm Total Unadjusted Error, 200µA
LTC2411	24-Bit, Fully Differential, No Latency ΔΣ ADC in MS10	0.29ppm Noise, 4ppm INL, 10ppm Total Unadjusted Error, 200µA
LTC2413	24-Bit, No Latency ΔΣ ADC	Simultaneous 50Hz and 60Hz Rejection, 0.16ppm Noise
LTC2420	20-Bit, No Latency ΔΣ ADC in SO-8	1.2ppm Noise, 8ppm INL, Pin Compatible with LTC2400
LTC2424/LTC2428	4-/8-Channel, 20-Bit, No Latency ΔΣ ADC	1.2ppm Noise, 8ppm INL, Pin Compatible with LTC2404/LTC2408

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